AEROFLEX MCM MODELS

Description:

- A six die multi-chip model (MCM) on an alumina substrate, three on top and three on bottom. Interposers connect from substrate to silicon die

Provided:

- Single line, non-coupled S-parameter models from MCM pin to silicon die bump for all signals on the module (total 75)
  - 21 address/control/clock, each with external pin + 6 internal die bumps (7 ports, .s7p)
  - 54 data/data mask: external pin + 1 internal die bump (2 ports, .s1p)

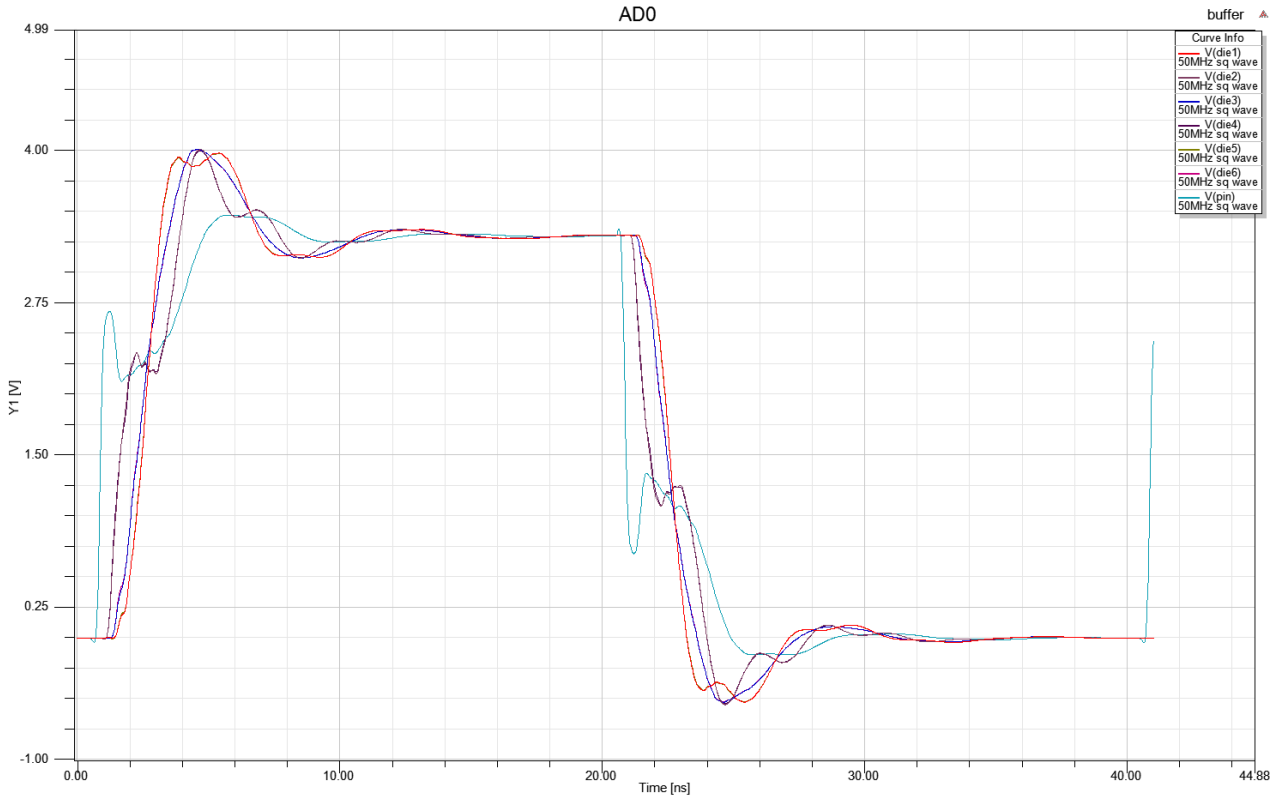
Intended use:

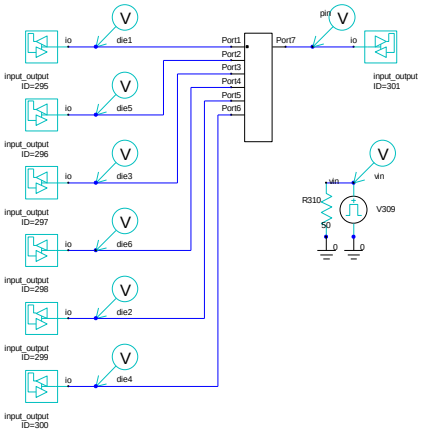
- Include as part of system level simulation model, with memory die I/O buffer model on the die side of the model and remaining interconnect models and I/O buffer models on the other

RESULTS, AD0

Setup:

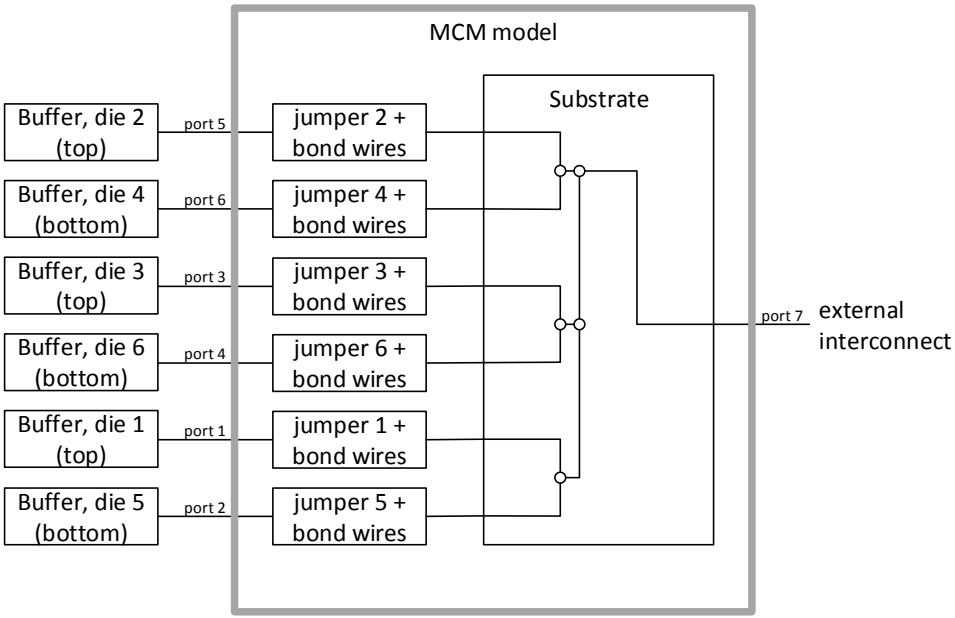
- Ansys Sidesigner 2014.0.2
- Micron MT48LC32M16A2TG “y27b.ibs”, Rev 2.4: 04/14/2004, “dq” I/O buffer
- driving at pin, receiving at each die bump



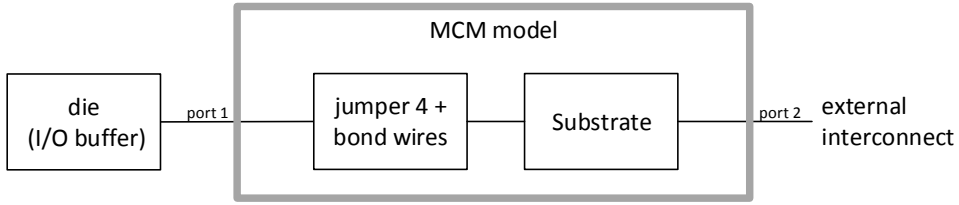


MODEL STRUCTURE

AD[12:2], BA[1:0], CASB,
CKE, CLK, CSB, RASB, WEB



DQ[7:0,M]_[6:1]



Note: die 1, die 2, die 3 are top
die 4, die 5, die 6 are bottom

ADDRESS, CONTROL, AND CLOCK MODELS

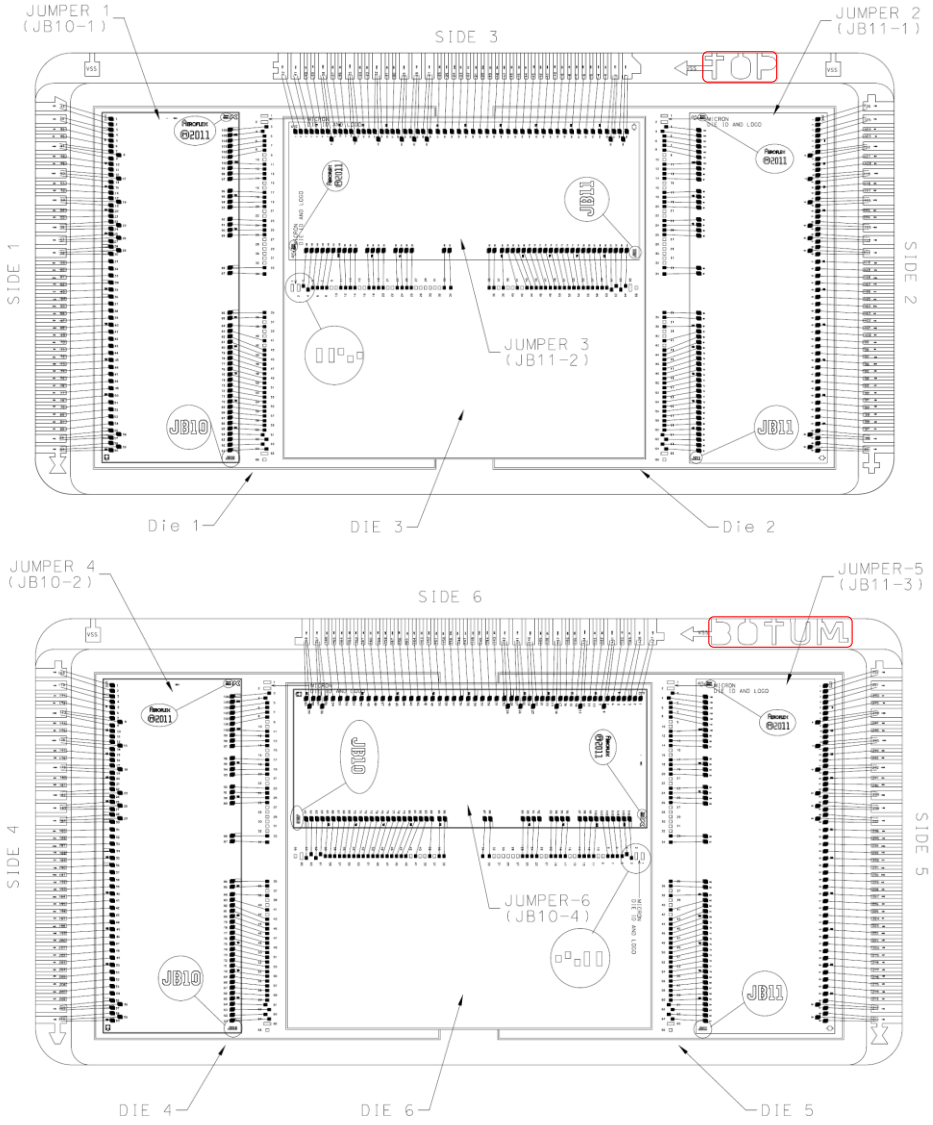
model	port 1	port 2	port 3	port 4	port 5	port 6	port 7
pm7147a-e1_AD0.s7p	[AD0_DIE1,	AD0_DIE5,	AD0_DIE3,	AD0_DIE6,	AD0_DIE2,	AD0_DIE4,	AD0]
pm7147a-e1_AD1.s7p	[AD1_DIE1,	AD1_DIE5,	AD1_DIE3,	AD1_DIE6,	AD1_DIE2,	AD1_DIE4,	AD1]
pm7147a-e1_AD2.s7p	[AD2_DIE1,	AD2_DIE5,	AD2_DIE3,	AD2_DIE6,	AD2_DIE2,	AD2_DIE4,	AD2]
pm7147a-e1_AD3.s7p	[AD3_DIE1,	AD3_DIE5,	AD3_DIE3,	AD3_DIE6,	AD3_DIE2,	AD3_DIE4,	AD3]
pm7147a-e1_AD4.s7p	[AD4_DIE1,	AD4_DIE5,	AD4_DIE3,	AD4_DIE6,	AD4_DIE2,	AD4_DIE4,	AD4]
pm7147a-e1_AD5.s7p	[AD5_DIE1,	AD5_DIE5,	AD5_DIE3,	AD5_DIE6,	AD5_DIE2,	AD5_DIE4,	AD5]
pm7147a-e1_AD6.s7p	[AD6_DIE1,	AD6_DIE5,	AD6_DIE3,	AD6_DIE2,	AD6_DIE4,	AD6_DIE6,	AD6]
pm7147a-e1_AD7.s7p	[AD7_DIE1,	AD7_DIE5,	AD7_DIE3,	AD7_DIE6,	AD7_DIE2,	AD7_DIE4,	AD7]
pm7147a-e1_AD8.s7p	[AD8_DIE1,	AD8_DIE5,	AD8_DIE3,	AD8_DIE6,	AD8_DIE2,	AD8_DIE4,	AD8]
pm7147a-e1_AD9.s7p	[AD9_DIE1,	AD9_DIE5,	AD9_DIE3,	AD9_DIE6,	AD9_DIE2,	AD9_DIE4,	AD9]
pm7147a-e1_AD10.s7p	[AD10_DIE1,	AD10_DIE5,	AD10_DIE3,	AD10_DIE6,	AD10_DIE2,	AD10_DIE4,	AD10]
pm7147a-e1_AD11.s7p	[AD11_DIE1,	AD11_DIE5,	AD11_DIE3,	AD11_DIE6,	AD11_DIE2,	AD11_DIE4,	AD11]
pm7147a-e1_AD12.s7p	[AD12_DIE1,	AD12_DIE5,	AD12_DIE3,	AD12_DIE6,	AD12_DIE2,	AD12_DIE4,	AD12]
pm7147a-e1_BA0.s7p	[BA0_DIE1,	BA0_DIE5,	BA0_DIE3,	BA0_DIE6,	BA0_DIE2,	BA0_DIE4,	BA0]
pm7147a-e1_BA1.s7p	[BA1_DIE1,	BA1_DIE5,	BA1_DIE3,	BA1_DIE6,	BA1_DIE2,	BA1_DIE4,	BA1]
pm7147a-e1_CASB.s7p	[CASB_DIE1,	CASB_DIE5,	CASB_DIE3,	CASB_DIE6,	CASB_DIE2,	CASB_DIE4,	CASB]
pm7147a-e1_CKE.s7p	[CKE_DIE1,	CKE_DIE5,	CKE_DIE3,	CKE_DIE6,	CKE_DIE2,	CKE_DIE4,	CKE]
pm7147a-e1_CLK.s7p	[CLK_DIE1,	CLK_DIE5,	CLK_DIE3,	CLK_DIE6,	CLK_DIE2,	CLK_DIE4,	CLK]
pm7147a-e1_CSB.s7p	[CSB_DIE1,	CSB_DIE5,	CSB_DIE3,	CSB_DIE6,	CSB_DIE2,	CSB_DIE4,	CSB]
pm7147a-e1_RASB.s7p	[RASB_DIE1,	RASB_DIE5,	RASB_DIE3,	RASB_DIE6,	RASB_DIE2,	RASB_DIE4,	RASB]
pm7147a-e1_WEB.s7p	[WEB_DIE1,	WEB_DIE5,	WEB_DIE3,	WEB_DIE6,	WEB_DIE2,	WEB_DIE4,	WEB]

DQ/DQM MODELS

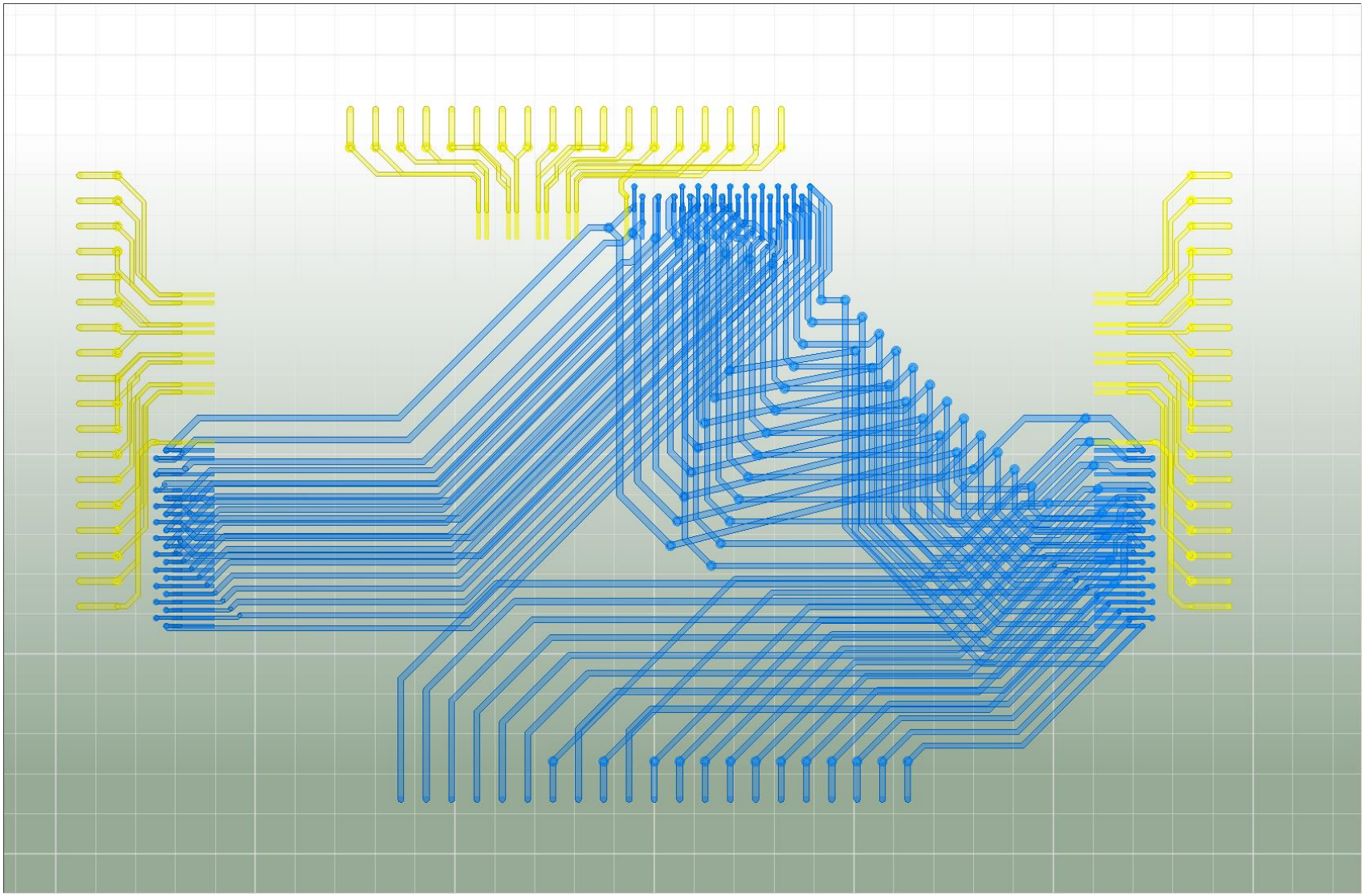
model	port 1	port 2
pm7147a-e1_dq0_1.s2p	[dq0_die1,	DQ0_1]
pm7147a-e1_dq1_1.s2p	[dq1_die1,	DQ1_1]
pm7147a-e1_dq2_1.s2p	[dq2_die1,	DQ2_1]
pm7147a-e1_dq3_1.s2p	[dq3_die1,	DQ3_1]
pm7147a-e1_dq4_1.s2p	[dq4_die1,	DQ4_1]
pm7147a-e1_dq5_1.s2p	[dq5_die1,	DQ5_1]
pm7147a-e1_dq6_1.s2p	[dq6_die1,	DQ6_1]
pm7147a-e1_dq7_1.s2p	[dq7_die1,	DQ7_1]
pm7147a-e1_dqm_1.s2p	[dqm_die1,	DQM_1]
pm7147a-e1_dq0_2.s2p	[dq0_die2,	DQ0_2]
pm7147a-e1_dq1_2.s2p	[dq1_die2,	DQ1_2]
pm7147a-e1_dq2_2.s2p	[dq2_die2,	DQ2_2]
pm7147a-e1_dq3_2.s2p	[dq3_die2,	DQ3_2]
pm7147a-e1_dq4_2.s2p	[dq4_die2,	DQ4_2]
pm7147a-e1_dq5_2.s2p	[dq5_die2,	DQ5_2]
pm7147a-e1_dq6_2.s2p	[dq6_die2,	DQ6_2]
pm7147a-e1_dq7_2.s2p	[dq7_die2,	DQ7_2]
pm7147a-e1_dqm_2.s2p	[dqm_die2,	DQM_2]
pm7147a-e1_dq0_3.s2p	[dq0_die3,	DQ0_3]
pm7147a-e1_dq1_3.s2p	[dq1_die3,	DQ1_3]
pm7147a-e1_dq2_3.s2p	[dq2_die3,	DQ2_3]
pm7147a-e1_dq3_3.s2p	[dq3_die3,	DQ3_3]
pm7147a-e1_dq4_3.s2p	[dq4_die3,	DQ4_3]
pm7147a-e1_dq5_3.s2p	[dq5_die3,	DQ5_3]
pm7147a-e1_dq6_3.s2p	[dq6_die3,	DQ6_3]
pm7147a-e1_dq7_3.s2p	[dq7_die3,	DQ7_3]
pm7147a-e1_dqm_3.s2p	[dqm_die3,	DQM_3]

model	port 1	port 2
pm7147a-e1_dq0_4.s2p	[dq0_die4,	DQ0_4]
pm7147a-e1_dq1_4.s2p	[dq1_die4,	DQ1_4]
pm7147a-e1_dq2_4.s2p	[dq2_die4,	DQ2_4]
pm7147a-e1_dq3_4.s2p	[dq3_die4,	DQ3_4]
pm7147a-e1_dq4_4.s2p	[dq4_die4,	DQ4_4]
pm7147a-e1_dq5_4.s2p	[dq5_die4,	DQ5_4]
pm7147a-e1_dq6_4.s2p	[dq6_die4,	DQ6_4]
pm7147a-e1_dq7_4.s2p	[dq7_die4,	DQ7_4]
pm7147a-e1_dqm_4.s2p	[dqm_die4,	DQM_4]
pm7147a-e1_dq0_5.s2p	[dq0_die5,	DQ0_5]
pm7147a-e1_dq1_5.s2p	[dq1_die5,	DQ1_5]
pm7147a-e1_dq2_5.s2p	[dq2_die5,	DQ2_5]
pm7147a-e1_dq3_5.s2p	[dq3_die5,	DQ3_5]
pm7147a-e1_dq4_5.s2p	[dq4_die5,	DQ4_5]
pm7147a-e1_dq5_5.s2p	[dq5_die5,	DQ5_5]
pm7147a-e1_dq6_5.s2p	[dq6_die5,	DQ6_5]
pm7147a-e1_dq7_5.s2p	[dq7_die5,	DQ7_5]
pm7147a-e1_dqm_5.s2p	[dqm_die5,	DQM_5]
pm7147a-e1_dq0_6.s2p	[dq0_die6,	DQ0_6]
pm7147a-e1_dq1_6.s2p	[dq1_die6,	DQ1_6]
pm7147a-e1_dq2_6.s2p	[dq2_die6,	DQ2_6]
pm7147a-e1_dq3_6.s2p	[dq3_die6,	DQ3_6]
pm7147a-e1_dq4_6.s2p	[dq4_die6,	DQ4_6]
pm7147a-e1_dq5_6.s2p	[dq5_die6,	DQ5_6]
pm7147a-e1_dq6_6.s2p	[dq6_die6,	DQ6_6]
pm7147a-e1_dq7_6.s2p	[dq7_die6,	DQ7_6]
pm7147a-e1_dqm_6.s2p	[dqm_die6,	DQM_6]

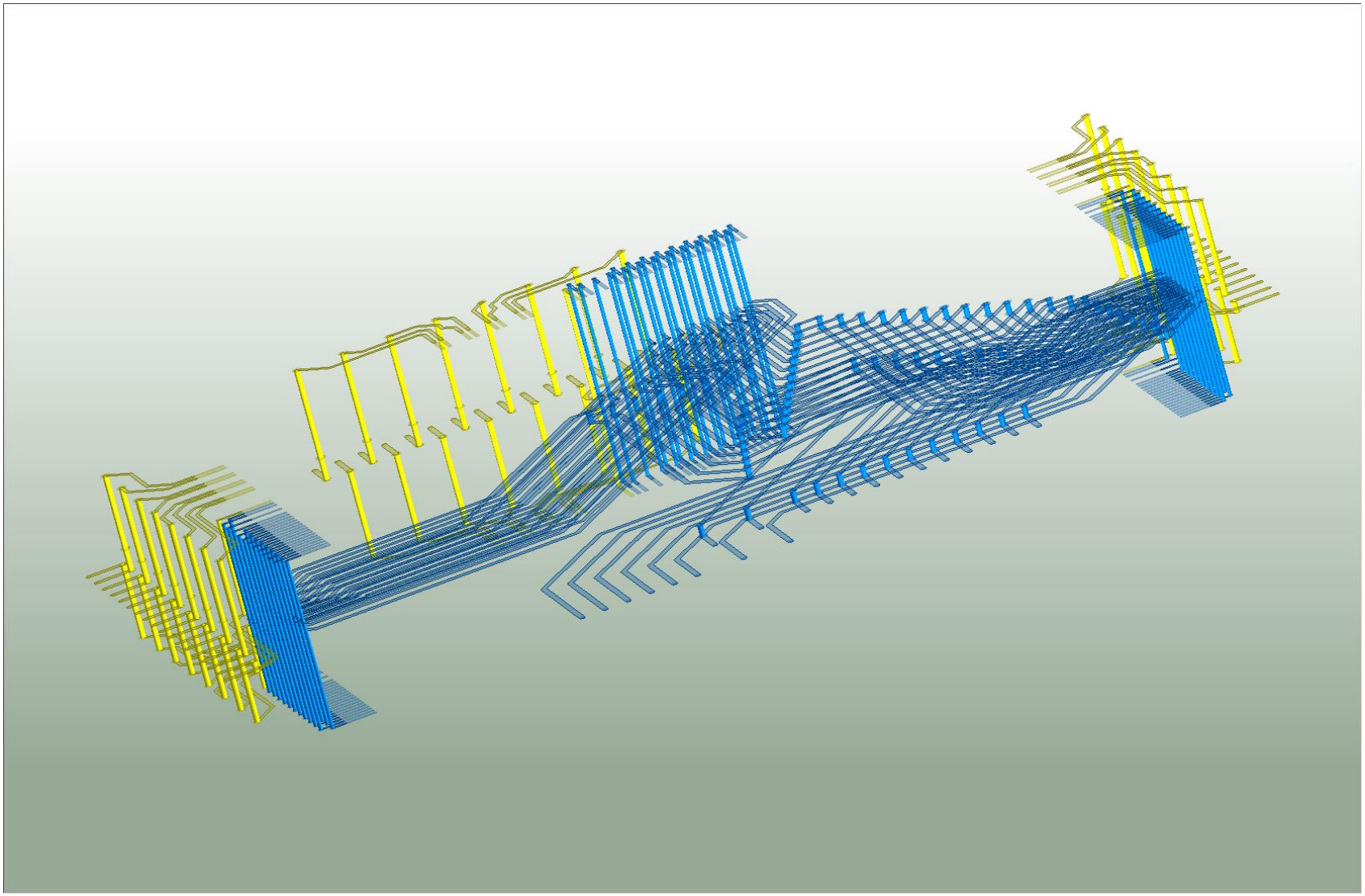
DIE PLACEMENT



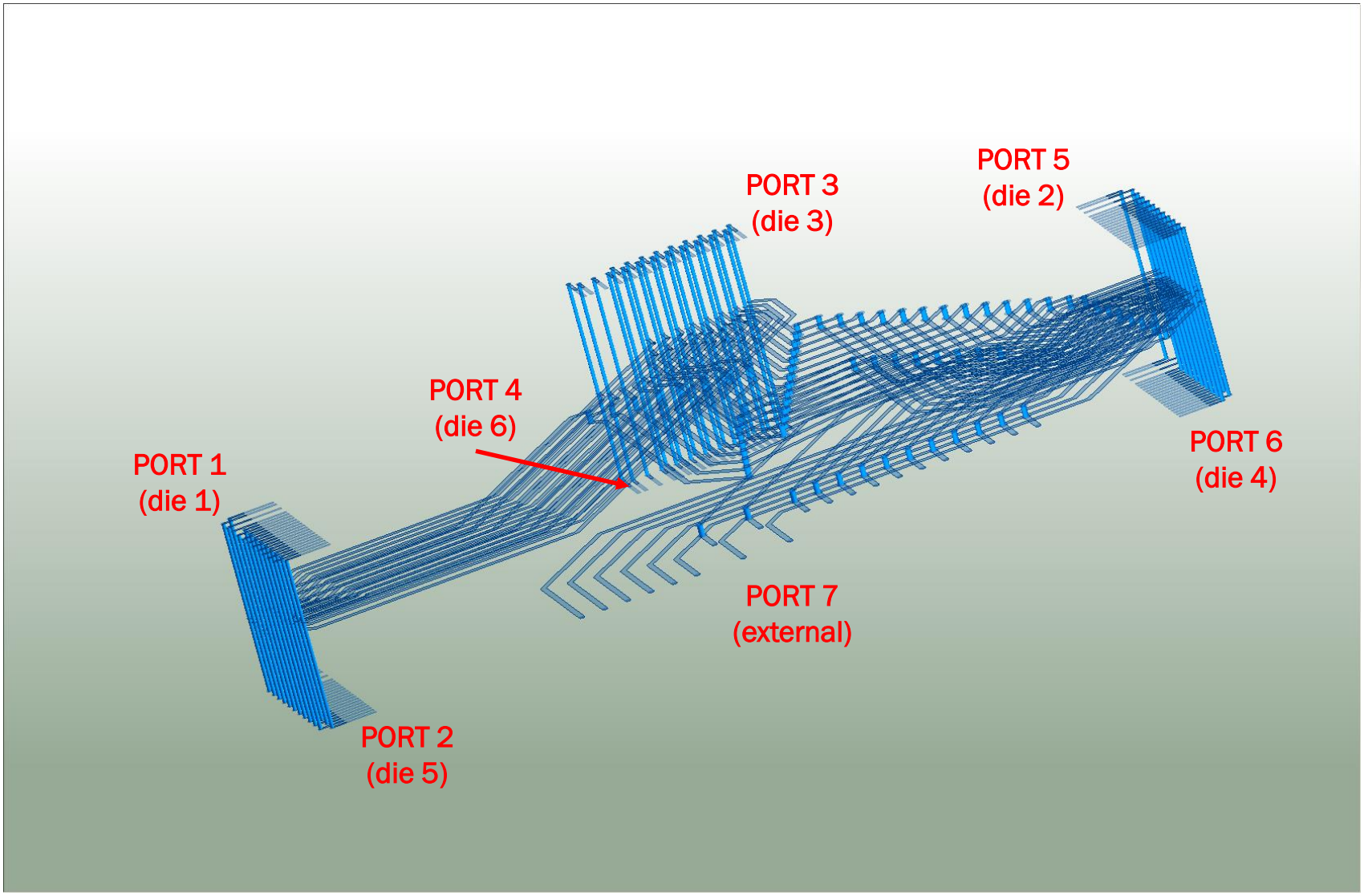
SIGNAL ROUTING, PLAN



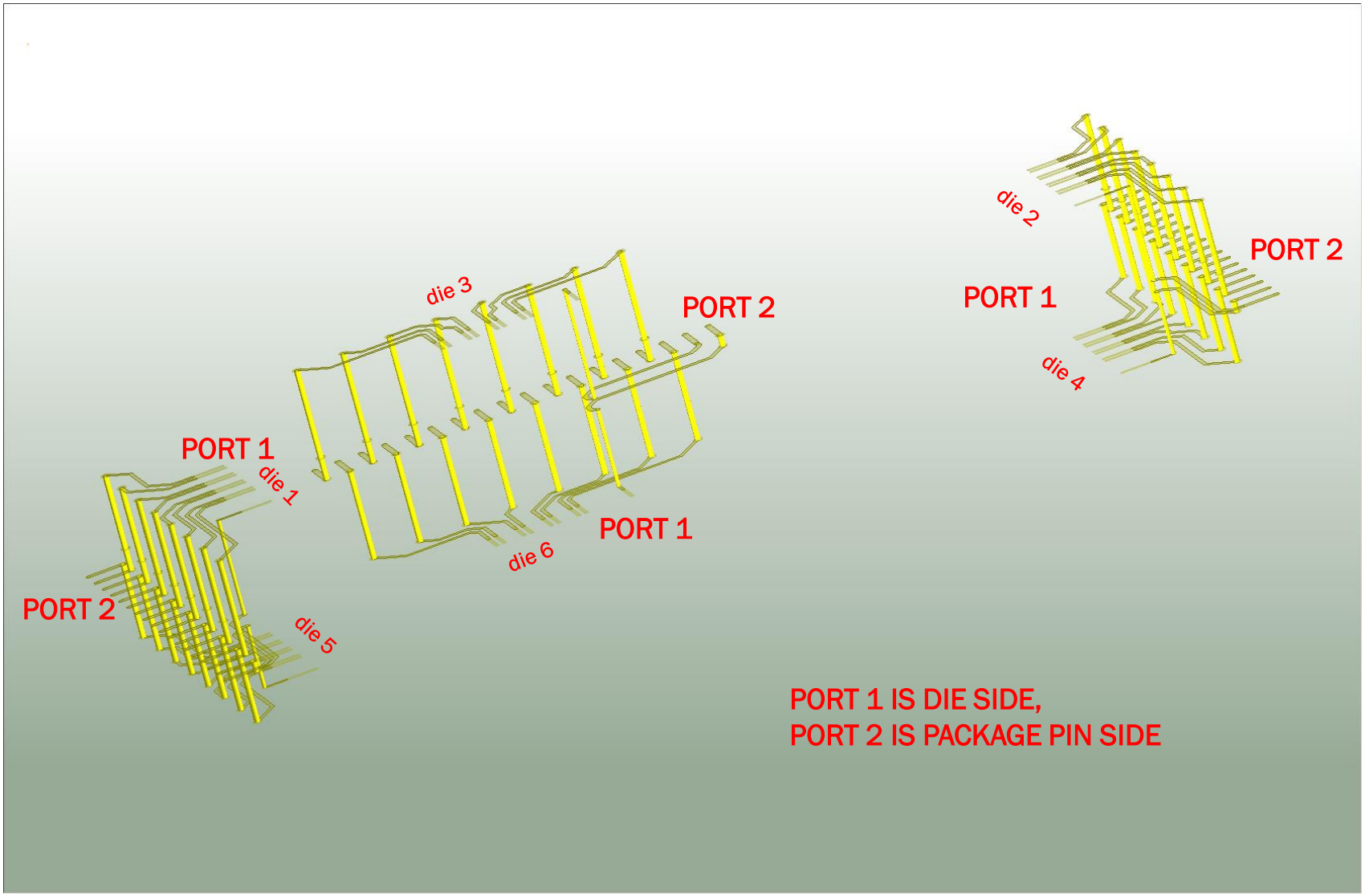
SIGNAL ROUTING, ISOMETRIC



ADDRESS / CONTROL / CLOCK ROUTING



DATA ROUTING



REFERENCE DOCUMENTS

3.0G SDRAM Wirebond Diagram.pdf

UT8SDMQ64-6.pdf (MCM data sheet)

Jumper Die and Wire Bond RLC Schematics.pdf

Interposer__Wirebond_IBIS_RLC_SE_netlist

ut8sdmq64m40.ibs, ut8sdmq64m48.ibs

pm7147a-e1_chain.mcm