User Manual

1Gb NOR Flash Evaluation Board

UT81NDQ512G8T

Product Name	Manufacturer Part Number	SMD#	Device Type
4Tb NAND Flash	UT81NDQ512G8T-KU060-R1-EVB	N/A	N/A

Features

- Open NAND Flash Interface (ONFI) 4.0-compliant
- JEDEC NAND Flash Interoperability (JESD230C) compliant
- Triple-level cell (TLC)
- B17A Industrial die source
- Organization
  - Page size x8: 18,592 bytes (16,384 + 2208 bytes)
  - Block size: 2304 pages, (36,864K + 4968K bytes)
  - Plane size: 4 planes x 504 blocks
  - Device size: 16128 blocks
- NV-DDR3 I/O performance
  - Up to NV-DDR3 timing mode 9
  - Clock rate: 3ns (NV-DDR3)
  - Read/write throughput per pin: 667 MT/s
  - Tested over temperature in mode 9
- NV-DDR2 I/O performance
  - Up to NV-DDR2 timing mode 8
  - Clock rate: 3.75ns (NV-DDR2)
  - Read/write throughput per pin: 533 MT/s
  - Tested over temperature in mode 6
- Asynchronous I/O performance
  - Up to asynchronous timing mode 5
  - tRC/tWC: 20ns (MIN)
  - Read/write throughput per pin: 50 MT/s
  - Tested over temperature in mode 5
- TLC Array performance
  - SNAP READ operation time without VPP: 51µs(TYP)
  - Single-Plane READ PAGE operation time without/with VPP : 74/73µs (TYP)
  - Multi-Plane READ PAGE operation time without VPP: 88µs(TYP)
  - Effective Program page time without VPP : 1900µs(TYP)
  - Erase block time: 15ms (TYP)
- Operating Voltage Range
  - VCC: 2.7–3.6V
  - VCCQ: 1.14–1.26V, 1.7–1.95V
- Command set: ONFI NAND Flash Protocol
- Data is required to be randomized by the external host prior to being inputted to the NAND device, see External Data Randomization in the User Manual
- First block (block address 00h) is valid when shipped from factory. For minimum required ECC, see Error Management in the User Manual

- RESET (FFh) required as first command after power-on
- Operation status byte provides software method for detecting
  - Operation completion
  - Pass/fail condition
  - Write-protect status
- Data strobe (DQS) signals provide a hardware method for synchronizing data DQ in the NV-DDR2/NVDDR3 interface
- Copyback operations supported within the plane from which data is read
- On-die Termination (ODT)
- Quality and reliability
  - Testing methodology: JESD47
  - Data retention: JESD47 compliant
  - TLC Endurance: 3,000 PROGRAM/ERASE cycles
  - SLC Endurance: 40,000 PROGRAM/ERASE cycles
- Package
  - 132-ball BGA
  - ΘJC : 2.68 °C/W

1 Introduction

The UT81NDQ512G8T-KU060-R1-EVB Development Board provides a rapid prototyping platform for the 4Tb NAND Flash. The evaluation board has been developed for the Xilinx KU060 FPGA, but is VITA compliant and should work with other FPGA platforms with a VITA compliant FMC. Headers allow access to all NAND signals. I/O voltage is controlled with a switch to allow either 1.8V or 1.2V I/O operation on the eval board.

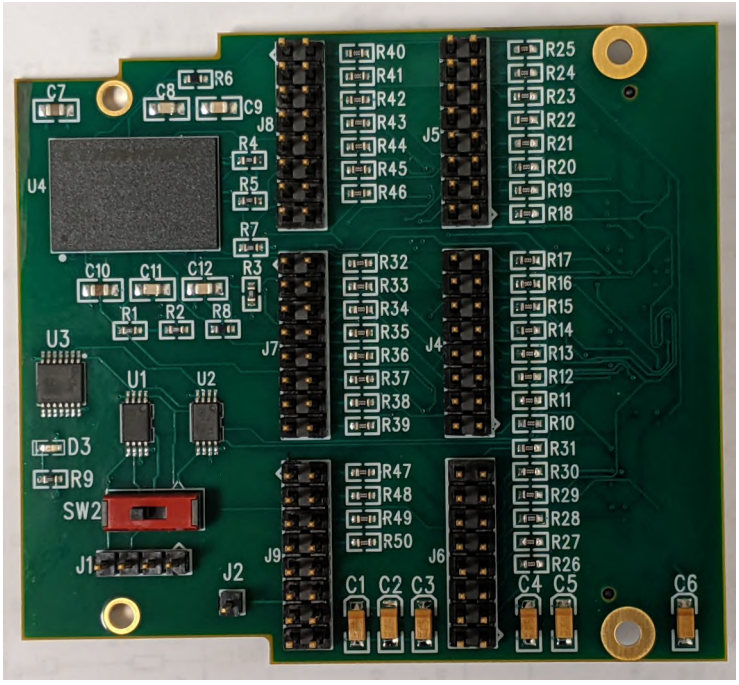
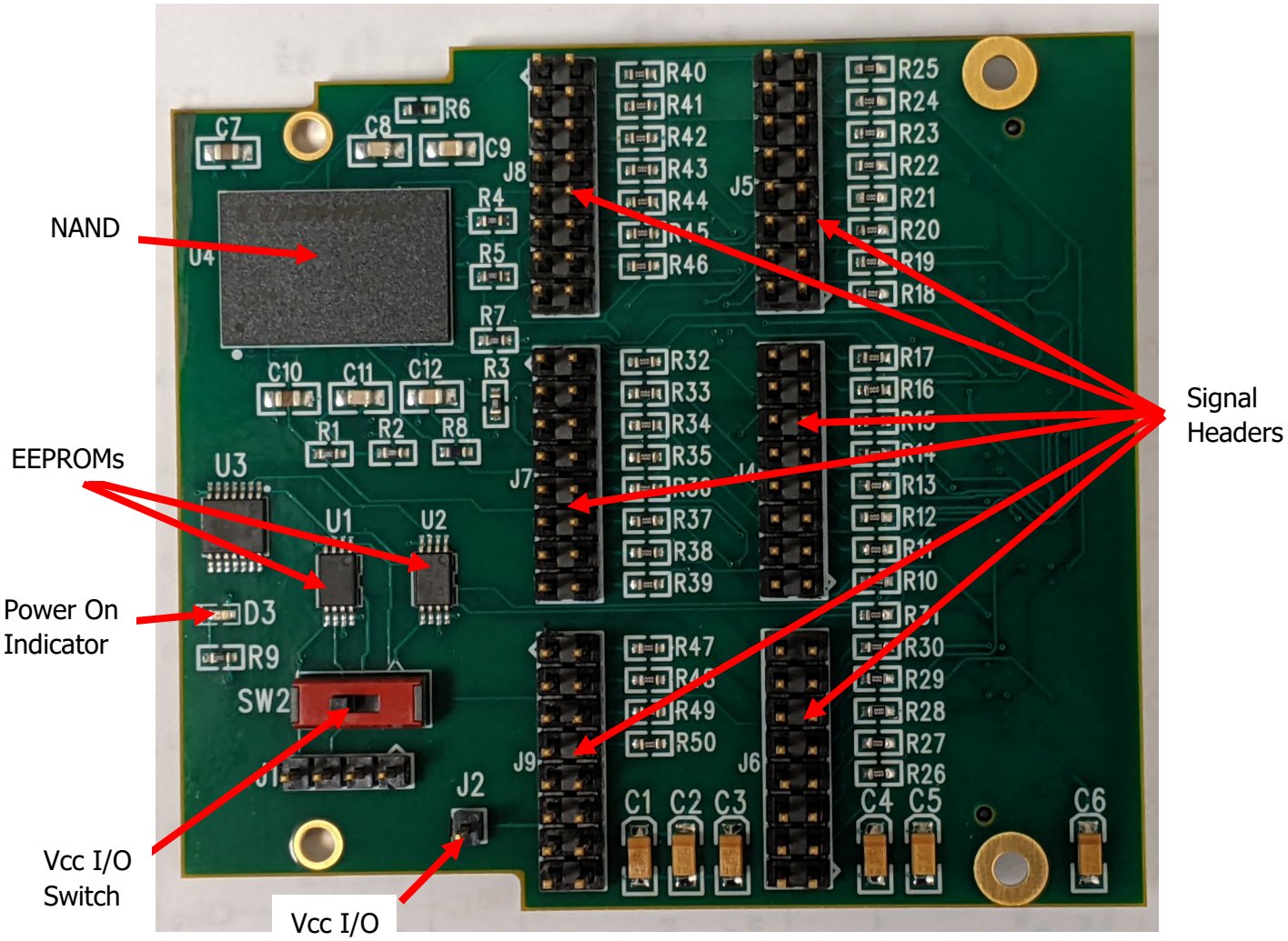


Figure 1: UT81NDQ512G8T Evaluation Board

1.1 Reference Documents

Description	Reference Document
UT81NDQ512G8T Data Sheet	https://caes.com/sites/default/files/documents/Datasheet-UT81NDQ512G8T.pdf
UT81NDQ512G8T User's Guide	Contact Factory for a copy
ONFi	http://www.onfi.org/specifications/
VITA 57	https://www.vita.com/Standards

2 Block Diagram Description and Picture



3 Jumper and Switch Setting Summary

Ref Des	Pin	Description
J1	1	Vcc core
	2	GND
	3	EEPROM SCL
	4	EEPROM SDA
J2	1	Vcc I/O
J4	2	DQ7_1
	4	DQ6_1
	6	DQ5_1
	8	DQ4_1
	10	DQ3_1
	12	DQ2_1
	14	DQ1_1
	16	DQ0_1
	Odd	GND
J5	2	RE_0#/RE_0_T
	4	RE_0_C
	6	ALE_1
	8	CLE_1
	10	WP_1#
	12	CE1_1#
	14	CE0_1#
	16	WE_1#
	Odd	GND
J6	2	RE_1#/RE_1_T
	4	RE_1_C
	6	R/B0_0#
	8	R/B1_0#
	10	R/B0_1#
	12	R/B1_1#
	14	N/C
	16	N/C
	Odd	GND
J7	2	DQ7_0
	4	DQ6_0
	6	DQ5_0
	8	DQ4_0
	10	DQ3_0

Ref Des	Pin	Description
	12	DQ2_0
	14	DQ1_0
	16	DQ0_0
	Odd	
J8	2	Vref
	4	ALE_0
	6	CLE_0
	8	WP_0#
	10	CE1_0#
	12	CE0_0#
	14	WE_0#
	16	N/C
	Odd	GND
J9	2	DQS_0/DQS_0_T
	4	DQS_0_C
	6	DQS_1/DQS_1_T
	8	DQS_1_C
	10	N/C
	12	N/C
	14	N/C
	16	SEFI_Flag (N/C for Rev 0)
	Odd	GND
SW2	Left	(Toward R9) 1.2V Vcc I/O
	Right	(Toward J9) 1.8V Vcc I/O

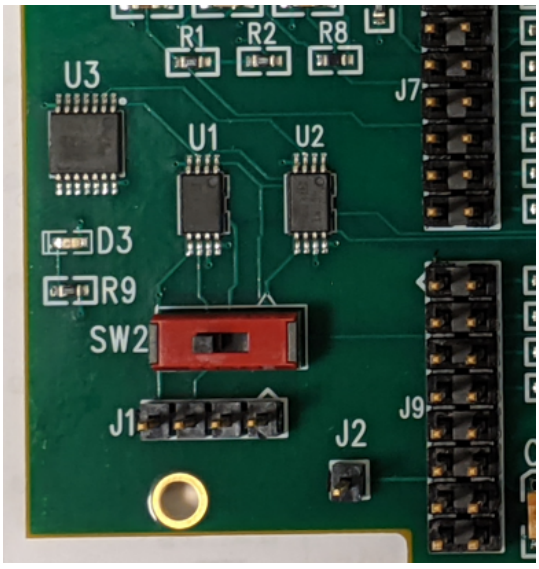


Figure 2: UT81NDQ512G8T Vcc I/O Switch

Note: Switch SW2 in Figure 2 ("left" position) sets Vcc I/O to 1.2 V. SW2 in the "right" position will set the Vcc I/O supply to 1.8 V.

4 Startup

The Vcc I/O switch needs to be in the correct position for the intended interface. If the user wants to use the NV-DDR3 interface, the switch must be in the 1.2V ("left") position. The part must be powered up with 1.2V applied to the I/O so that it is automatically configured for using the NV-DDR3 interface. If the part is powered with the 1.8V I/O configuration, then either the asynchronous or NV-DDR2 interface can be used. Asynchronous is the default interface for the 1.8V I/O voltage. During bootup, the FPGA board reads from the EEPROM the switch has selected. The FPGA board then configures the Vcc I/O level for the NAND.

Header pins J1 and J2 are available if supply lines need to be monitored. All power for the EVB will come from the FPGA board. No external power supplies are required.

1. If not monitoring R/B#, the host must wait at least 100µs after VCCQ reaches VCCQ (MIN) and VCC reaches VCC (MIN). If monitoring R/B#, the host must wait until R/B# is HIGH.
2. Each LUN draws less than an average of IST measured over intervals of 1ms until the RESET (FFh) command is issued.
3. The RESET (FFh) command must be the first command issued to all targets (CE#s) after the NAND Flash device is powered on. Each target will be busy for tPOR after a RESET command is issued. LUN0 of each target is selected by default after power-on.
4. The device is now initialized and ready for normal operation.

5 Configuration

After performing the steps above, the asynchronous interface is active for all targets on the device when the device powers on within the 1.8V VCCQ operational range. If the NAND Flash device powers on within the 1.2V VCCQ operational range, the NV-DDR3 interface is active.

Each target's interface is independent of other targets, so the host is responsible for changing the interface for each target.

Activating NV-DDR2 Interface

Prior to selecting the NV-DDR2 interface, it is recommended that settings for the NVDDR2 interface should be configured. Specifically:

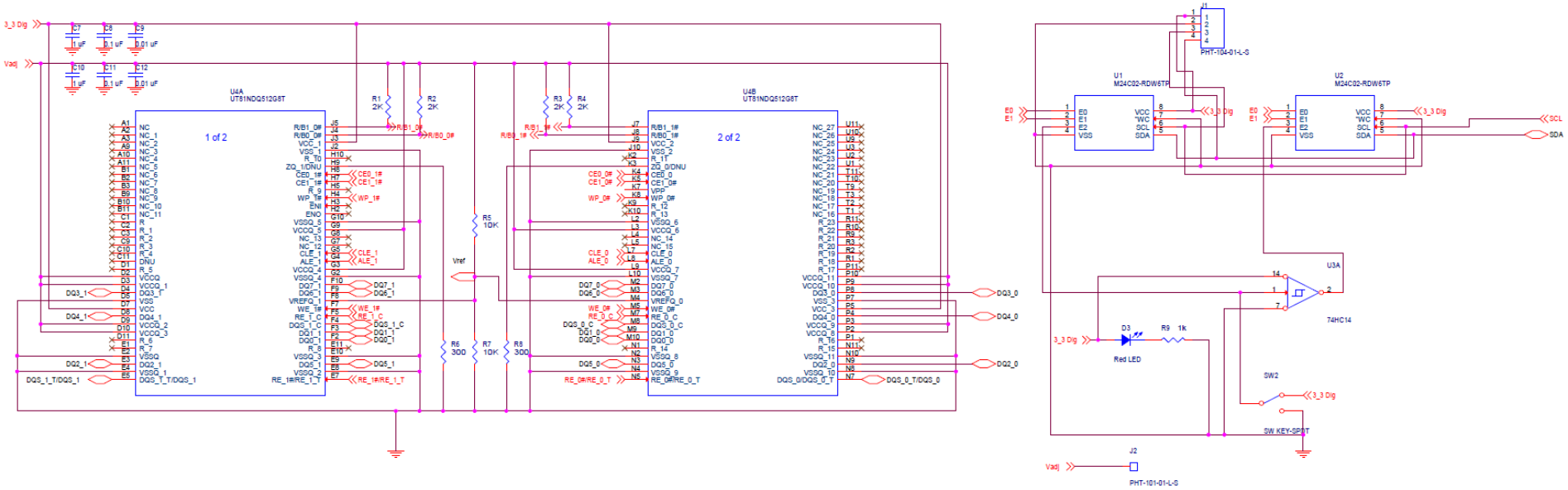
- SET FEATURES (EFh) command should be used to configure the NV-DDR2 configuration feature address.
- If on-die termination (ODT) is used, the appropriate ODT CONFIGURE (E2) commands should be issued.

These actions should be completed prior to selecting the NV-DDR2 interface. If these settings are modified when the NV-DDR2 interface is already selected, the host should take care to ensure appropriate settings are applied in a manner that avoids signal integrity issues.

To activate the NV-DDR2 NAND Flash interface, the following steps are repeated for each target:

1. Issue the SET FEATURES (EFh) command.
2. Write address 01h, which selects the timing mode feature address.
3. Write P1 with 2Xh, where X is the timing mode used in the NV-DDR2 interface (see Configuration Operations in the NAND user manual).
4. Write P2–P4 as 00h-00h-00h.

6 UT81NDQ512G8T-EVB Electrical Schematics



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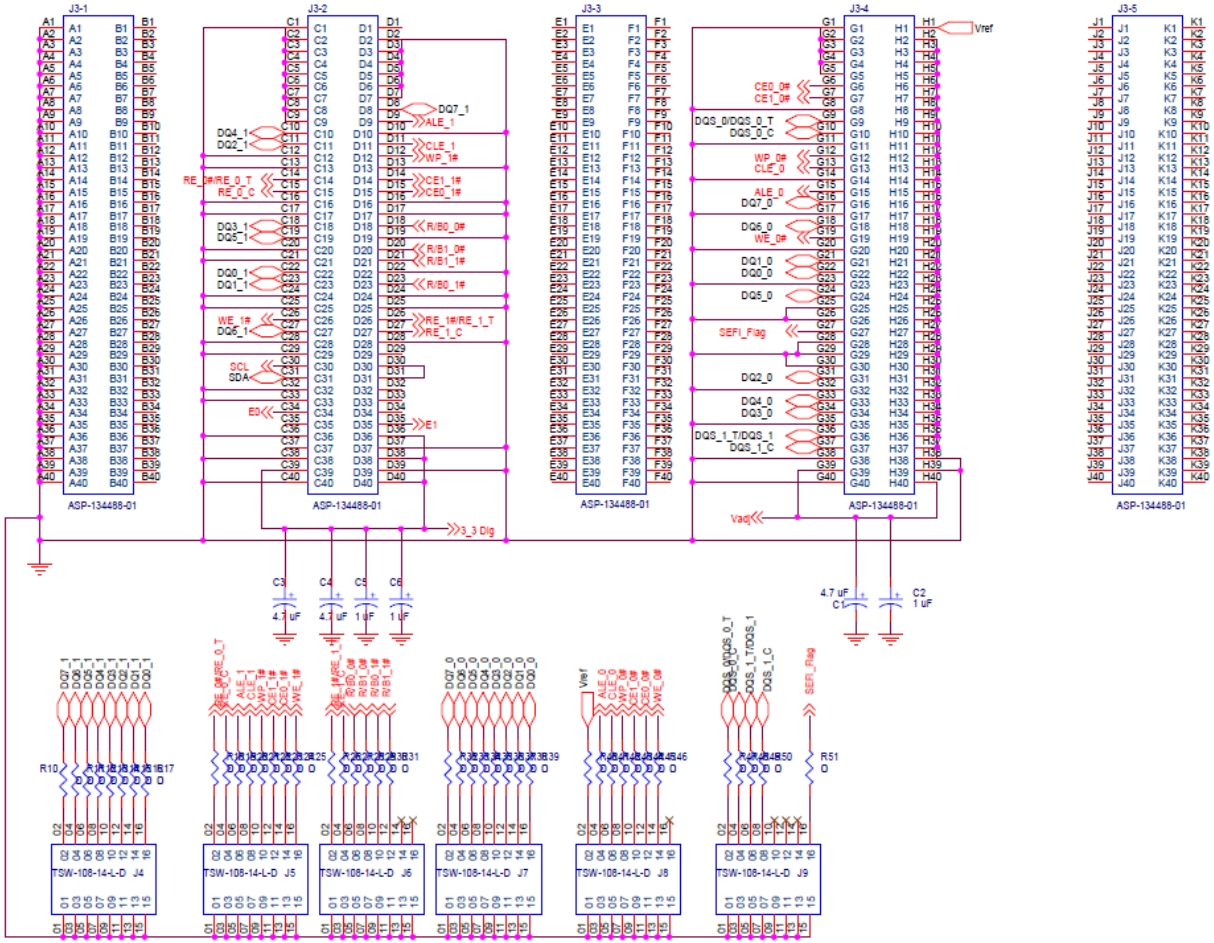

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RELEASED 3/22

Revision History

Date	Revision	Change Description
4/2022	0.0.1	Initial Release

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Datasheet Definitions

	DEFINITION
Advanced Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet **is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final**.
Preliminary Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

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