FRONTGRADE

DATASHEET

UT700

32-bit Fault-Tolerant SPARC™ V8/LEON 3FT Processor

4/16/2021

Version #:2.0.3

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Features

- Supports up to 166 MHz clock rate
- Separate instruction and data cache architecture
- High-performance fully pipelined IEEE-754 FPU
- Enhanced pipeline with 1.2 DMIPS / MHz performance
- Implemented on 130nm CMOS technology
- Internally configured clock network
- Power saving 1.2V core power supply
- 3.3V I/O compatibility
- Hardened-by-design flip-flops and memory cells
- Reed Solomon EDAC
- Multifunctional memory controller
- 10/100 Base-T Ethernet port for VxWorks development
- Integrated PCI 2.2 compatible core
- Four integrated multi-protocol SpaceWire nodes that support the RMAP protocol
- SPI interface
- Two CAN 2.0 compliant bus interfaces
- MIL-STD-1553 BC/RT/MT
- -55oC to +105oC temperature range
- Operational environment:
  - — Intrinsic total-dose: 100 krad (Si)
  - — SEL Immune≤110 MeV-cm^2/mg
- Packaging options:
  - — 484-pin Ceramic Land Grid, Column Grid and Ball Grid Array packages
- Standard Microcircuit Drawing 5962-13238:
  - — QML Q and V
- Applications:
  - — Nuclear power plant controls
  - — Critical transportation systems
  - — High-altitude avionics
  - — Medical electronics
  - — X-Ray cargo scanning
  - — Spaceborne computer
  - — System controller boards
  - — Avionics processing boards

Introduction

The UT700 features a seven-stage pipelined monolithic, high performance, fault-tolerant SPARCTM V8/LEON 3FT Processor. L1 cache consists of 16kB for both instruction and data caches. A Reed Solomon EDAC provides fault- tolerant protection for SDRAM. Integer performance is 1.2 DMIPS/MHz. RMAP protocol is supported for all four SpaceWire ports. The UT700 provides a 32-bit master/target PCI interface, including a 16-bit user I/O interface for off-chip peripherals. A compliant 2.0 AMBA bus interface integrates the on-chip LEON 3FT, SpaceWire, Ethernet, memory controller, cPCI, CAN bus, MIL-STD-1553, SPI and programmable interrupt peripherals.

The UT700 is SPARC V8 compliant; therefore, developers may use industry standard compilers, kernels, and development tools. A full software development suite is available including a C/C++ cross-compiler system based on GCC and the Newlib embedded C-library.

BCC includes a small run-time kernel with interrupt support and Pthreads library. For multi-threaded applications, a SPARCTM compliant port of the eCos real-time kernel, RTEMS 4.10, and VxWorks 6.x is supported.

The UT700 LEON 3FT processor is based upon the industry-standard SPARC V8 architecture. The system-on-chip incorporates the SPARC V8 core and the peripheral blocks indicated below. The core and peripherals communicate internally via the AMBA (Advanced Microcontroller Bus Architecture) interconnect. This bus is comprised of the AHB (Advanced High-speed Bus) which is used for high-speed data transfer, and the APB (Advanced Peripheral Bus) which is used for low-speed data transfer.

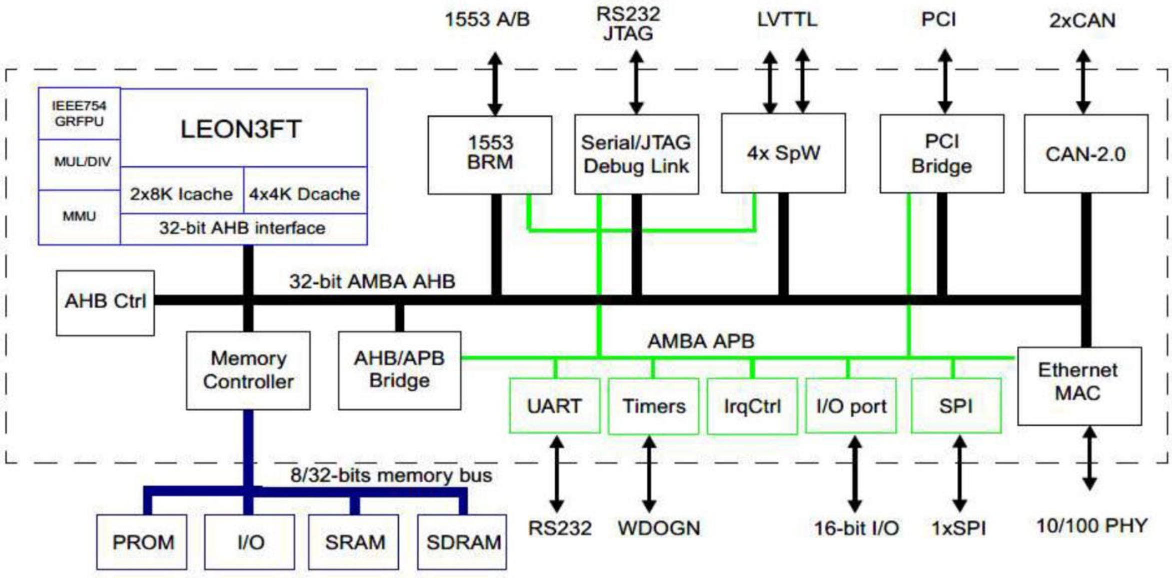

Figure 1:1: UT700 Functional Block Diagram

The LEON 3FT architecture includes the following peripheral blocks:

- LEON3 SPARC V8 integer unit with 16kB instruction cache and 16kB of data cache
- IEEE-754 floating point unit
- Debug support unit
- UART, JTAG, SpaceWire, PCI, and Ethernet debug links
- 8/16/32-bit memory controller with BCH EDAC for external PROM and SRAM
- 32-bit SDRAM controller with Reed Solomon EDAC for external SDRAM
- Timer unit with three 32-bit timers and watchdog
- Interrupt controller for 15 interrupts in two priority levels
- 16-bit general purpose I/O port (GPIO) which can be used as external interrupt sources
- Up to four SpaceWire links with RMAP on all channels
- MIL-STD-1553 interface supports BC/RT/MT
- Up to two CAN controllers
- Ethernet with support for MII
- cPCI interface with 8-channel arbiter
- Serial Peripheral Interface (SPI)

Pin Identification and Description

Pin Type

Abbreviation	Description
I	CMOS input
IS	CMOS input Schmitt
O	CMOS output
I/O	CMOS bi-direct
OD	CMOS open drain
PCI-I	PCI input
PCI-O	PCI output
PCI-I/O	PCI bi-direct
PCI-3	PCI three-state

System Signals

Number	Name	Type	Reset Value	Description
Y20	SYSCLK	I	—	Main system clock
E19	NODIV	I	—	Clock divider input. Set to ‘1’ for 1x memory clock, ‘0’ for 1/2x memory clock, relative to SYSCLK.
L19	$\overline{\text{RESET}}$	IS	—	System reset
K19	$\overline{\text{ERROR}}$[1]	OD	—	Processor error mode indicator. This is an active low output.
J19	$\overline{\text{WDOG}}$[1]	OD	—	Watchdog indicator. This is an active low output

Notes:

1. This pin is actively driven low and must be tied to V_{DD} through a pull-up resistor.

Address Bus

Number	Name	Type	Reset Value	Description
W5	ADDR[0]	O	low	Bit 0 of the address bus
Y5	ADDR[1]	O	low	Bit 1 of the address bus
W6	ADDR[2]	O	low	Bit 2 of the address bus
AA5	ADDR[3]	O	low	Bit 3 of the address bus
Y6	ADDR[4]	O	low	Bit 4 of the address bus
AB5	ADDR[5]	O	low	Bit 5 of the address bus
W7	ADDR[6]	O	low	Bit 6 of the address bus
AA6	ADDR[7]	O	low	Bit 7 of the address bus
Y7	ADDR[8]	O	low	Bit 8 of the address bus
AA7	ADDR[9]	O	low	Bit 9 of the address bus
AB6	ADDR[10]	O	low	Bit 10 of the address bus
W8	ADDR[11]	O	low	Bit 11 of the address bus
AB7	ADDR[12]	O	low	Bit 12 of the address bus
Y8	ADDR[13]	O	low	Bit 13 of the address bus
AA8	ADDR[14]	O	low	Bit 14 of the address bus
W9	ADDR[15]	O	low	Bit 15 of the address bus
AB8	ADDR[16]	O	low	Bit 16 of the address bus
Y9	ADDR[17]	O	low	Bit 17 of the address bus
W10	ADDR[18]	O	low	Bit 18 of the address bus
AB9	ADDR[19]	O	low	Bit 19 of the address bus
Y10	ADDR[20]	O	low	Bit 20 of the address bus
AA9	ADDR[21]	O	low	Bit 21 of the address bus
W11	ADDR[22]	O	low	Bit 22 of the address bus
AA10	ADDR[23]	O	low	Bit 23 of the address bus
Y11	ADDR[24]	O	low	Bit 24 of the address bus
AB10	ADDR[25]	O	low	Bit 25 of the address bus
AB11	ADDR[26]	O	low	Bit 26 of the address bus
AB11	ADDR[27]	O	low	Bit 27 of the address bus

Data Bus

Number	Name	Type	Reset Value	Description
W12	DATA[0]	I/O	high-z	Bit 0 of the data bus
W13	DATA[1]	I/O	high-z	Bit 1 of the data bus
Y12	DATA[2]	I/O	high-z	Bit 2 of the data bus
AA13	DATA[3]	I/O	high-z	Bit 3 of the data bus
AA12	DATA[4]	I/O	high-z	Bit 4 of the data bus
AB13	DATA[5]	I/O	high-z	Bit 5 of the data bus
W14	DATA[6]	I/O	high-z	Bit 6 of the data bus
AA14	DATA[7]	I/O	high-z	Bit 7 of the data bus
Y13	DATA[8]	I/O	high-z	Bit 8 of the data bus
W15	DATA[9]	I/O	high-z	Bit 9 of the data bus
AB15	DATA[10]	I/O	high-z	Bit 10 of the data bus
Y14	DATA[11]	I/O	high-z	Bit 11 of the data bus
AB14	DATA[12]	I/O	high-z	Bit 12 of the data bus
W16	DATA[13]	I/O	high-z	Bit 13 of the data bus
AA18	DATA[14]	I/O	high-z	Bit 14 of the data bus
Y15	DATA[15]	I/O	high-z	Bit 15 of the data bus
AB16	DATA[16]	I/O	high-z	Bit 16 of the data bus
AA15	DATA[17]	I/O	high-z	Bit 17 of the data bus
AB17	DATA[18]	I/O	high-z	Bit 18 of the data bus
AA16	DATA[19]	I/O	high-z	Bit 19 of the data bus
AA19	DATA[20]	I/O	high-z	Bit 20 of the data bus
W17	DATA[21]	I/O	high-z	Bit 21 of the data bus
AB18	DATA[22]	I/O	high-z	Bit 22 of the data bus
Y16	DATA[23]	I/O	high-z	Bit 23 of the data bus
Y17	DATA[24]	I/O	high-z	Bit 24 of the data bus
AA17	DATA[25]	I/O	high-z	Bit 25 of the data bus
W18	DATA[26]	I/O	high-z	Bit 26 of the data bus
AB19	DATA[27]	I/O	high-z	Bit 27 of the data bus
Y19	DATA[28]	I/O	high-z	Bit 28 of the data bus
AB20	DATA[29]	I/O	high-z	Bit 29 of the data bus
Y18	DATA[30]	I/O	high-z	Bit 30 of the data bus
AA20	DATA[31]	I/O	high-z	Bit 31 of the data bus

Check Bits

Number	Name	Type	Reset Value	Description
V19	CB[0]	I/O	high-z	Bit 0 of EDAC BCH/RS checkbits
AA21	CB[1]	I/O	high-z	Bit 1 of EDAC BCH/RS checkbits
Y21	CB[2]	I/O	high-z	Bit 2 of EDAC BCH/RS checkbits
W19	CB[3]	I/O	high-z	Bit 3 of EDAC BCH/RS checkbits
Y22	CB[4]	I/O	high-z	Bit 4 of EDAC BCH/RS checkbits
W20	CB[5]	I/O	high-z	Bit 5 of EDAC BCH/RS checkbits
W22	CB[6]	I/O	high-z	Bit 6 of EDAC BCH/RS checkbits
W21	CB[7]	I/O	high-z	Bit 7 of EDAC BCH/RS checkbits
V18	CB[8]	I/O	high	Bit 8 of EDAC RS checkbits
U18	CB[9]	I/O	high	Bit 9 of EDAC RS checkbits
T18	CB[10]	I/O	high	Bit 10 of EDAC RS checkbits
R18	CB[11]	I/O	high	Bit 11 of EDAC RS checkbits
P18	CB[12]	I/O	high	Bit 12 of EDAC RS checkbits
N18	CB[13]	I/O	high	Bit 13 of EDAC RS checkbits
M18	CB[14]	I/O	high	Bit 14 of EDAC RS checkbits
M19	CB[15]	I/O	high	Bit 15 of EDAC RS checkbits

Memory Control Signals

Number	Name	Type	Reset Value	Description
V21	$\overline{\text{WRITE}}$	O	high	PROM and I/O write enable strobe
U19	$\overline{\text{OE}}$	O	high	PROM and I/O output enable
T20	$\overline{\text{IOS}}$	O	high	I/O area chip select
V22	$\overline{\text{ROM[0]}}$	O	high	PROM chip select
U20	$\overline{\text{ROM[1]}}$	O	high	PROM chip select
U22	$\overline{\text{RWE[0]}}$	O	high	SRAM write enable strobe
T19	$\overline{\text{RWE[1]}}$	O	high	SRAM write enable strobe
T22	$\overline{\text{RWE[2]}}$	O	high	SRAM write enable strobe
T21	$\overline{\text{RWE[3]}}$	O	high	SRAM write enable strobe
V20	$\overline{\text{RAMOE[0]}}$	O	high	SRAM output enable
R21	$\overline{\text{RAMOE[1]}}$	O	high	SRAM output enable
R20	$\overline{\text{RAMOE[2]}}$	O	high	SRAM output enable
R22	$\overline{\text{RAMOE[3]}}$	O	high	SRAM output enable
R19	$\overline{\text{RAMOE[4]}}$	O	high	SRAM output enable
P22	$\overline{\text{RAMS[0]}}$	O	high	SRAM chip select
P20	$\overline{\text{RAMS[1]}}$	O	high	SRAM chip select
P21	$\overline{\text{RAMS[2]}}$	O	high	SRAM chip select
P19	$\overline{\text{RAMS[3]}}$	O	high	SRAM chip select
N19	$\overline{\text{RAMS[4]}}$	O	high	SRAM chip select
K20	READ	O	high	SRAM, PROM, and I/O read indicator
K22	$\overline{\text{BEXC}}$	I	—	Bus exception
K21	$\overline{\text{BRDY}}$	I	—	Bus ready

SDRAM

Number	Name	Type	Reset Value	Description
AB12	SDCLK	O	high	SDRAM clock
N22	$\overline{\text{SDRAS}}$	O	high	SDRAM row address strobe
N20	$\overline{\text{SDCAS}}$	O	high	SDRAM column address strobe
N21	$\overline{\text{SDWE}}$	O	high	SDRAM write enable
M21	$\overline{\text{SDCS[0]}}$	O	high	SDRAM chip select
M22	$\overline{\text{SDCS[1]}}$	O	high	SDRAM chip select
L21	SDDQM[0]	O	high	SDRAM data mask
M20	SDDQM[1]	O	high	SDRAM data mask
L20	SDDQM[2]	O	high	SDRAM data mask
L22	SDDQM[3]	O	high	SDRAM data mask

CAN 2.0 Interface

Number	Name	Type	Reset Value	Description
J20	CAN_RXD [0]	I	—	CAN receive data
J22	CAN_TXD [0]	O	high	CAN transmit data
J21	CAN_RXD [1]	I	—	CAN receive data
H22	CAN_TXD [1]	O	high	CAN transmit data

Debug Support Unit (DSU)

Number	Name	Type	Reset Value	Description
H19	DSUACT	O	low	DSU mode indicator
H20	DSUBRE	I	—	DSU break
G19	DSUEN	I	—	DSU enable
G20	DSURX	I	—	DSU UART receive data
G21	DSUTX	O	high	DSU UART transmit data

JTAG Interface

Number	Name	Type	Reset Value	Description
F20	$\overline{\text{TRST}}$	I	—	JTAG reset
F21	$\overline{\text{TMS}}$	I	—	JTAG test mode select
G22	TCK	I	—	JTAG clock
F22	TDI	I	—	JTAG test data input
F19	TDO	O	—	JTAG test data output

Ethernet Interface

Number	Name	Type	Reset Value	Description
E22	EMDC	O	low	Ethernet media interface clock
D22	ERX_CLK	I	—	Ethernet RX clock
D20	EMDIO	I/O	high-z	Ethernet media interface data
E21	ERX_COL	I	—	Ethernet collision error
E20	ERX_CRS	I	—	Ethernet carrier sense detect
D21	ERX_DV	I	—	Ethernet receiver data valid
C21	ERX_ER	I	—	Ethernet reception error
C22	ERXD [0]	I	—	Ethernet receive data
B21	ERXD [1]	I	—	Ethernet receive data
C20	ERXD [2]	I	—	Ethernet receive data
B20	ERXD [3]	I	—	Ethernet receive data
C19	ETXD [0]	O	low	Ethernet transmit data
C18	ETXD [1]	O	high	Ethernet transmit data
B18	ETXD [2]	O	low	Ethernet transmit data
B19	ETXD [3]	O	high	Ethernet transmit data

Number	Name	Type	Reset Value	Description
A19	ETX_CLK	I	—	Ethernet TX clock
A18	ETX_EN	O	low	Ethernet transmit enable
A20	ETX_ER	O	low	Ethernet transmit error. Always driven low
E17	EDCLDIS	I	—	Ethernet EDCL disable
E18	$\overline{\text{EMDINT}}$	I	—	Ethernet management interface data interrupt

Note:

1. Ethernet interface operation is intended for terrestrial use only, not guaranteed in radiation environments.

General Purpose I/O

Number	Name	Type	Reset Value	Description
B17	GPIO[0]	I/O	high-z	Bit 0 of general purpose I/O
C17	GPIO[1]	I/O	high-z	Bit 1 of general purpose I/O
A17	GPIO[2]	I/O	high-z	Bit 2 of general purpose I/O
D17	GPIO[3]	I/O	high-z	Bit 3 of general purpose I/O
C16	GPIO[4]	I/O	high-z	Bit 4 of general purpose I/O
D16	GPIO[5]	I/O	high-z	Bit 5 of general purpose I/O
C15	GPIO[6]	I/O	high-z	Bit 6 of general purpose I/O
D15	GPIO[7]	I/O	high-z	Bit 7 of general purpose I/O
C7	GPIO[8]	I/O	high-z	Bit 8 of general purpose I/O
B5	GPIO[9]	I/O	high-z	Bit 9 of general purpose I/O
D7	GPIO[10]	I/O	high-z	Bit 10 of general purpose I/O
A5	GPIO[11]	I/O	high-z	Bit 11 of general purpose I/O
D6	GPIO[12]	I/O	high-z	Bit 12 of general purpose I/O
C5	GPIO[13]	I/O	high-z	Bit 13 of general purpose I/O
C6	GPIO[14]	I/O	high-z	Bit 14 of general purpose I/O
D5	GPIO[15]	I/O	high-z	Bit 15 of general purpose I/O

SpaceWire Interface

Number	Name	Type	Reset Value	Description
A11	SPW_CLK	I	—	SpaceWire clock
A16	SPW_RXS[0]	I	—	SpaceWire receive strobe
A15	SPW_RXD[0]	I	—	SpaceWire receive data
B16	SPW_TXS[0]	O	low	SpaceWire transmit strobe
B15	SPW_TXD[0]	O	low	SpaceWire transmit data
A14	SPW_RXS[1]	I	—	SpaceWire receive strobe
A13	SPW_RXD[1]	I	—	SpaceWire receive data
B14	SPW_TXS[1]	O	low	SpaceWire transmit strobe
B13	SPW_TXD[1]	O	low	SpaceWire transmit data
A9	SPW_RXS[2]	I	—	SpaceWire receive strobe
A8	SPW_RXD[2]	I	—	SpaceWire receive data
B9	SPW_TXS[2]	O	low	SpaceWire transmit strobe
B8	SPW_TXD[2]	O	low	SpaceWire transmit data
A7	SPW_RXS[3]	I	—	SpaceWire receive strobe
A6	SPW_RXD[3]	I	—	SpaceWire receive data
B7	SPW_TXS[3]	O	low	SpaceWire transmit strobe
B6	SPW_TXD[3]	O	low	SpaceWire transmit data

UART Interface

Number	Name	Type	Reset Value	Description
C12	RXD	I	—	UART receive data
C11	TXD	O	high	UART transmit data

PCI Address Data Bus

Number	Name	Type	Reset Value	Description
AA2	PCI_AD[0]	PCI-I/O	high-z	Bit 0 of PCI address and data bus
AA3	PCI_AD[1]	PCI-I/O	high-z	Bit 1 of PCI address and data bus
Y1	PCI_AD[2]	PCI-I/O	high-z	Bit 2 of PCI address and data bus
Y2	PCI_AD[3]	PCI-I/O	high-z	Bit 3 of PCI address and data bus
Y3	PCI_AD[4]	PCI-I/O	high-z	Bit 4 of PCI address and data bus
W1	PCI_AD[5]	PCI-I/O	high-z	Bit 5 of PCI address and data bus
W2	PCI_AD[6]	PCI-I/O	high-z	Bit 6 of PCI address and data bus
W3	PCI_AD[7]	PCI-I/O	high-z	Bit 7 of PCI address and data bus
V2	PCI_AD[8]	PCI-I/O	high-z	Bit 8 of PCI address and data bus
V3	PCI_AD[9]	PCI-I/O	high-z	Bit 9 of PCI address and data bus
U1	PCI_AD[10]	PCI-I/O	high-z	Bit 10 of PCI address and data bus
U2	PCI_AD[11]	PCI-I/O	high-z	Bit 11 of PCI address and data bus
U3	PCI_AD[12]	PCI-I/O	high-z	Bit 12 of PCI address and data bus
T1	PCI_AD[13]	PCI-I/O	high-z	Bit 13 of PCI address and data bus
R2	PCI_AD[14]	PCI-I/O	high-z	Bit 14 of PCI address and data bus
R1	PCI_AD[15]	PCI-I/O	high-z	Bit 15 of PCI address and data bus
J1	PCI_AD[16]	PCI-I/O	high-z	Bit 16 of PCI address and data bus
K2	PCI_AD[17]	PCI-I/O	high-z	Bit 17 of PCI address and data bus
K1	PCI_AD[18]	PCI-I/O	high-z	Bit 18 of PCI address and data bus
G1	PCI_AD[19]	PCI-I/O	high-z	Bit 19 of PCI address and data bus
H3	PCI_AD[20]	PCI-I/O	high-z	Bit 20 of PCI address and data bus
H2	PCI_AD[21]	PCI-I/O	high-z	Bit 21 of PCI address and data bus
F1	PCI_AD[22]	PCI-I/O	high-z	Bit 22 of PCI address and data bus
F2	PCI_AD[23]	PCI-I/O	high-z	Bit 23 of PCI address and data bus
E1	PCI_AD[24]	PCI-I/O	high-z	Bit 24 of PCI address and data bus
E2	PCI_AD[25]	PCI-I/O	high-z	Bit 25 of PCI address and data bus
F3	PCI_AD[26]	PCI-I/O	high-z	Bit 26 of PCI address and data bus
D1	PCI_AD[27]	PCI-I/O	high-z	Bit 27 of PCI address and data bus
D2	PCI_AD[28]	PCI-I/O	high-z	Bit 28 of PCI address and data bus
E3	PCI_AD[29]	PCI-I/O	high-z	Bit 29 of PCI address and data bus
D3	PCI_AD[30]	PCI-I/O	high-z	Bit 30 of PCI address and data bus
C1	PCI_AD[31]	PCI-I/O	high-z	Bit 31 of PCI address and data bus

PCI Control Signals

Number	Name	Type	Reset Value	Description
C3	$\overline{\text{PCI\_RST}}$	PCI-I	—	PCI reset input
C2	PCI_CLK	PCI-I	—	PCI clock input
V1	PCI_C/$\overline{\text{BE}}$ [0]	PCI-I/O	high-z	PCI bus command and byte enable
P2	PCI_C/$\overline{\text{BE}}$ [1]	PCI-I/O	high-z	PCI bus command and byte enable
H1	PCI_C/$\overline{\text{BE}}$ [2]	PCI-I/O	high-z	PCI bus command and byte enable
G2	PCI_C/$\overline{\text{BE}}$ [3]	PCI-I/O	high-z	PCI bus command and byte enable
P1	PCI_PAR	PCI-I/O	high-z	PCI parity checkbit
L1	$\overline{\text{PCI\_FRAME}}$[1]	PCI-3	high-z	PCI cycle frame indicator
L2	$\overline{\text{PCI\_IRDY}}$[1]	PCI-3	high-z	PCI initiator ready indicator
M1	$\overline{\text{PCI\_TRDY}}$[1]	PCI-3	high-z	PCI target ready indicator
N1	$\overline{\text{PCI\_STOP}}$[1]	PCI-3	high-z	PCI target stop request
M2	$\overline{\text{PCI\_DEVSEL}}$[1]	PCI-3	high-z	PCI device select
N2	$\overline{\text{PCI\_PERR}}$[1]	PCI-3	high-z	PCI parity error indicator
G3	PCI_IDSEL	PCI-3	high-z	PCI initialization device select
A4	$\overline{\text{PCI\_REQ}}$	PCI-3	high-z	PCI request to arbiter in point to point configuration
B2	$\overline{\text{PCI\_GNT}}$	PCI-I	—	PCI bus access indicator in point to point configuration
AB3	$\overline{\text{PCI\_HOST}}$	PCI-I	—	PCI host enable input (Connect to $\overline{\text{SYSEN}}$ PCI bus)

Note:

1. This pin must be tied to V_{DD} through a pull-up resistor as specified in the PCI Local Bus Specification Revision 2.1 Section 4.3.3.

PCI Arbiter

Number	Name	Type	Reset Value	Description
B4	$\overline{\text{PCI\_ARB\_REQ}}$ [0]	PCI-I	—	PCI arbiter bus request
AB4	$\overline{\text{PCI\_ARB\_REQ}}$ [1]	PCI-I	—	PCI arbiter bus request
Y4	$\overline{\text{PCI\_ARB\_REQ}}$ [2]	PCI-I	—	PCI arbiter bus request
T3	$\overline{\text{PCI\_ARB\_REQ}}$ [3]	PCI-I	—	PCI arbiter bus request
P3	$\overline{\text{PCI\_ARB\_REQ}}$ [4]	PCI-I	—	PCI arbiter bus request
M3	$\overline{\text{PCI\_ARB\_REQ}}$ [5]	PCI-I	—	PCI arbiter bus request
K3	$\overline{\text{PCI\_ARB\_REQ}}$ [6]	PCI-I	—	PCI arbiter bus request
C4	$\overline{\text{PCI\_ARB\_REQ}}$ [7]	PCI-I	—	PCI arbiter bus request
B3	$\overline{\text{PCI\_ARB\_GNT}}$ [0]	PCI-O	high-z	PCI arbiter bus grant
AA4	$\overline{\text{PCI\_ARB\_GNT}}$ [1]	PCI-O	high-z	PCI arbiter bus grant
W4	$\overline{\text{PCI\_ARB\_GNT}}$ [2]	PCI-O	high-z	PCI arbiter bus grant
R3	$\overline{\text{PCI\_ARB\_GNT}}$ [3]	PCI-O	high-z	PCI arbiter bus grant
N3	$\overline{\text{PCI\_ARB\_GNT}}$ [4]	PCI-O	high-z	PCI arbiter bus grant
L3	$\overline{\text{PCI\_ARB\_GNT}}$ [5]	PCI-O	high-z	PCI arbiter bus grant
J3	$\overline{\text{PCI\_ARB\_GNT}}$ [6]	PCI-O	high-z	PCI arbiter bus grant
A3	$\overline{\text{PCI\_ARB\_GNT}}$ [7]	PCI-O	high-z	PCI arbiter bus grant

Serial Peripheral Interface (SPI)

Number	Name	Type	Reset Value	Description
E12	SPICLK	O	—	SPI Clock
E13	SPIMOSI	O	—	SPI Master Out Slave In
E11	SPIMISO	I	—	SPI Master In Slave Out
E10	SPISLVSEL	O	—	SPI Select

MIL-STD-1553 Signals

Number	Name	Type	Reset Value	Description
B11	1553CLK	I	—	MIL-STD-1553B Clock
C13	1553RXA	I	—	MIL-STD-1553B Receive Positive A
D12	$\overline{\text{1553RXA}}$	I	—	MIL-STD-1553B Receive Negative A
C8	1553RXB	I	—	MIL-STD-1553B Receive Positive B
C9	$\overline{\text{1553RXB}}$	I	—	MIL-STD-1553B Receive Negative B
D11	1553RXENA	O	—	MIL-STD-1553B Receive Enable A
D9	1553RXENB	O	—	MIL-STD-1553B Receive Enable B
D13	1553TXINHA	O	high	MIL-STD-1553B Transmit Inhibit A
D10	1553TXINHB	O	high	MIL-STD-1553B Transmit Inhibit B
D14	1553TXA	O	—	MIL-STD-1553B Transmit Positive A Synchronously reset to zero with 1553CLK
C14	$\overline{\text{1553TXA}}$	O	—	MIL-STD-1553B Transmit Negative A Synchronously reset to zero with 1553CLK
B10	1553TXB	O	—	MIL-STD-1553B Transmit Positive B Synchronously reset to zero with 1553CLK
C10	$\overline{\text{1553TXB}}$	O	—	MIL-STD-1553B Transmit Negative B Synchronously reset to zero with 1553CLK

Note:

1. Refer to the Problem Advisory, SPO-2021-PA-0003, or the GIDEP, GB4-P-21-03, for 1553 peripheral transmission glitches on power-up sequence.

Power and Ground Pins

Number	Name	Description
B1, B12, B22, E7, E9, E14, E16, F6, F10, F13, F17, G5, G9, G14, H6, H8, H10, H13, H15, J7, J16, K5, K8, K15, K17, L6, M6, N5, N8, N15, N17, P7, P16, R6, R8, R10, R13, R15, T5, T9, T14, U6, U9, U11, U12, U14, U17, V10, V13, AA1, AA22	V_{DD}	I/O supply voltage
A1, A12, A22, E6, F4, G4, G8, G11, G12, G15, G17, H4, H7, H16, H18, J2, J4, J9, J14, K4, K10, K13, L7, L11, L12, L17, M7, M11, M12, M17, N4, N10, N13, P4, P9, P14, R4, R7, R16, T2, T4, T8, T15, T17, U4, U10, U13, V4, V5, V8, V11, V12, V15, AB1, AB22	V_{SS}	I/O supply ground
A2, A21, E5, F8, F15, G7, G10, G13, G16, G18, H5, H9, H11, H12, H14, H17, J6, J8, J15, K7, K16, L8, L15, L18, M4, M8, M15, N7, N16, P6, P8, P15, R5, R9, R11, R12, R14, R17, T7, T10, T13, T16, U8, U15, V6, V17, AB2, AB21	V_{DDC}	Core supply voltage
A10, E8, E15, F5, F7, F9, F11, F12, F14, F16, F18, G6, H21, J5, J10, J11, J12, J13, J17, K6, K9, K11, K12, K14, K18, L5, L9, L10, L13, L14, L16, M5, M9, M10, M13, M14, M16, N6,	V_{SSC}	Core supply ground
N9, N11, N12, N14, P5, P10, P11, P12, P13, P17, T6, T11, T12, U5, U7, U16, U21, V7, V14, V16		
D4, D18, E4, J18, L4, V9	N/C	No connect. These pins may be left floating, or tied to V_{DD} or V_{SS}
D8	Unused	This pin may be left floating or tied to V_{SS}
D19	Unused	This pin must be tied to V_{SS}

Bootstrap Signals

The states of the following signals are latched in upon the rising edge of reset in order to configure the UT 700 for the indicated operation

Name	Function
GPIO[1:0]	Sets the data width of the PROM area 00: 8 bits 01: 16 bits 10: 32 bits 11: Not used
GPIO[2]	Enable EDAC checking of the PROM area 0: EDAC disabled 1: EDAC enabled
GPIO[7:4]	Set the SpW clock divisor link bits in the SpW Clock Divisor Register
GPIO[15:12]	Sets the least significant address nibble of the IP and MAC address for the Ethernet Debug Communication Link (EDCL)

AC and DC Electrical Specifications

Absolute Maximum Ratings[1]

Symbol	Description	Package	MIN	MAX	Units
V_{DDC}	Core supply voltage		-0.3	1.85	V
V_{DD}	I/O supply voltage		-0.3	5.2	V
V_{IN}	Input voltage any pin		V_{SS} - 0.3	V_{DD} + 0.3	V
P_D[2]	Maximum power dissipation permitted @ T_C = 105°C		—	4	W
T_J	Junction temperature		—	150	°C
θ_{JC}	Thermal resistance, junction to case	484 CLGA/CCGA/CBGA	—	5	°C/W
T_{STG}	Storage temperature		-65	150	°C
ESD_{HBM}	ESD protection (human body model) Class 2		2000	—	V

Notes:

1. Stresses greater than those listed in the following table can result in permanent damage to the device. These parameters cannot be violated.
2. Per MIL-STD-883, Method 1012, Section 3.4.1, $P_D = (T_J\ (max) - T_C\ (max)) / \theta_{JC}$

Recommended Operating Conditions

(V_{DD}=3.3V±0.3V; V_{DDC}=1.2V±0.1V; T_C=-55°C to 105°C)

Symbol	Description	MIN	MAX	Units
V_{DDC}	Core supply voltage	1.1	1.3	V
V_{DD}	I/O supply voltage	3.0	3.6	V
V_{IN}	Input voltage any pin	0	V_{DD}	V
T_C	Case operating temperature	-55	105	°C
t_R	Rise time, all CMOS and PCI inputs (0.1 V_{DD} to 0.9 V_{DD})	—	20	ns
t_F	Fall time, all CMOS and PCI inputs (0.9 V_{DD} to 0.1 V_{DD})	—	20	ns

Operating Environment

The UT700 processor includes the following SEU mitigation features:

- Cache memory error-detecting of up to 4 errors per tag or 32-bit word
- Autonomous and software transparent error handling
- No timing impact due to error detection or correction

Parameter	Limit	Units
Total Ionizing Dose (TID) [1]	1E5	rad (Si)
Single Event Latchup Immune (SEL) [2]	110	MeV-cm^2/mg
Single Event Upset (SEU) [3, 4]	5.2E-7	errors/device-day
Single Event Upset (SEU) [3, 4] Multiple-bit error (MBE) rate which over comes internal error detection and correction architecture	2.80E-11	MBE/device-day

Notes:

1. TID irradiation per MIL-STD-883, Test Method 1019, condition A. Post irradiation electrical testing performed at room temperature.
2. Worst case temperature of T_C = +105°C, V_{DD} = 3.6V, V_{DD} = 1.3V
3. Contact factory for additional information regarding the determination of the inherent and multiple-bit upset rates.
4. The error rate calculation was performed using SpaceRad 6.0 for a Geosynchronous orbit in the Adams 90% worst -case environment with 100mil Al shielding.

Power Supply Operating Characteristics (pre- and post-radiation)

(V_{DD} = 3.3V±0.3V; V_{DDC} =1.2V±0.1V; T_C = -55°C to 105°C)

Symbol	Description	Conditions		MIN	MAX	Units
I_{DDCS}	Standby core power supply quiescent current	V_{DDC} = 1.3V, V_{DD}= 3.6V All clock inputs at 0MHz	T_C =-55°C and 25°C	—	8	mA
			T_C =105°C	—	100	
		RHA:R	T_C =25°C	—	50	
I_{DDS}	Standby I/O power supply quiescent current	V_{DDC} = 1.3V, V_{DD} = 3.6V All clock inputs at 0MHz	T_C =-55°C and 25°C	—	0.7	mA
			T_C =105°C	—	2	

DC Characteristics for LVCMOS3 Inputs (pre- and post-radiation)

(V_{DD} = 3.3V±0.3V; V_{DDC} = 1.2V±0.1V; T_C = -55°C to 105°C)

Symbol	Description	Conditions	MIN	MAX	Units
V_{IH}[1]	High-level input voltage		0.7V_{DD}	—	V
V_{IL}[1]	Low-level input voltage		—	0.3V_{DD}	V
V_{T}^{+}	Positive going threshold voltage for Schmitt inputs		—	0.7V_{DD}	V
V_{T}^{-}	Negative going threshold voltage for Schmitt inputs		0.3V_{DD}	—	V
V_H	Hysteresis voltage for Schmitt inputs		0.4	—	V
I_{IN}	Input leakage current (All inputs except pull-ups and pull-downs)	$V_{IN} = V_{DD}$	—	-1	µA
		$V_{IN} = V_{SS}$	-1	—	
I_{IN}	Input leakage current for pins with internal pull-up resistors (CB[15:8], $\overline{\text{EMDINT}}$, and NODIV)	$V_{IN} = V_{DD}$	-10	10	µA
		$V_{IN} = V_{SS}$	-100	-10	
I_{IN}	Input leakage current for pins with internal pull-down resistors (EDCLDIS, SPIMISO, 1553CLK, 1553RXA, 1553RXA, 1553RXB, and $\overline{\text{1553RXB}}$)	$V_{IN} = V_{DD}$	+10	+150	µA
		$V_{IN} = V_{SS}$	-10	10	
C_{IN}[2]	Input pin capacitance	ƒ = 1MHz; V_{DD} = 0V, V_{DDC} = 0V	—	16	pF

Notes:

1. JTAG inputs are not tested.
2. Capacitance is measured for initial qualification and when design changes might affect the input/output capacitance.

DC Characteristics for LVCMOS3 Outputs (pre- and post-radiation)

(V_{DD} = 3.3V±0.3V; V_{DDC} = 1.2V±0.1V; T_C=-55°C to 105°C)

Symbol	Description	Conditions	MIN	MAX	Units
V_{OL1}[1]	Low-level output voltage (All outputs except those listed below and in Section 3.8)	I_{OL} = 100 µA	—	0.25	V
		I_{OL} = 4mA	—	0.4	
V_{OHI}[1, 2]	High-level output voltage (All outputs except those listed below and in Section 3.8)	I_{OH} = -100 µA	V_{DD}-0.25	—	V
		I_{OH} = -4mA	2.4	—	
V_{OL}[2]	Low-level output voltage (GPIO[15:0], SPW_TXD[3:0], SPW_TXS[3:0], TXD)	I_{OL} = 100 µA	—	0.25	V
		I_{OL} = 12mA	—	0.4	
V_{OH}[2]	High-level output voltage (GPIO[15:0], SPW_TXD[3:0], SPW_TXS[3:0], TXD)	I_{OH} = -100 µA	V_{DD}-0.25	—	V
		I_{OH} = -12mA	2.4	—	
V_{OL}[3]	Low-level output voltage ($\overline{\text{WRITE}}$, $\overline{\text{OE}}$, $\overline{\text{IOS}}$, $\overline{\text{ROM[1:0]}}$, $\overline{\text{RWE[3:0]}}$, $\overline{\text{RAMOE[4:0]}}$, $\overline{\text{RAMS[4:0]}}$, $\overline{\text{SDCS[1:0]}}$, $\overline{\text{SDRAS}}$, $\overline{\text{SDCAS}}$, $\overline{\text{SDWE}}$, $\overline{\text{SDCLK}}$, $\overline{\text{READ}}$, $\overline{\text{SDDQM[3:0]}}$, $\overline{\text{ADDR[27:0]}}$, $\overline{\text{DATA[31:0]}}$ and $\overline{\text{CB[15:0]}}$)	I_{OL} = 100 µA	—	0.25	V
		I_{OL} = 24mA	—	0.4	
V_{OH}[3]	High-level output voltage ($\overline{\text{WRITE}}$, $\overline{\text{OE}}$, $\overline{\text{IOS}}$, $\overline{\text{ROM[1:0]}}$, $\overline{\text{RWE[3:0]}}$, $\overline{\text{RAMOE[4:0]}}$, $\overline{\text{RAMS[4:0]}}$, $\overline{\text{SDCS[1:0]}}$, $\overline{\text{SDRAS}}$, $\overline{\text{SDCAS}}$, $\overline{\text{SDWE}}$, $\overline{\text{SDCLK}}$, $\overline{\text{READ}}$, $\overline{\text{SDDQM[3:0]}}$, $\overline{\text{ADDR[27:0]}}$, $\overline{\text{DATA[31:0]}}$ and $\overline{\text{CB[15:0]}}$)	I_{OH} = -100 µA	V_{DD}-0.25	—	V
		I_{OH} = -24mA	2.4	—	
V_{OL}[4]	Low-level output voltage (SPICLK, SPIMOSI, SPISLVSEL)	I_{OL} = 100 µA	—	0.25	V
		I_{OL} = 8mA	—	0.4	
V_{OH}[4]	High-level output voltage (SPICLK, SPIMOSI, SPISLVSEL)	I_{OH} = -100 µA	V_{DD}-0.25	—	V
		I_{OH} = -8mA	2.4	—	
I_{OZ}	Three-state output current	$V_O = V_{DD}$	-10	10	µA
		$V_O = V_{SS}$	-10	10	
I_{OS}[3]	Short-circuit output current (All outputs except PCI outputs)	$V_O = V_{DD}$; V_{DD} = 3.6V	—	130	mA
		V_O = VSS; V_{DD} = 3.6V	-65	—	
C_{OUT}[4]	Output pin capacitance	ƒ = 1MHz; V_{DD} = 0V V_{DDC} = 0V	—	16	pF

Notes:

1. JTAG outputs are not tested
2. Except open-drain output
3. Guaranteed by design
4. Capacitance is measured for initial qualification and when design changes might affect the input/output capacitance

AC Characteristics for LVCMOS3 Inputs and Outputs (pre- and post-radiation)

(V_{DD}=3.3V±0.3V; V_{DDC} =1.2V±0.1V; T_C=-55°C to 105°C)

Symbol	Description	Conditions	MIN	MAX	Units
f_{CLK}	System clock frequency		—	166	MHz
t_{HIGH}	System clock high time		2.4	—	ns
t_{LOW}	System clock low time		2.4	—	ns
t_{DSD} 1	System clock to SDRAM clock propagation delay		2.0	6.0	ns

Note:

1. Reference Figure 4:14 for test load

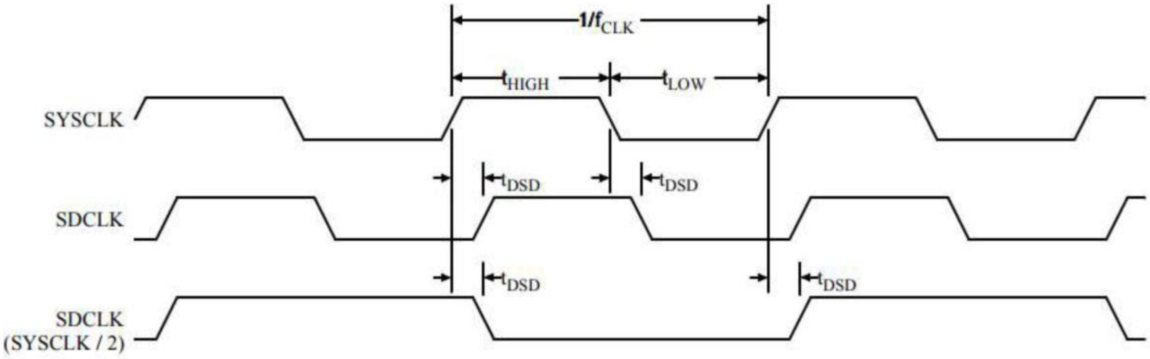

Figure 3:1: System Clock and SDCLK Timing Diagram

DC Electrical Characteristics for PCI Inputs (pre- and post-radiation)

(V_{DD} = 3.3V±0.3V; V_{DDC} = 1.2V±0.1V; T_C = -55°C to 105°C)

Symbol	Description	Conditions	MIN	MAX	Units
V_{IH}	High-level input voltage		0.5V_{DD}	—	V
V_{IL}	Low-level input voltage		—	0.3V_{DD}	V
I_{IN}	Input leakage current	V_{IN} = V_{DD}	—	+10	µA
		V_{IN} = V_{SS}	-10	—	
C_{IN}[1]	Input pin capacitance	f = 1MHz; V_{DD} = 0V, V_{DDC} = 0V	—	22	pF

Note:

1. Capacitance is measured for initial qualification and when design changes might affect the input/output capacitance .

DC Electrical Characteristics for PCI Outputs (pre- and post-radiation)

(V_{DD} = 3.3V±0.3V; V_{DDC} = 1.2V±0.1V; T_C = -55°C to 105°C)

Symbol	Description	Conditions	MIN	MAX	Units
V_{OH}	High-level output voltage (PCI_AD[31:0], PCI_C/BE[3: 0], PCI_RST, PCI_IDSEL, PCI_FRAME, PCI_IRDY], PCI_TRDY , PCI_DEVSEL , PCI_STOP, PCI_PERR, PCI_PAR)	I_{OH} =-500 µA	$0.9V_{DD}$	—	V
V_{OL}	Low-level output voltage (PCI_AD[31:0], PCI_C/BE[3: 0], PCI_RST, PCI_IDSEL, PCI_FRAME, PCI_IRDY], PCI_TRDY , PCI_DEVSEL, PCI_STOP, PCI_PERR, PCI_PAR)	I_{OL} =1500 µA	—	$0.1V_{DD}$	V
I_{OZ}	Three-state output current	$V_O = V_{DD}$	-10	+10	µA
		$V_O = V_{SS}$	-10	+10	
I_{OS} [1]	Short-circuit output current	$V_O = V_{DD}$; V_{DD} = 3.6V	—	270	mA
		$V_O = V_{SS}$; V_{DD} = 3.6V	-130	—	
C_{OUT} [2]	Output pin capacitance	ƒ = 1MHz; V_{DD} = 0V, V_{DDC} = 0V	—	22	pF

Notes:

1. Guaranteed by design
2. Capacitance is measured for initial qualification and when design changes might affect the input/output capacitance

AC Electrical Characteristics for PCI Inputs (pre- and post-radiation)

(V_{DD}=3.3V±0.3V; V_{DDC} =1.2V±0.1V; T_C=-55°C to 105°C)

Symbol	Description	Conditions	MIN	MAX	Units
f_{PCI_CLK}	PCI clock frequency		—	33	MHz
t_{HIGH}	PCI clock high time		11	—	ns
t_{LOW}	PCI clock low time		11	—	ns

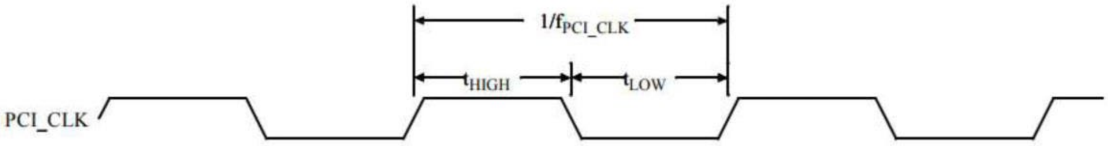

Figure 3:2: PCI Clock Timing Diagram

Timing Specifications

Power Sequencing and Reset

(V_{DD} = 3.3V±0.3V; V_{DDC} =1.2V±0.1V; T_C =-55°C to 105°C)

Symbol	Description	Conditions	MIN	MAX	Units
t_{VCD}[1]	V_{DD} valid to V_{DDC} delay	$V_{DD} \geq 3.0V$; $V_{DDC} \geq 1.1V$	0	—	ns
t_{VHBZ}[1]	V_{DD} valid to control signals high-z ($\overline{\mathrm{WRITE}}$, $\overline{\mathrm{OE}}$, $\overline{\mathrm{IOS}}$, $\overline{\mathrm{ROM[1:0]}}$, $\overline{\mathrm{RWE[3:0]}}$, $\overline{\mathrm{RAMOE[4:0]}}$, READ, $\overline{\mathrm{SDWE}}$, and $\overline{\mathrm{SDCS[1:0]}}$) V_{DD} valid to outputs high-z ([DATA[31:0], CB[15:0], and GPIO[15:0])	$V_{DD} \geq 1.5V$; $V_{DDC} = 0V$	—	4	t_{CLK}
t_{CHBV}[1]	V_{DDC} valid to control signals valid-inactive ($\overline{\mathrm{WRITE}}$, $\overline{\mathrm{OE}}$, $\overline{\mathrm{IOS}}$, $\overline{\mathrm{ROM[1:0]}}$, $\overline{\mathrm{RWE[3:0]}}$, $\overline{\mathrm{RAMOE[4:0]}}$, READ, $\overline{\mathrm{SDWE}}$, and $\overline{\mathrm{SDCS[1:0]}}$)	$V_{DD} \geq 3.0V$; $V_{DDC} \geq 1.1V$	—	4	t_{CLK}
t_{RESET1}[1]	V_{DDC} valid to $\overline{\mathrm{RESET}}$ deassert	$V_{DDC} \geq 1.1V$	4	—	t_{CLK}
t_{RESET2}[1]	$\overline{\mathrm{RESET}}$ deasserted to outputs valid-active ($\overline{\mathrm{ROMS[0]}}$ and $\overline{\mathrm{OE}}$)		—	12	t_{CLK}
t_{RESET3}[1]	$\overline{\mathrm{RESET}}$ asserted to control signals valid inactive ($\overline{\mathrm{WRITE}}$, $\overline{\mathrm{OE}}$, $\overline{\mathrm{IOS}}$, $\overline{\mathrm{ROM[1:0]}}$, $\overline{\mathrm{RWE[3:0]}}$, $\overline{\mathrm{RAMOE[4:0]}}$, READ, $\overline{\mathrm{SDWE}}$, and $\overline{\mathrm{SDCS[1:0]}}$) $\overline{\mathrm{RESET}}$ asserted to outputs high-z (DATA[31:0], CB[15:0], and GPIO[15:0])		—	4	t_{CLK}

Note:

1. Guaranteed by design.

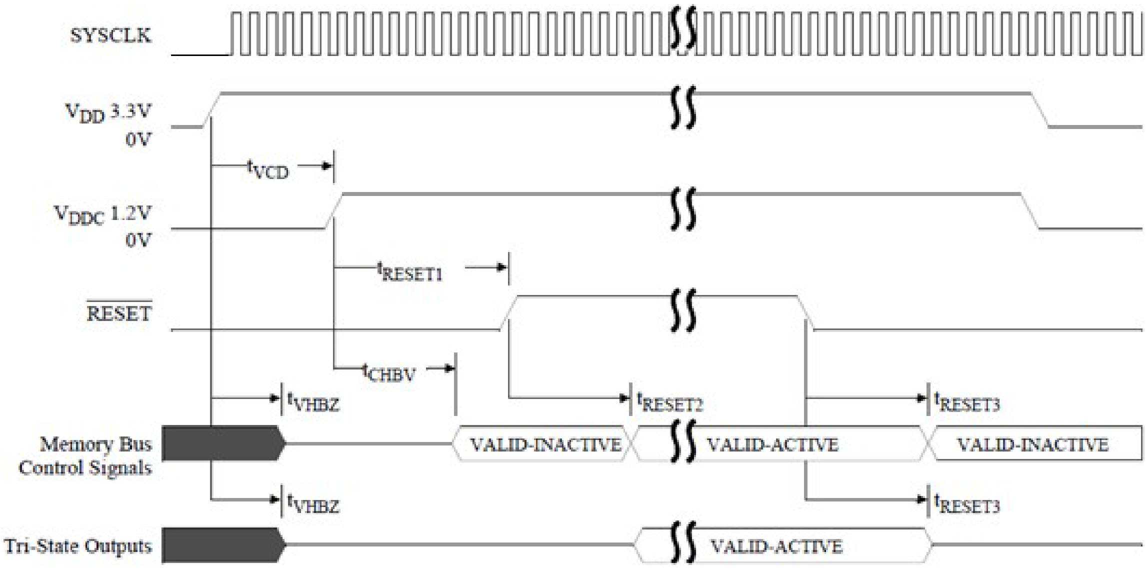

Figure 4:1: Power Sequencing and Reset Timing Diagram

Power Sequencing

For optimal power sequencing, both power-up and power-down, ramp both V_{DD} and V_{DDC} together. During power- up, if $V_{DDC} > V_{DD} + 0.3V$, excessive current or damage may occur to the device. During power down, it is acceptable for V_{DD} to be less than V_{DDC} by more than 0.3V as long as V_{DDC} is not actively driven.

Bus Control and Bi-Direct Fail-Safe Circuitry

In order to prevent bus contention on the external memory interface while V_{DDC} is ramping up, the UT700 has functionality to ensure that the bi-direct and memory bus control signals described in Section 4.1 will be in a high-z state t_{VHBZ} delay after V_{DD} reaches 1.5V. The core logic will put these signals into their valid-inactive states t_{CHBV} clock cycles after V_{DDC} reaches 1.1V.

Frontgrade recommends that users place pull-up resistors on the indicated output enable, write enable, and chip select pins, and a pulldown resistor on the READ pin, if t_{VCD} is greater than 100ns. This will prevent bus capacitance or transients from inadvertently placing these pins in an active state, which could result in external memory devices driving the address and data buses.

Reset Circuitry

The reset circuitry is controlled by the core logic; therefore, the circuitry is functional only after V_{DDC} reaches its minimum operating voltage of 1.1V. After V_{DDC} is stable, the system must continue to assert $\overline{\text{RESET}}$ for a minimum of t_{RESET1} clock cycles before it can be de-asserted. Asserting $\overline{\text{RESET}}$ for less time could result in the $\overline{\text{RESET}}$ signal not being recognized.

The UT700 will begin fetching code from external memory no more than t_{RESET2} clock cycles after $\overline{\text{RESET}}$ is de-asserted. Control signals $\overline{\text{ROMS[0]}}$, and $\overline{\text{OE}}$ will be driven to their valid-active states in order for the UT700 to begin fetching code from PROM. During normal operation, the indicated bus control signals will go to a valid-inactive state, and the bi-directs will go to a high-z state, within t_{RESET3} clock cycles after the assertion of $\overline{\text{RESET}}$.

Boot Strap Programming on GPIO

Data on pins GPIO[2:0], GPIO[7:4] and GPIO[15:12] are latched on the rising edge of reset. The states of GPIO[2:0] determine the data width of the PROM area and enable EDAC for the PROM area. Chapter 3 of the User's Manual describes the value of these inputs to achieve the required operation. The states of GPIO[7:4] provide a means to configure the SpaceWire clock divisor link bits in the Clock Divisor Register. The states of GPIO[15:12] set the least significant address nibble of the IP and MAC address for the Ethernet Debug Communication Link (EDCL).

In order for the state of GPIO pins to be properly latched, Frontgrade recommends placing pull-up or pull-down resistors on these pins to ensure that the setup and hold timing is met. The states of these pins should be statically set prior to the rising edge of $\overline{\text{RESET}}$.

Output Timing Characteristics for Memory Interface, $\overline{\text{ERROR}}$ and $\overline{\text{WDOG}}$

(V_{DD} = 3.3V±0.3V; V_{DDC} = 1.2V±0.1V; T_C = -55°C to 105°C)

Symbol	Description	MIN	MAX	Units
t1a[1]	SDCLK↑ to ADDR[27:0] valid	1.5	8.5	ns
t1b[1]	SDCLK↑ to $\overline{\text{SDCS[1:0]}}$ valid	2	7.5	ns
t1c[1]	SDCLK↑ to output valid $\overline{\text{SDRAS}}$, $\overline{\text{SDCAS}}$, and $\overline{\text{SDWE}}$	1.5	8.5	ns
t1d[1]	SDCLK↑ to SDDQM[3:0] valid	2.5	8.5	ns
t1e[1]	SDCLK↑ to output valid ($\overline{\text{WRITE}}$, $\overline{\text{OE}}$, $\overline{\text{IOS}}$, $\overline{\text{ROM[1:0]}}$, $\overline{\text{RWE[3:0]}}$, $\overline{\text{RAMOE[4:0]}}$, $\overline{\text{RAMS[1:0]}}$, and READ)	1	8	ns
t2[1, 2]	SDCLK↑ to output valid (DATA[31:0] and CB[15:0])	2.5	8.5	ns
t3[1, 2, 3]	SDCLK↑ to output high-Z (DATA[31:0] and CB[15:0])	2.5	8.5	ns
t4[1, 4]	SDCLK↑ to signal low ($\overline{\text{ERROR}}$ and $\overline{\text{WDOG}}$[4])	—	10	ns
t8[1, 2, 3]	$\overline{\text{WRITE}}$ ↑ or $\overline{\text{RWE[3:0]}}$ ↑ to output high-z (DATA [31:0] and CB[15:0])	0.5	—	ns
t9[1]	Skew from first memory output signal transition to last memory output signal transition	—	2	ns

Notes:

1. All outputs are measured using the load conditions shown in Figure 4:14
2. CB[7] is not tested in the case of BCH EDAC
3. High-Z defined as +/-300mV change from steady state
4. Guaranteed by design

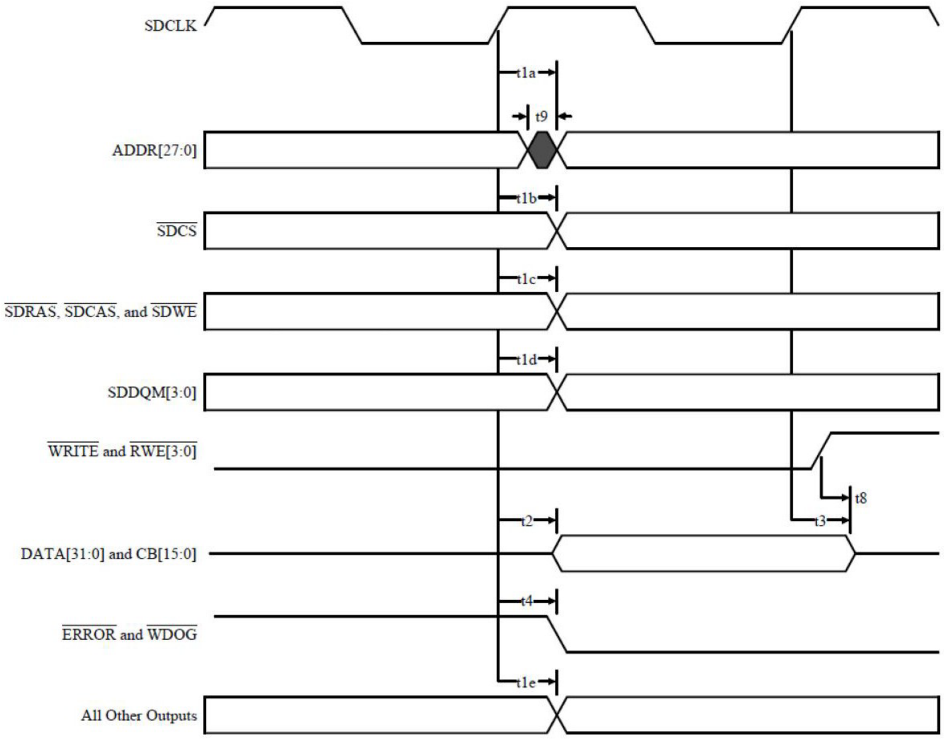

Figure 4:2: Memory Interface, $\overline{\text{ERROR}}$ and $\overline{\text{WDOG}}$ Output Timing Diagram

Input Timing Characteristics for Memory Interface

(V_{DD}=3.3V±0.3V; V_{DDC}=1.2V±0.1V; T_C=-55°C to 105°C)

Symbol	Description	MIN	MAX	Units
t5a[1]	Setup time to SDCLK↑ (DATA[31:0] and CB[15:0])	1	—	ns
t5b	Setup time to SDCLK↑ ($\overline{\text{BEXC}}$, and synchronous $\overline{\text{BRDY}}$)	2	—	ns
t6a[1]	Hold time from SDCLK↑ (DATA[31:0] and CB[15:0])	1.5	—	ns
t6b	Hold time from SDCLK↑ (Synchronous $\overline{\text{BRDY}}$)	0	—	ns
t7[2]	Asynchronous $\overline{\text{BRDY}}$ pulse width	1.5	—	tCLK

Notes:
1. CB[7] is not tested in the case of BCH EDAC
2. Supplied as a design limit. Neither guaranteed nor tested

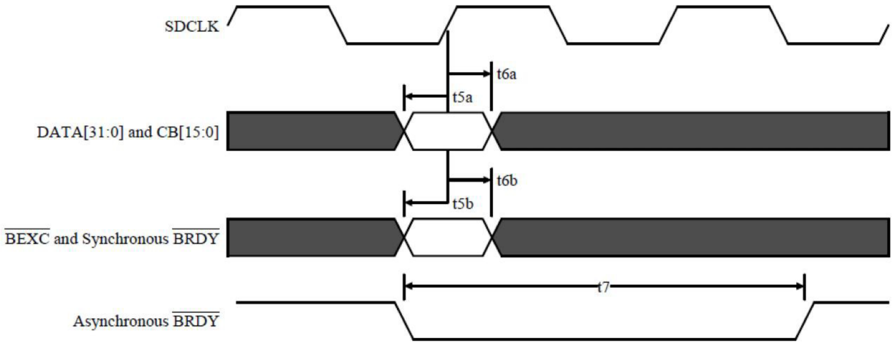

Figure 4:3: Memory Interface Input Timing Diagram

Input Timing Characteristics for Memory Interface

(V_{DD}=3.3V±0.3V; V_{DDC}=1.2V±0.1V; T_C=-55°C to 105°C)

Symbol	Description	MIN	MAX	Units
t10[1]	SDCLK↑ to GPIO output valid (GPIO[15:0])	—	10	ns

Note:
1. All outputs are measured using the load conditions shown in Figure 4:14

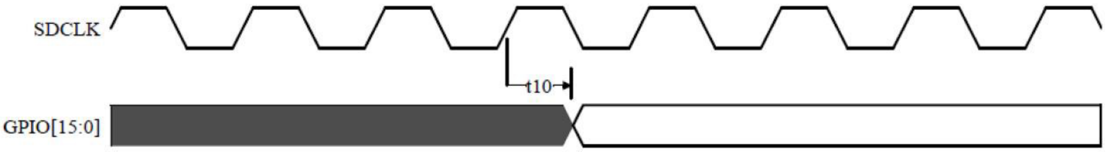

Figure 4:4: General Purpose I/O Timing Diagram

Timing Characteristics for SpaceWire Interface

(V_{DD} = 3.3V±0.3V; V_{DDC} =1.2V±0.1V; T_C=-55°C to 105°C)

Symbol	Description	MIN	MAX	Units
t11[1, 2]	SPW_CLK period	5	—	ns
t14[3, 4, 5]	Transmit data and strobe bit width variation (SPW_TXD[3:0] and SPW_TXS[3:0])	UI-600	UI+600	ps
t15[5, 6]	Receive data and strobe bit width (SPW_RXD[3:0] and SPW_RXS[3:0])	5	—	ns
t16[5]	Receive data and strobe edge separation (SPW_RXD[3:0] and SPW_RXS[3:0])	1/2*t11 + 0.5	—	ns

Notes:

1. The SPW_CLK frequency must be less than or equal to 10x the SYSCLK frequency. For example, if SPW_CLK is running at 200MHz, the SYSCLK frequency must be greater than or equal to 20MHz.
2. Functionally tested.
3. Applies to both high pulse and low pulse.
4. A unit interval (UI) is defined as the nominal, or ideal, bit width.
5. Guaranteed by design.
6. The SPW_CLK period must be less than or equal to the minimum receive data/strobe bit width.

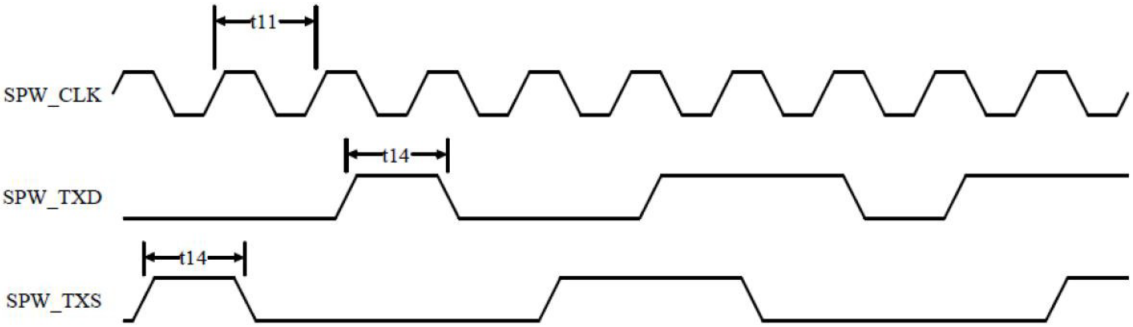

Figure 4:5: SpaceWire Transmit Timing Diagram

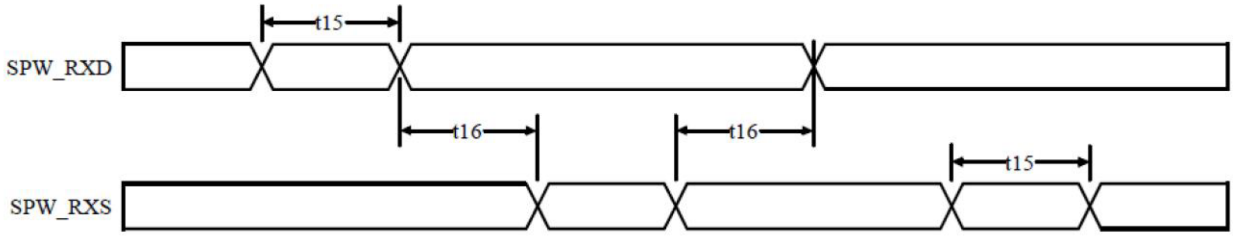

Figure 4:6: SpaceWire Receive Timing Diagram

Timing Characteristics for PCI Interface

(V_{DD}=3.3V±0.3V; V_{DDC}=1.2V±0.1V; T_C=-55°C to 105°C)

Symbol	Description	MIN	MAX	Units
t17[1]	PCI_CLK↑ to output valid (PCI_AD[31:0], PCI_C/BE[3:0], PCI_PAR, PCI_FRAME, PCI_IRDY, PCI_TRDY, PCI_STOP, PCI_DEVSEL, PCI_REQ, and PCI_ARBGNT[7:0])	2	13	ns
t18[1, 2]	PCI_CLK↑ to output valid from high-z (PCI_AD[31:0], PCI_C/BE[3:0], PCI_PAR, PCI_FRAME, PCI_IRDY, PCI_TRDY, PCI_STOP, PCI_DEVSEL, PCI_PERR)	2	13	ns
t19[1, 2]	PCI_CLK↑ to output high-Z (PCI_AD[31:0], PCI_C/BE[3:0], PCI_PAR, PCI_FRAME, PCI_IRDY, PCI_TRDY, PCI_STOP, PCI_DEVSEL, PCI_PERR)	—	14	ns
t20[3, 4]	Setup time to PCI_CLK↑ (PCI_AD[31:0], PCI_C/BE[3:0], PCI_PAR, PCI_FRAME, PCI_IRDY, PCI_TRDY, PCI_STOP, PCI_DEVSEL, PCI_PERR, PCI_IDSEL, PCI_GNT, and PCI_ARB_REQ[7:0])	4	—	ns
t21[3, 4]	Hold time from PCI_CLK↑ (PCI_AD[31:0], PCI_C/BE[3:0], PCI_PAR, PCI_FRAME, PCI_IRDY, PCI_TRDY, PCI_STOP, PCI_DEVSEL, PCI_PERR, PCI_IDSEL, PCI_GNT , and PCI_ARB_REQ[7:0])	1	—	ns
t22[5]	PCI_CLK↑ to RESET deassertion	10	—	PCI Clocks
t23a[5]	PCI_CLK↑ to PCI_RST deassertion	10	—	PCI Clocks
t23b[5]	PCI_RST assertion to PCI_CLK idle	10	—	PCI Clocks
t24	PCI_RST active to output high-Z	—	40	ns

Notes:

1. All outputs are measured using the load conditions shown in Figure 4:14
2. High-Z defined as +/-300mV change from steady state.
3. PCI_TRDY, PCI_STOP and PCI_DEVSEL timing is guaranteed by design when used as inputs.
4. PCI_PERR and PCI_GNT are guaranteed by design.
5. Guaranteed by design.

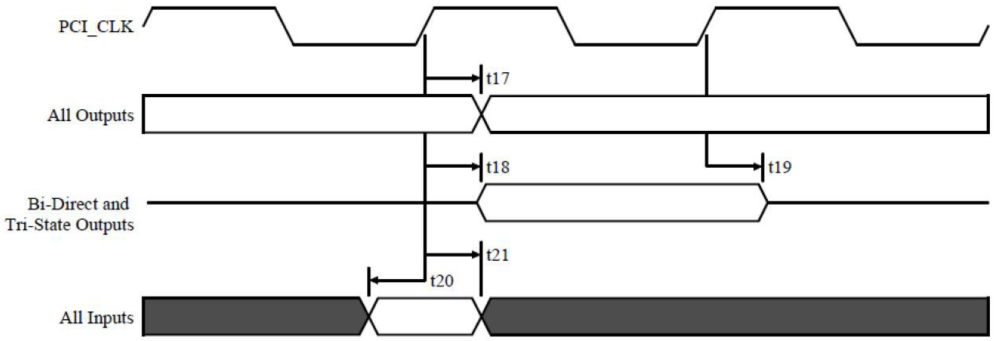

Figure 4:7: PCI Timing Diagram

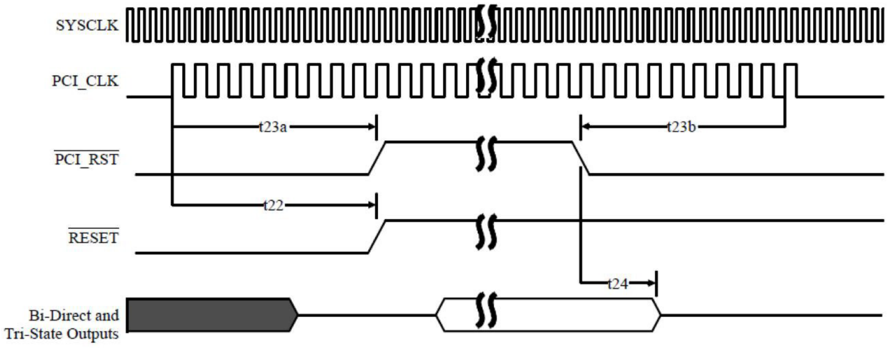

Figure 4:8: Timing Relationships of Clock and Reset for PCI Core Utilization

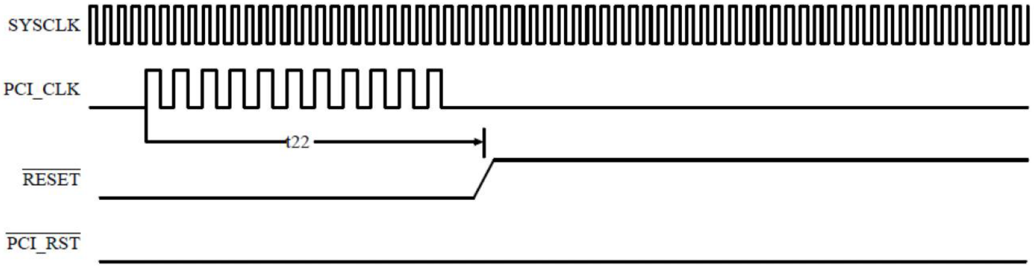

Figure 4:9: Timing Relationships of Clock and Reset for Unused PCI Core

Timing Characteristics for Ethernet Interface

(V_{DD} = 3.3V±0.3V; V_{DDC} = 1.2V±0.1V; T_C =-55°C to 105°C)

Symbol	Description	MIN	MAX	Units
t25[1]	ETX_CLK↑ to output valid (ETXD [3:0], and ETX_EN)	—	12	ns
t26[2, 3]	Setup time to ERX_CLK↑ (ERX_DV, ERX_ER, and ERXD[3:0])	3	—	ns
t27[2, 3]	Hold time from ERX_CLK↑ (ERX_DV, ERX_ER, and ERXD[3:0])	1	—	ns
t28[1]	EMDC↑ to output valid (EMDIO)	$-4+t_{AMBA}$[4]	$4+t_{AMBA}$[4]	ns
t29[5]	Setup time to EMDC↑ (EMDIO)	10	—	ns
t30[5]	Hold time from EMDC↑ (EMDIO)	10	—	ns

Notes:

1. All outputs are measured using the load conditions shown in Figure 4:14
2. ERX_ER timing is guaranteed by design.
3. ERX_COL and ERX_CRS are asynchronous inputs and are not tested.
4. t_{AMBA} is defined as t_{SYSCLK} for NODIV = 1 and t_{SYSCLK} * 2 for NODIV = 0.
5. Guaranteed by design.

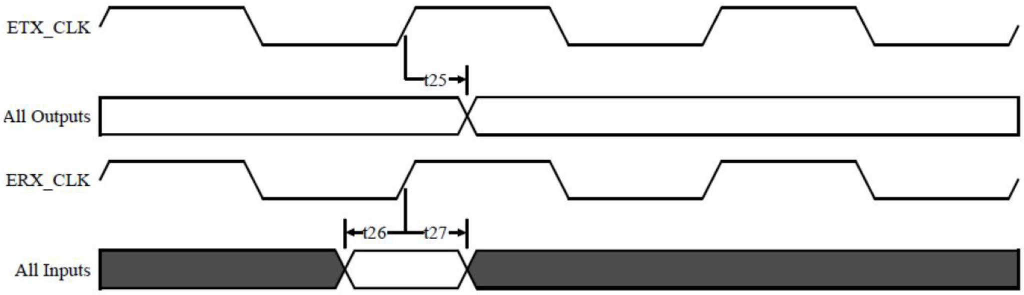

Figure 4:10: Ethernet Transmit and Receive Timing

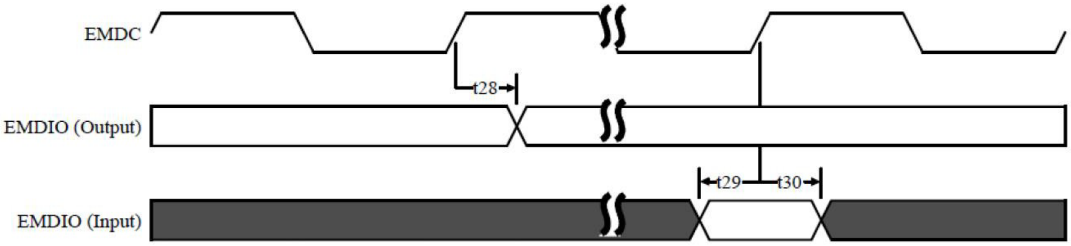

Figure 4:11: Ethernet MDIO Interface Timing

Timing Characteristics for MIL-STD-1553 Interface[2]

(V_{DD} = 3.3V±0.3V; V_{DDC} = 1.2V±0.1V; T_C = -55°C to 105°C)

Symbol	Description	MIN	MAX	Units
t31[1]	1553CLK↑ to output valid (1553RXENA, 1553RXENB, 1553TXINHA, 1553TXINHB, 1553TXA, $\overline{\text{1553TXA}}$, 1553TXB, and $\overline{\text{1553TXB}}$)	—	20	ns

Notes:

1. All outputs are measured using the load conditions shown in Figure 4:14
2. The 1553RXA, $\overline{\text{1552RXA}}$, 1553RXB, and $\overline{\text{1553RXB}}$ inputs are resynchronized internally.

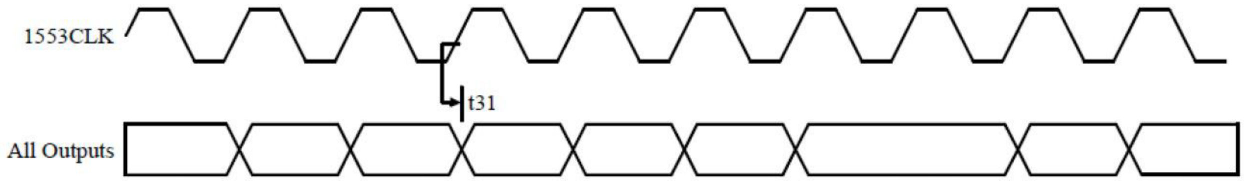

Figure 4:12: MIL-STD-1553 Interface Timing

Timing Characteristics for SPI[2]

(V_{DD} = 3.3V±0.3V; V_{DDC} = 1.2V±0.1V; T_C = -55°C to 105°C)

Symbol	Description	MIN	MAX	Units
t32[1]	SPICLK↑ to output valid (SPIMOSI)	-2	2	ns

Notes:

1. All outputs are measured using the load conditions shown in Figure 4:14
2. The SPIMISO input is resynchronized internally.

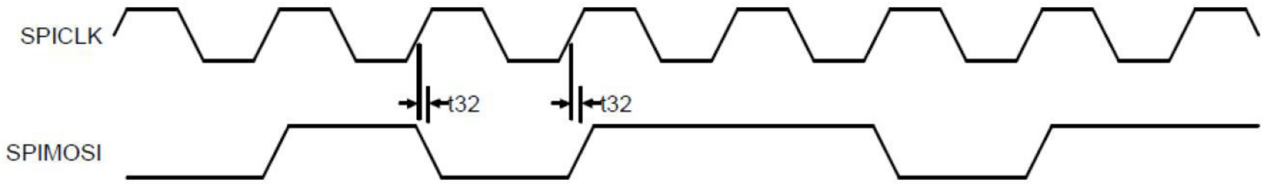

Figure 4:13: Serial Peripheral Interface (SPI) Timing

Test Conditions for Timing Specifications

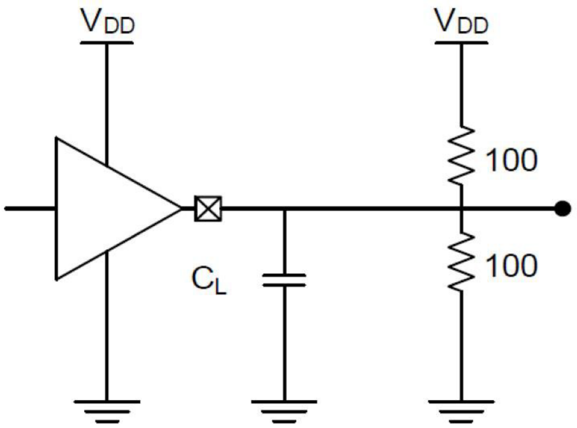

Figure 4:14: Equivalent Load Circuit for Timing Characteristics Tests

Notes:

1. C_L = 50 pF for ATE test load
2. C_L = 15 pF for benchtop test load

Packaging

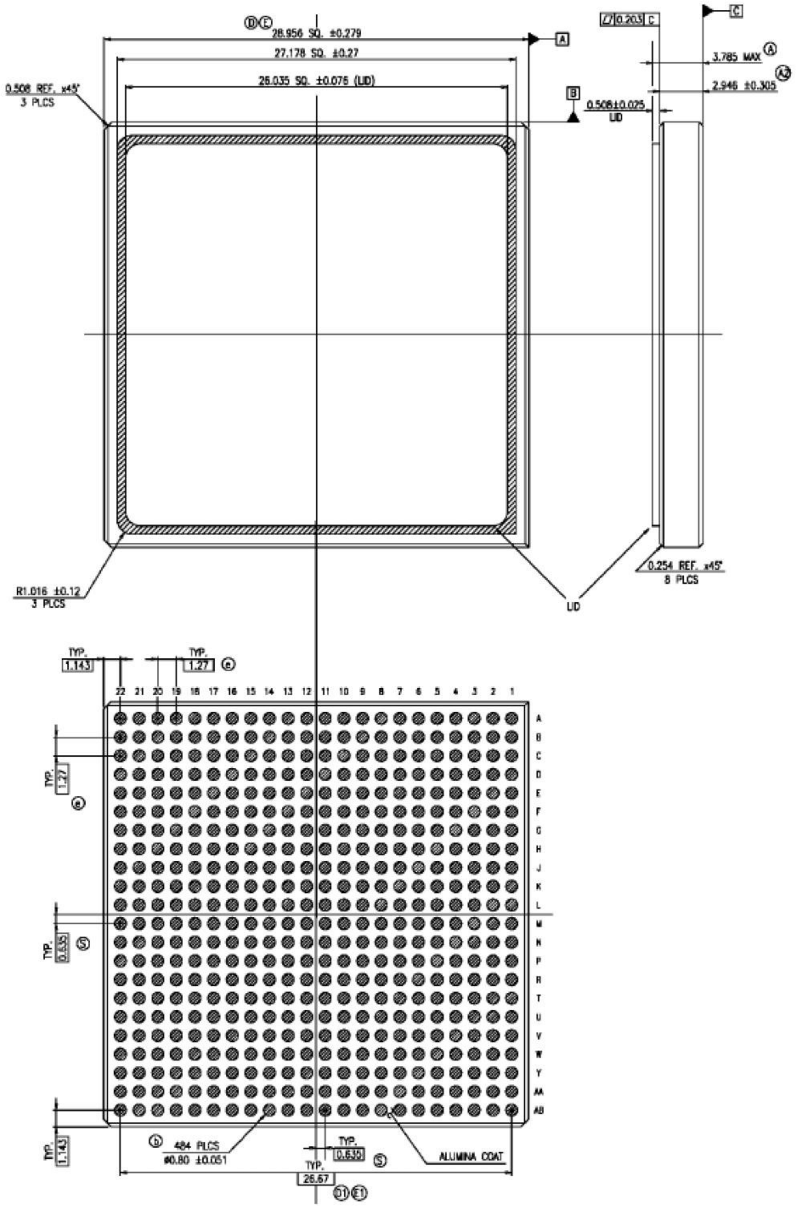

Figure 5:1: 484-lead Ceramic Land Grid Array

Notes:

1. Lid is connected to V_{SS}
2. Units are millimeters.

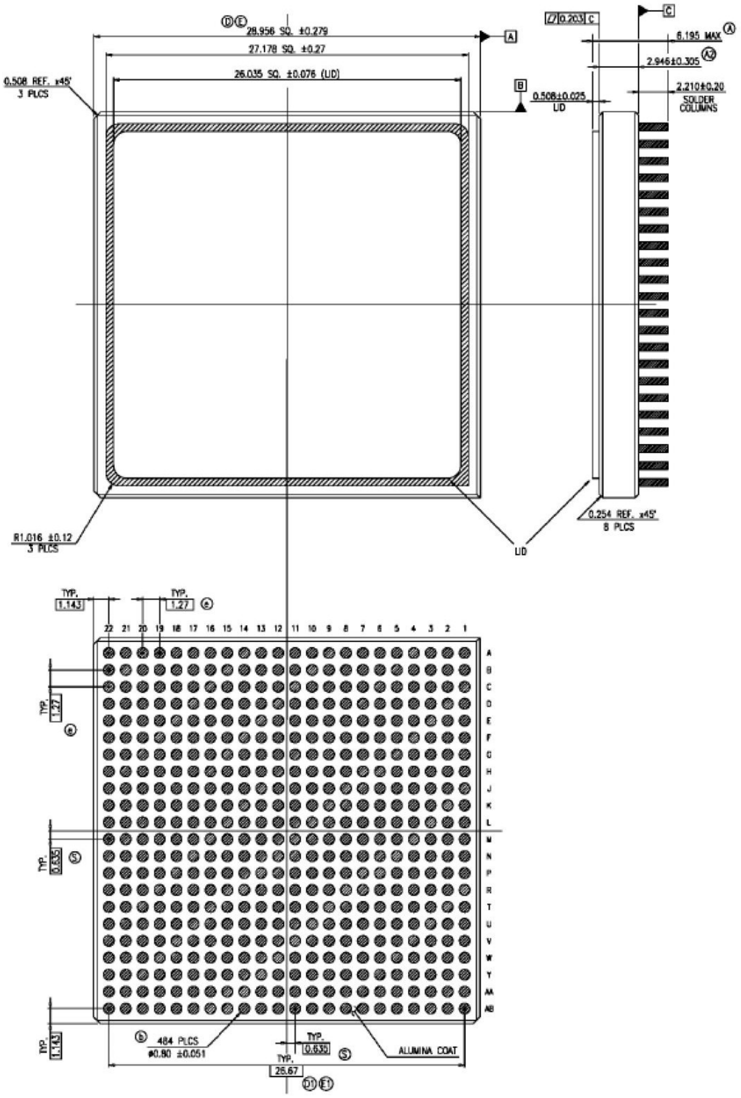

Figure 5:2: 484-lead Ceramic Column Grid Array

Notes:

1. Lid is connected to V_{SS},
2. Units are millimeters.

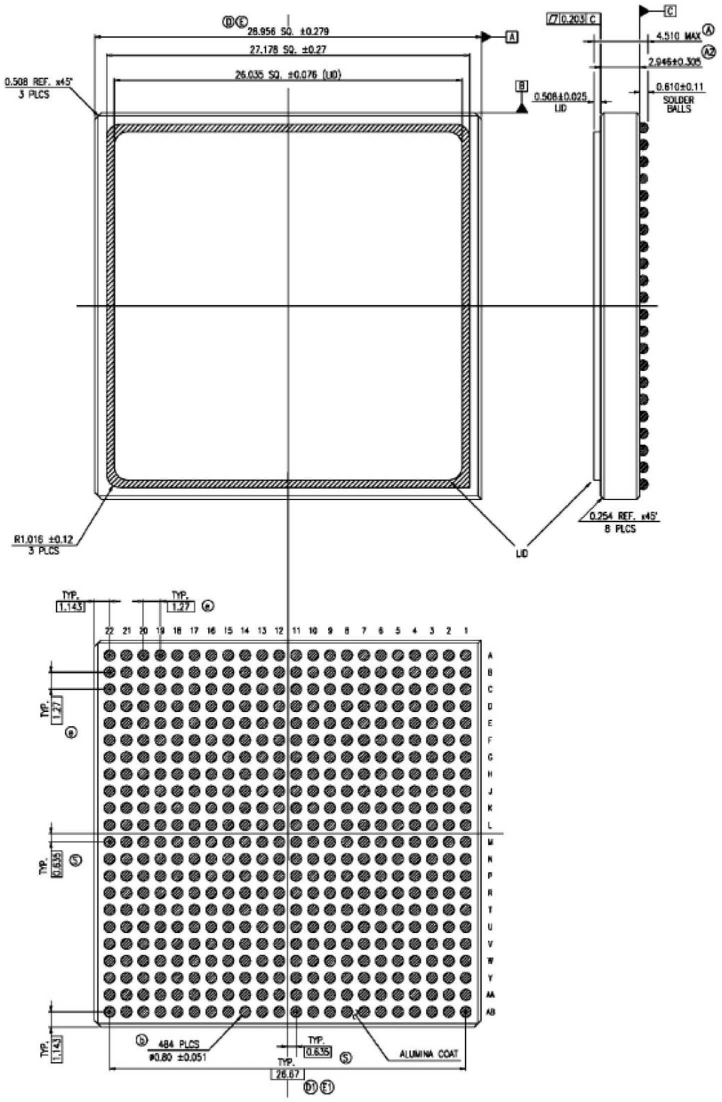

Figure 5:3: 484-lead Ceramic Ball Grid Array

Notes:

1. Lid is connected to V_{SS}
2. Units are millimeters.

Ordering Information

UT700 LEON 3FT Frontgrade Part Numbering Ordering Information

UT700 * * *

Lead Finish: (Note: 1)
(C) = Gold
(A) = Hot Solder Dipped or Tinned

Screening Level: (Note: 2, 3)
(P) = Prototype (Temperature Range 25°C only)
(E) = HiRel (Temperature Range: -55°C to +105°C)

Case Outline:
(Z) = 484-Ceramic Land Grid Array
(S) = 484-Ceramic Column Grid Array
(C) = 484-Ceramic Ball Grid Array

Device Type:
UT700 32-bit LEON 3FT

Notes:

1. Lead finish (A, C, or X) must be specified.
2. Prototype Flow per Frontgrade Manufacturing Flows Document. Tested at 25°C only. Lead finish is GOLD ONLY Radiation neither tested nor guaranteed.
3. HiRel Temperature Range Flow per Frontgrade Manufacturing Flows Document. Devices are tested at -55°C room temp, and 125°C. Radiation neither tested nor guaranteed.

Package Options

Package Option	Associated Lead Finish
(Z) 484-CLGA	(C) Gold
(S) 484-CCGA	(A) Hot Solder Dipped
(C) 484-CBGA	(A) Hot Solder Dipped

Ordering Information

UT700 LEON 3FT: SMD Part Number Ordering Information

5962 - 13238 ** * * *

Lead Finish: (Note: 1)
(C) = Gold
(X) = Solder

Case Outline:
(X) = 484-Ceramic Land Grid Array Package
(Y) = 484-Ceramic Column Grid Array Package

Screening Level:
(Q) = QML Class Q
(V) = QML Class V

Device Type:
(01) = UT700 (Temperature range: -55°C to +105°C)

Drawing Number:
13238

Total Dose
(R) = 1E5 rad(Si)

Federal Stock Class Designator
No Options

Note:

1. Lead finish is “C” (gold) only.

Revision History

Date	Revision #	Author	Change Description	Page #
11/19/13	1.0.0		Release of Preliminary Data Sheet	
08/26/14	1.1.0		Release Production Datasheet Corrected SEL Immune Corrected V_{DDC}, V_{DD} limits, and note 3 temperature Moved Operational Environment table from section 5 to 3.3 and updated Added IDDCS, IDDS limits from TBD Added IIN and IIN limits (to bound the range for pull up/down resistors) Corrected tDSD limits Corrected IIN and IOZ limits Corrected symbols t14, t15, t16, and the corresponding timing diagrams Moved the Operational Environment table to section 3.3 on page 16 Corrected package drawings	
11/21/14	1.2.0		Changed Figure 1.1 Data and Instr Cache Values from 2x4kB to 4x4kB Added GPIO[2] entry to Bootstrap signals table Re-wrote section 4.1.4 Corrected SMD lead finish designator Added Footer	
3/XX/15	1.3.1		Removed note 3 and changed the maximum junction temperature value from 125°C to 150°C in the Absolute Maximum Ratings Table. Rewrote section 4.1.1 on power sequencing	
09/06/2017	2.0.0		New Format	
01/16/2018	2.0.1		Update to Class information	
02/01/2018	2.0.2		Alignment	
04/24/2018	2.0.3		Release of Preliminary Data Sheet	

Datasheet Definitions

	Definition
Advanced Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the **datasheet is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final.**
Preliminary Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.