



FRONTGRADE

DATASHEET

UT54ACS74/UT54ACTS74

Dual D Flip-Flops with Clear & Preset

11/1/2010

Version #: 1.0

Features

- 1.2 μ CMOS
 - > Latchup immune
- High speed
- Low power consumption
- Single 5-volt supply
- Available QML Q or V processes
- Flexible package
 - > 14-pin DIP
 - > 14-lead flatpack
- UT54ACS74 - SMD 5962-96534
- UT54ACTS74 - SMD 5962-96535

Description

The UT54ACS74 and the UT54ACTS74 contain two independent D-type positive triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the D input meeting the setup time requirement is transferred to the outputs on the positive-going edge of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

The devices are characterized over full military temperature range of -55°C to +125°C.

Function Table

Inputs				Output	
$\overline{\text{PRE}}$	$\overline{\text{CLR}}$	CLK	D	Q	$\overline{\text{Q}}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H 1	H 1
H	H	\uparrow	H	H	L
H	H	\uparrow	L	L	H
H	H	L	X	Q ₀	$\overline{\text{Q}}_0$

Note:

1. The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at preset and clear are near V_{IL} maximum. In addition, this configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

Pinouts

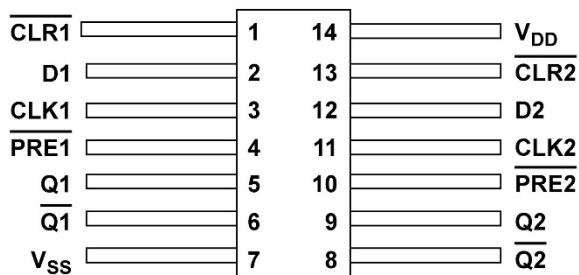


Figure 1: 14-Pin DIP, Top View

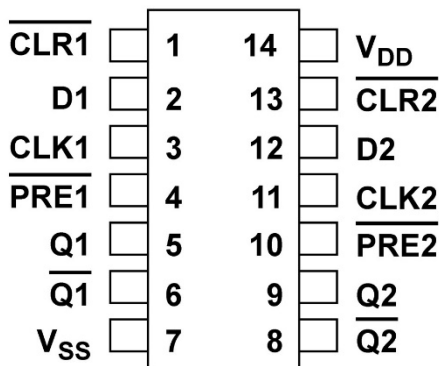
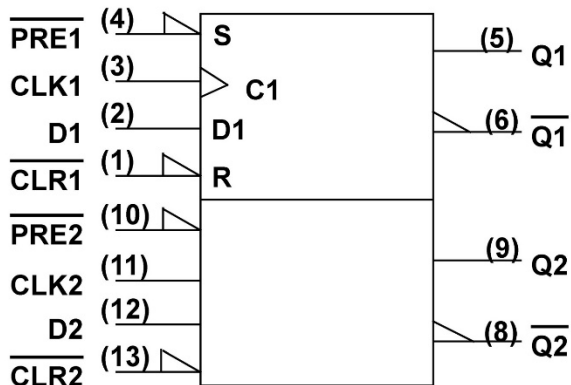


Figure 2: 14-Lead Flatpack, Top View

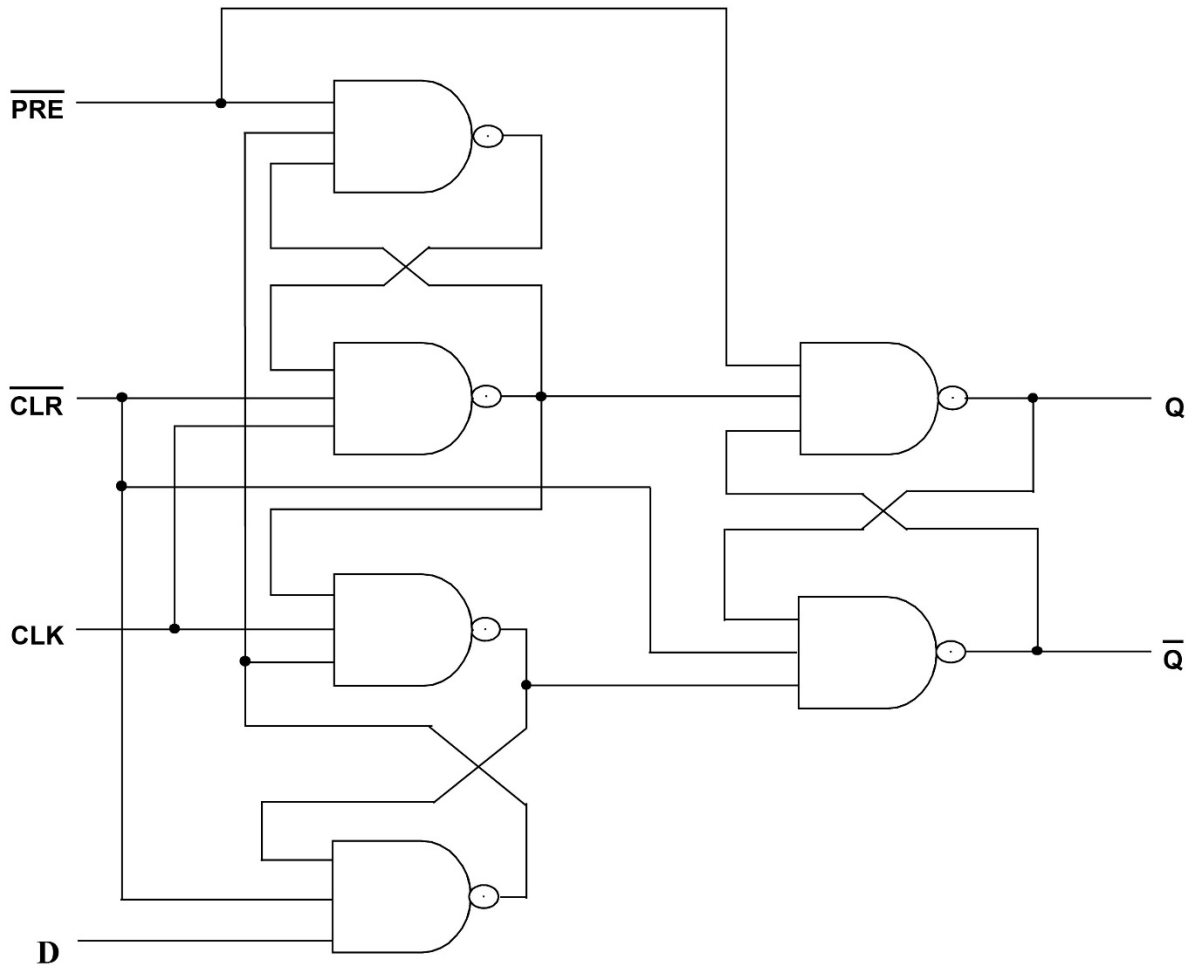
Logic Symbol



Note:

1. Logic symbol in accordance with ANSI/IEEE standard 91-1984 and IEC Publication 617-12.

Logic Diagram



Operational Environment¹

Parameter	Limit	Units
Total Dose	1.0E6	rads(Si)
SEU Threshold ²	80	MeV-cm ² /mg
SEL Threshold	120	MeV-cm ² /mg
Neutron Fluence	1.0E14	n/cm ²

Notes:

1. Logic will not latchup during radiation exposure within the limits defined in the table.
2. Device storage elements are immune to SEU affects.

Absolute Maximum Ratings

Symbol	Parameter	Limit	Units
V_{DD}	Supply voltage	-0.3 to 7.0	V
$V_{I/O}$	Voltage any pin	-3 to $V_{DD} + 3$	V
T_{STG}	Storage Temperature range	-65 to +150	°C
T_J	Maximum junction temperature	+175	°C
T_{LS}	Lead temperature (soldering 5 seconds)	+300	°C
Θ_{JC}	Thermal resistance junction to case	20	°C/W
I_I	DC input current	±10	mA
P_D	Maximum power dissipation	1	W

Notes:

- Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Limits	Units
V_{DD}	Supply voltage	4.5 to 5.5	V
V_{IN}	Input voltage any pin	0 to V_{DD}	V
T_C	Temperature range	-55 to +125	°C

Electrical Characteristics⁷

($V_{DD} = 5.0V \pm 10\%$; $V_{SS} = 0V^6$, $-55^\circ C < T_c < +125^\circ C$); Unless otherwise noted, T_c is per the temperature range ordered.

Symbol	Description	Condition	MIN	MAX	Unit
V_{IL}	Low-level input voltage ¹ ACTS ACS			0.8 .3 V_{DD}	V
V_{IH}	High-level input voltage ¹ ACTS ACS		.5 V_{DD} .7 V_{DD}		V
I_{IN}	Input leakage current ACTS/ACS	$V_{IN} = V_{DD}$ or V_{SS}	-1	1	μA
V_{OL}	Low-level output voltage ³ ACTS ACS	$I_{OL} = 8.0mA$ $I_{OL} = 100\mu A$		0.40 0.25	V
V_{OH}	High-level output voltage ³ ACTS ACS	$I_{OH} = -8.0mA$ $I_{OH} = -100\mu A$.7 V_{DD} $V_{DD} - 0.25$		V
I_{OS}	Short-circuit output current ^{2,4} ACTS/ACS	$V_O = V_{DD}$ and V_{SS}	-200	200	mA
I_{OL}	Output current ¹⁰ (Sink)	$V_{IN} = V_{DD}$ or V_{SS} $V_{OL} = 0.4V$	8		mA
I_{OH}	Output current ¹⁰ (Source)	$V_{IN} = V_{DD}$ or V_{SS} $V_{OH} = V_{DD} - 0.4V$	-8		mA
P_{total}	Power dissipation ^{2,8,9}	$C_L = 50pF$		1.9	mW/ MHz
I_{DDQ}	Quiescent Supply Current	$V_{DD} = 5.5V$		10	μA
ΔI_{DDQ}	Quiescent Supply Current Delta ACTS	For input under test $V_{IN} = V_{DD} - 2.1V$ For all other inputs $V_{IN} = V_{DD}$ or V_{SS} $V_{DD} = 5.5V$		1.6	mA
C_{IN}	Input capacitance ⁵	$f = 1MHz @ 0V$		15	pF
C_{OUT}	Output capacitance ⁵	$f = 1MHz @ 0V$		15	pF

Notes:

1. Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: $V_{IH} = V_{IH(min)} + 20\%$, $- 0\%$; $V_{IL} = V_{IL(max)} + 0\%$, $- 50\%$, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to $V_{IH(min)}$ and $V_{IL(max)}$.
2. Supplied as a design limit but not guaranteed or tested.
3. Per MIL-PRF-38535, for current density $\leq 5.0E5$ amps/cm², the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765 pF/MHz.
4. Not more than one output may be shorted at a time for maximum duration of one second.
5. Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at a frequency of 1MHz and a signal amplitude of 50mV rms maximum. 6) Maximum allowable relative shift equals 50mV.
6. All specifications valid for radiation dose $\leq 1E6$ rads(Si).
7. Power does not include power contribution of any TTL output sink current.
8. Power dissipation specified per switching output.
9. This value is guaranteed based on characterization data, but not tested.

AC Electrical Characteristics²

($V_{DD} = 5.0V \pm 10\%$; $V_{SS} = 0V^1$, $-55^{\circ}C < T_C < +125^{\circ}C$); Unless otherwise noted, T_C is per the temperature range ordered.

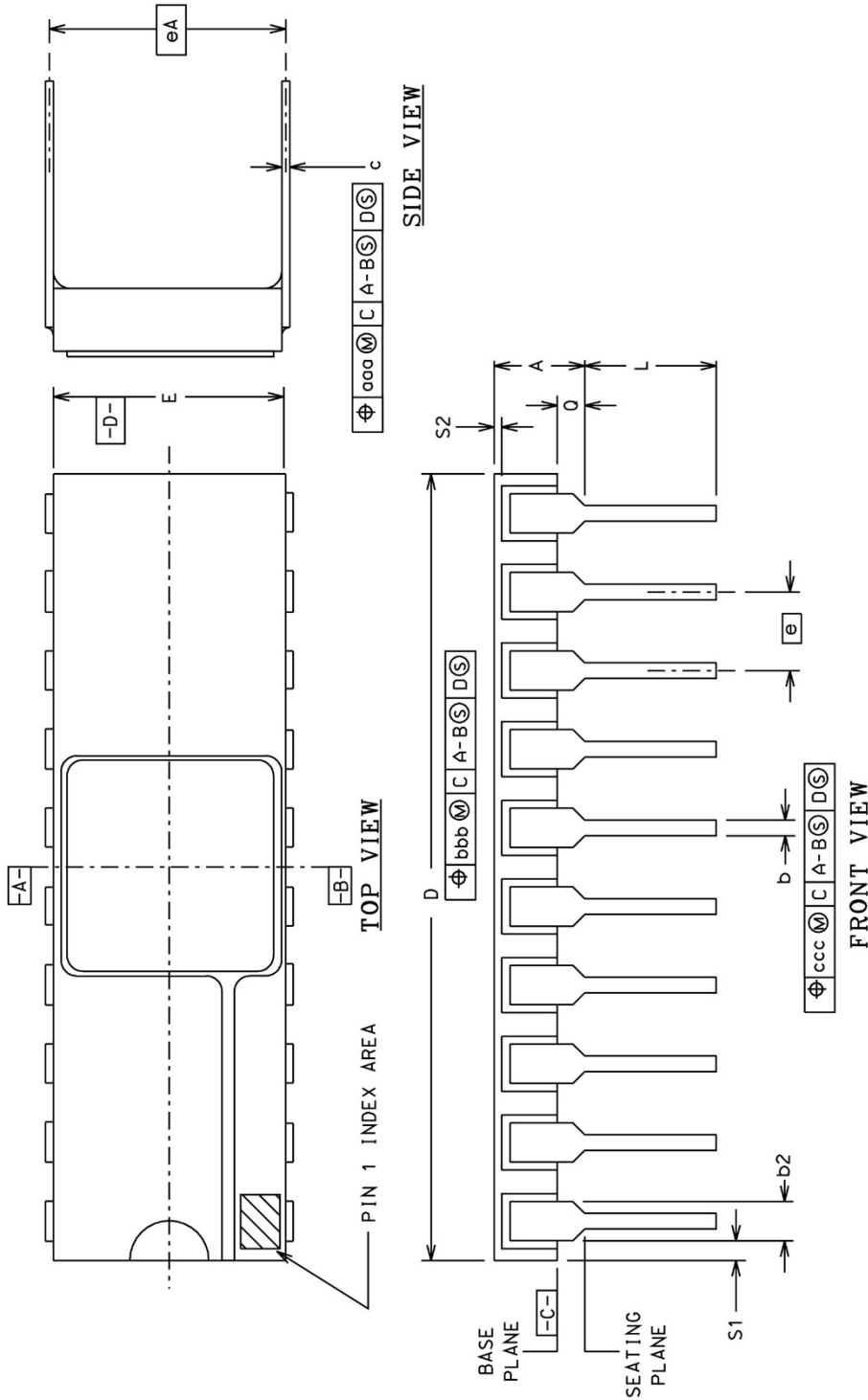
Symbol	Parameter	Minimum	Maximum	Unit
t_{PHL}	CLK to Q, \bar{Q}	3	21	ns
t_{PLH}	CLK to Q, \bar{Q}	1	20	ns
t_{PLH}	\overline{PRE} to Q	1	15	ns
t_{PHL}	\overline{PRE} to \bar{Q}	3	19	ns
t_{PHL}	\overline{CLR} to Q	3	19	ns
t_{PLH}	\overline{CLR} to \bar{Q}	1	15	ns
f_{MAX}	Maximum clock frequency		71	MHz
t_{SU1}	\overline{PRE} or \overline{CLR} inactive Setup time before CLK \uparrow	5		ns
t_{SU2}	Data setup time before CLK \uparrow	5		ns
t_{H3}	Data hold time after CLK \uparrow	2		ns
t_W	Minimum pulse width \overline{PRE} or \overline{CLR} low CLK high CLK low	7		ns

Notes:

1. Maximum allowable relative shift equals 50mV.
2. All specifications valid for radiation dose $\leq 1E6$ rads(Si).
3. Based on characterization, hold time (t_H) of 0ns can be assumed if data setup time (t_{SU2}) is ≥ 10 ns. This is guaranteed, but not tested.

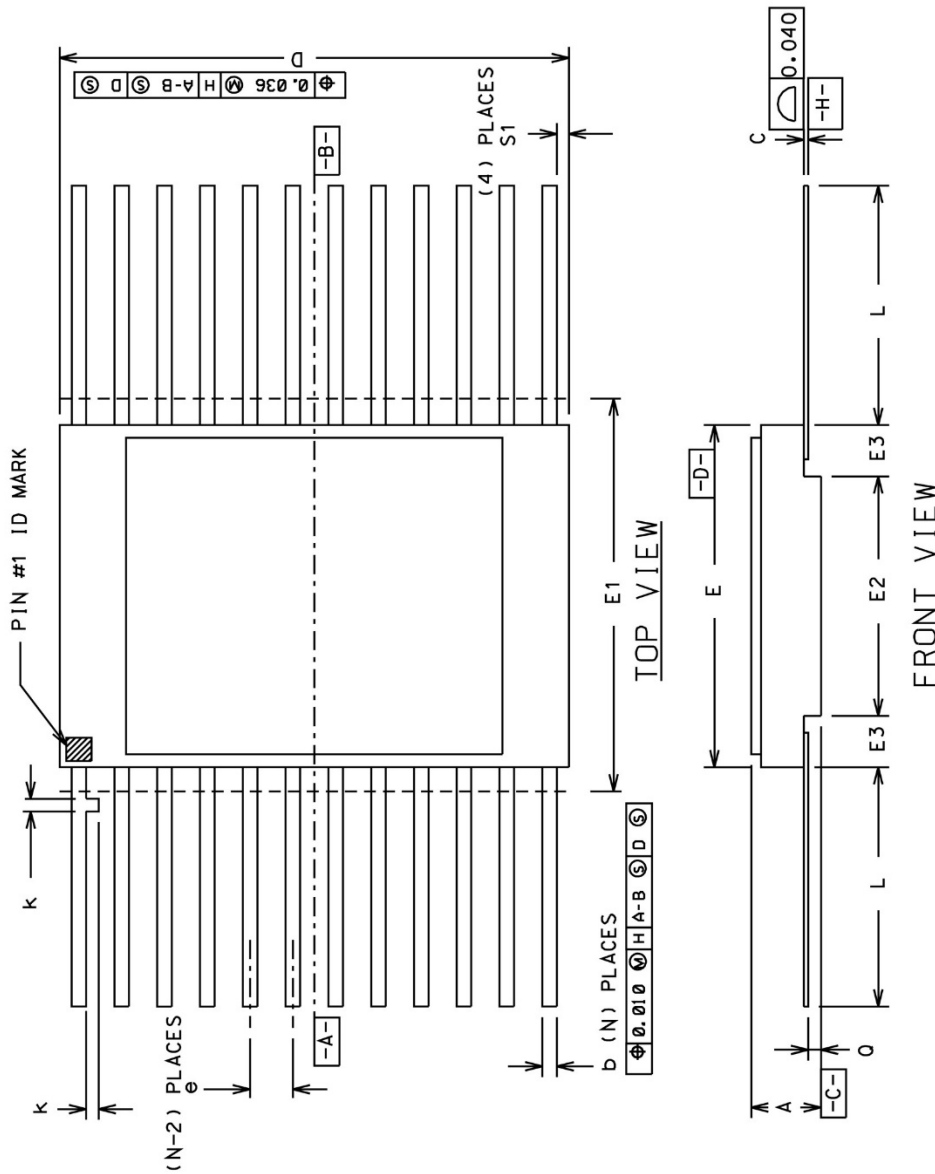
Packaging

Side-Braced Packages



PKG CONFIG	LEAD COUNT	MIL-STD-1835 DWG CONF C	DIMENSION SYMBOLS														
			A	b	b2	c	D	E	e	eA	L	O	S1	S2	ooo	bbb	ccc
-01	14	D-1	0.200	0.026	0.065	0.018	0.785	0.310	0.100	0.300	0.200	0.060	0.005	0.005	0.015	0.030	0.010
			---	0.014	0.045	0.008	---	0.220	BSC	BSC	0.125	0.015	0.005	---	---	---	---
-02	16	D-2	0.200	0.026	0.065	0.018	0.840	0.310	0.100	0.300	0.200	0.060	0.005	0.005	0.015	0.030	0.010
			---	0.014	0.045	0.008	---	0.220	BSC	BSC	0.125	0.015	0.005	---	---	---	---
-03	20	D-8	0.200	0.026	0.065	0.018	1.060	0.310	0.100	0.300	0.200	0.070	0.005	0.005	0.015	0.030	0.010
			---	0.014	0.045	0.008	---	0.220	BSC	BSC	0.125	0.015	0.005	---	---	---	---

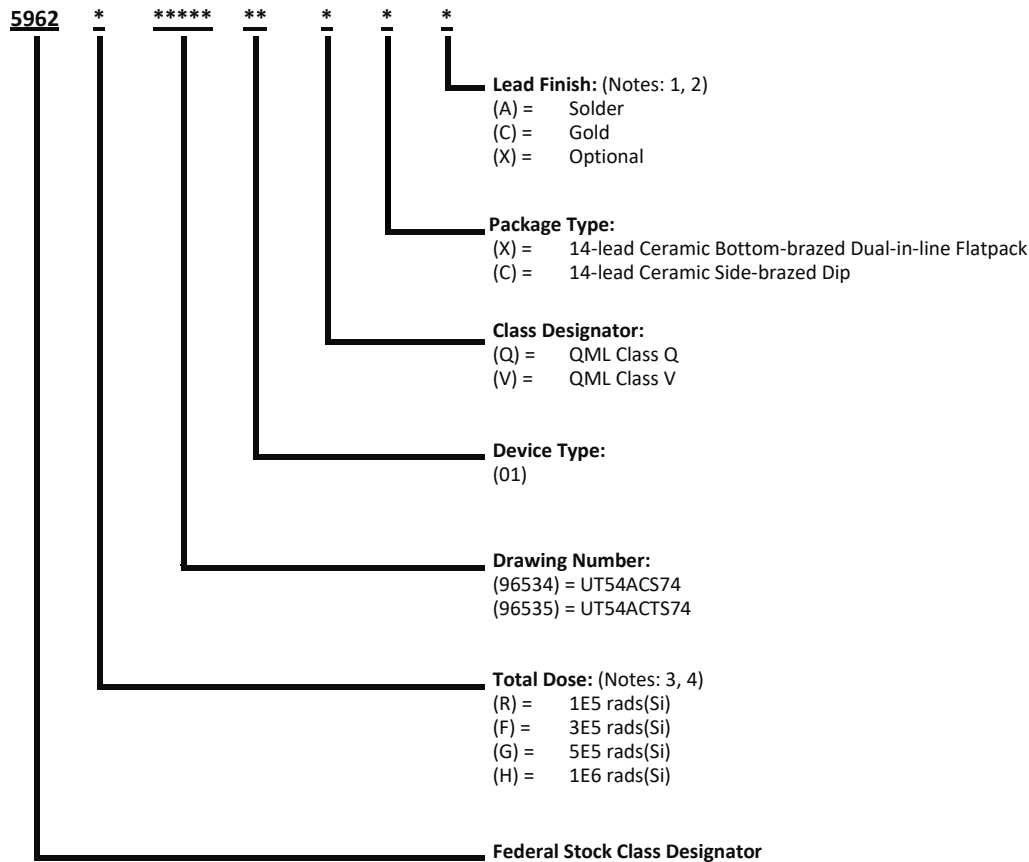
Flatpack Packages



PKG CONFIG	LEAD COUNT	MIL-STD 1835 DWG CONF B	DIMENSION SYMBOLS												
			A	b	c	D	E	E1	E2	E3	e	k	L	Q	S1
-03	14	F-2A	0.115	0.022	0.009	0.390	0.260	0.290	---	---	0.050	0.015	0.370	0.045	---
			0.045	0.015	0.004	---	0.235	---	0.130	BSC	0.008	0.270	0.026	0.005	
-04	16	F-5A	0.115	0.022	0.009	0.440	0.285	0.315	---	---	0.050	0.015	0.370	0.045	---
			0.045	0.015	0.004	---	0.245	---	0.130	BSC	0.008	0.250	0.026	0.005	
-05	20	F-9A	0.115	0.022	0.009	0.540	0.300	0.330	---	---	0.050	0.015	0.370	0.045	---
			0.045	0.015	0.004	---	0.245	---	0.130	BSC	0.008	0.250	0.026	0.000	

Ordering Information

UT54ACS74/UT54ACTS74 SMD Part Number Ordering Information



Notes:

1. Lead finish (A,C, or X) must be specified.
2. If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening. For prototype inquiries, contact factory.
4. Device type 02 is only offered with a TID tolerance guarantee of 3E5 rads(Si) or 1E6 rads(Si) and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A and section 3.11.2. Device type 03 is only offered with a TID tolerance guarantee of 1E5 rads(Si), 3E5 rads(Si), and 5E5 rads(Si), and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A.

Revision History

Date	Revision #	Author	Change Description	Page #

Datasheet Definitions

	Definition
Advanced Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet is subject to change . Specifications can be TBD and the part package and pinout are not final .
Preliminary Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

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