FRONTGRADE

APPLICATION NOTE

UT81ND512G8-Memory-Controller-IP-Compatibility

6/15/2023

Version #: 1.0.0

Features/ Capabilities	IntelliProp	Arasan	Siglead	Phison	Cadence	Comments
Webpage		https://www.arasan.com/products/nand-flash/onfi-4-1/	https://siglead.com/eng/product/ip/nand.php	https://www.phison.com/en/solutions/enterprise	https://ip.cadence.com/ipportfolio/ip-portfolio-overview/memory-ip/nandflash/nand-flash-controller	
ONFI Level	3.2 and 4.0	ONFI 3.2, 4.0 and 4.1			ONFI 4.x (excluding EZ-NAND), ONFI 3.x, and Toggle 2	
Transaction Speed					1200MT/s	
Density/LUNs Supported	266MT/s NV-DDR2 mode 5	NV-DDR2: 400MHz NV-DDR3: 600MHz				
ECC Support	128 total NAND targets	1Tb limit			BCH	
Page Size	BCH	For SLC Flash, Hamming Code is being used for 1 bit error correction and 2 bit error detection. BCH Code, capable of up to 32-Bit error correction, is used for MLC and TLC Flash devices	BCH		256B to 16kB	
Data Integrity Support (Wear Leveling, Bad Block Management, Garbage Collection, etc)		Page Size – 2KB, 4KB, 8KB, 16KB	2 to 16K Bytes			
Source Format (Verilog/VHDL)			Bad Block Management, Wear Leveling (Dynamic/Static), Garbage Collection, etc., can also be provided		Verilog	
Open / Encrypted Source	Verilog	Verilog	Verilog			

Features/ Capabilities	IntelliProp	Arasan	Siglead	Phison	Cadence	Comments
Target Platform (Xilinx/Intel/ASIC)	Encrypted				No specific FPGAs called out	
Supported Interfaces	Xilinx/Intel	No specific FPGAs called out	Xilinx, Altera, Lattice			
	NV-DDR, DDR2, Toggle 2.0	NV-DDR, DDR2, DDR3		Appears to be a hardware controller; Don't know if IP is an offering	Support for multi-LUN modes; give the impression that TLC parts are supported only in SLC mode	

Features/ Capabilities	Xilinx	Boyuan	Marvell	Hyperstone	Comments
Webpage	https://www.xilinx.com/products/intellectual-property/1fod2wk.html	http://www.bjbytech.com/index_en.html	https://www.marvell.com/products/storage/ssd/technologies.html	https://www.hyperstone.com/en/SiliconIP-Core-NAND-FlashController-1376.html	
ONFI Level	3.2 and 4.0	ONFI 2/3/4			
Transaction Speed					
Density/LUNs Supported	128 total NAND targets				
ECC Support	BCH	BCH and LDPC	No specific info listed		
Page Size		2KB, 4KB, 8KB and 16KB			
Data Integrity Support (Wear Leveling, Bad Block Management, Garbage Collection, etc)					
Source Format (Verilog/VHDL)	Verilog	Verilog			
Open / Encrypted Source					
Target Platform (Xilinx/Intel/ASIC)	No specific FPGAs called out	No specific FPGAs called out			

Features/ Capabilities	Xilinx	Boyuan	Marvell	Hyperstone	Comments
Supported Interfaces	NV-DDR, DDR2, Toggle 2.0				
			Appears to be a hardware controller; Don't know if IP is an offering		