FRONTGRADE

APPLICATION NOTE

UT700

Enable the External Memory Mapping
UT700 LEON 3FT

11/21/2019
Version #: 1.0.3

Table 1: Cross Reference of Applicable Products

Product Name	Manufacturer Part Number	SMD #	Device Type	Internal PIC Number
UT700 LEON	UT700	5962-13238	Memory Controller	WQ03

1.0 Overview

This application note explains the external memory mapping of the UT700 LEON 3FT SPARCÔ Processor with particular emphasis on the relationship between the memory space shared between SRAM and SDRAM. We also explain how to use the Memory Configuration Registers 2 (**MCFG2**, refer to **Chapter 3** of the UT700 Functional Manual) to configure and associate the memories select pins to the different memory bank sizes.

With this information, the system designers can precisely design an optimized memory subsystem they need.

2.0 Memory Map Overview

Table 2 shows the UT700 addressable external memory space.

Table 2: Memory Map Overview

Memory Area	Memory Range	Memory Chip Select Pins
PROM	0x0000_0000-0x0FFF_FFFF	$\overline{\text{ROM[0]}}$
PROM	0x1000_0000-0x1FFF_FFFF	$\overline{\text{ROM[1]}}$
I/O	0x2000_0000-0x2FFF_FFFF	$\overline{\text{IOS}}$
Reserved	0x3000_0000-0x3FFF_FFFF	N/A
SRAM/SDRAM	0x4000_0000-0x7FFF_FFFF	$\overline{\text{RAMS[4: 0]}}$/$\overline{\text{SDCS[1: 0]}}$

Note: PROM size is fixed at 256MB; use only **$\overline{\text{ROMS [0]}}$**.

The memory space is logically partitioned into three regions: the PROM, the memory mapped I/O, and the SRAM/SDRAM. The PROM and memory mapped I/O chip select pins always decode the same address space. For the shared SRAM/SDRAM space, address decoding depends upon how the designer configures the **MCFG2. Section 3.0** describes the SRAM and SDRAM valid configurations.

3.0 SRAM and SDRAM Bank Configuration Options

SRAM and SDRAM share a 1GB memory space starting from address 0x4000_0000 to 0x7FFF_FFFF. The designer may choose to implement a system that uses SRAM only, SDRAM only, or a combination of the two using the **MCFG2.**

The **DE** and **SI** bits in **MCFG2** determine which type of memory will be interfaced to the UT700; for example, deasserts **DE** enables SRAM only while asserts **SI** enables SDRAM only. Several different examples of memory interface options are shown in the following subsections. The **SZ** field in the **MCFG2** determines the size of each SRAM bank except for the area selected by $\overline{\textbf{RAMS [4]}}$, which always maps to the upper 512MB when SDRAM is not used. Accesses using $\overline{\textbf{RAMS [4]}}$ can be stretched using the **BRDY** input pin (To increase the number of wait states). SDRAM bank sizes are determined by **DZ** and **DS** (see **MCFG2**).

The following tables show several different memory configuration options based upon the states of **SI** and **DE**, and the SRAM bank size, **SZ,** or the SDRAM bank size, **DZ**. For more information, refer to **Chapter 3** of the UT700 Functional Manual available at https://www.frontgrade.com.

4.0 SRAM Memory Map

Table 3 shows the use case of SRAM only in the shared SRAM/SDRAM space.

Table 3 shows the relationship between the $\overline{\textbf{RAMS [4:0]}}$ select pins and the different memory blank sizes. For example, in the use case of 64MB bank size, each **RAMS [X] (X** = 0 to 3) selects a 64 MB memory blank while the RAMS [4] selects the upper 512MB blank memory space. Address space from 0x5000_0000 to 0x5FFF_FFFF are unused. Table 4 shows how to configure the different blank sizes using the **MCFG2** as shown in **Table 3.**

Note: Each SRAM chip select ($\overline{\textbf{RAMS [3:0]}}$) selects an address range that is dependent on the **MCFG2** setting.

Table 3: SRAM Memory Map

Start Address	SRAM Bank Sizes		
	256MB	128MB	64MB
0x7C00_0000	$\overline{\text{RAMS[4]}}$ (512 MB)	$\overline{\text{RAMS[4]}}$ (512 MB)	$\overline{\text{RAMS[4]}}$ (512 MB)
0x7800_0000			
0x7400_0000			
0x7000_0000			
0x6C00_0000			
0x6800_0000			
0x6400_0000			
0x6000_0000			
0x5C00_0000	$\overline{\text{RAMS[1]}}$	$\overline{\text{RAMS[3]}}$	UNUSED
0x5800_0000			
0x5400_0000		$\overline{\text{RAMS[2]}}$	
0x5000_0000			
0x4C00_0000	$\overline{\text{RAMS[0]}}$	$\overline{\text{RAMS[1]}}$	$\overline{\text{RAMS[3]}}$
0x4800_0000			$\overline{\text{RAMS[2]}}$
0x4400_0000		$\overline{\text{RAMS[0]}}$	$\overline{\text{RAMS[1]}}$
0x4000_0000			$\overline{\text{RAMS[0]}}$

4.1.1 SRAM Bank Configuration

Table 4 shows how to configure the different memory blank sizes using the **MCFG2,** refer to **Chapter 3** of the UT700 Functional Manual for more information.

Table 4: SRAM Memory Configuration

SRAM Bank Size	SI	DE	SZ
256MB	0	0	1111b
128MB	0	0	1110b
64MB	0	0	1101b

4.2 SRAM and SDRAM Memory Map

Table 5 shows the use case of both the SRAM and SDRAM in the shared SRAM/SDRAM space. Address decoding is similar to the use case of SRAM only, except that the upper 512MB of address space is used exclusively for SDRAM. In this configuration, **$\overline{\text{RAMS}}$ [4]** is never used. **Table 6** indicates the register field settings for the three bank size options shown in **Table 5**.

Note: Use SDCS [0] for SDRAM bank select only.

Table 5: SRAM and SDRAM Memory Map

<table>
<tr><th rowspan="2">Start Address</th><th colspan="3">SRAM Bank Sizes</th></tr>
<tr><th>256MB</th><th>128MB</th><th>64MB</th></tr>
<tr><td>0x7C00_0000</td><td rowspan="8">$\overline{\text{SDCS}}$[0]
(SDRAM)</td><td rowspan="8">$\overline{\text{SDCS}}$[0]
(SDRAM)</td><td rowspan="8">$\overline{\text{SDCS}}$[0]
(SDRAM)</td></tr>
<tr><td>0x7800_0000</td></tr>
<tr><td>0x7400_0000</td></tr>
<tr><td>0x7000_0000</td></tr>
<tr><td>0x6C00_0000</td></tr>
<tr><td>0x6800_0000</td></tr>
<tr><td>0x6400_0000</td></tr>
<tr><td>0x6000_0000</td></tr>
<tr><td>0x5C00_0000</td><td rowspan="4">$\overline{\text{RAMS}}$[1]</td><td>$\overline{\text{RAMS}}$[3]</td><td rowspan="4">UNUSED</td></tr>
<tr><td>0x5800_0000</td></tr>
<tr><td>0x5400_0000</td><td>$\overline{\text{RAMS}}$[2]</td></tr>
<tr><td>0x5000_0000</td></tr>
<tr><td>0x4C00_0000</td><td rowspan="4">$\overline{\text{RAMS}}$[0]</td><td rowspan="2">$\overline{\text{RAMS}}$[1]</td><td>$\overline{\text{RAMS}}$[3]</td></tr>
<tr><td>0x4800_0000</td><td>$\overline{\text{RAMS}}$[2]</td></tr>
<tr><td>0x4400_0000</td><td rowspan="2">$\overline{\text{RAMS}}$[0]</td><td>$\overline{\text{RAMS}}$[1]</td></tr>
<tr><td>0x4000_0000</td><td>$\overline{\text{RAMS}}$[0]</td></tr>
</table>

4.2.1 SRAM and SDRAM Bank Configuration

Table 6 shows how to configure the different memory blank sizes using the MCFG2.

Table 6: SRAM and SDRAM Memory Configuration

SRAM Bank Size	SI	DE	SZ	DZ
256MB	0	1	1111b	111b
128MB	0	1	1110b	111b
64MB	0	1	1101b	111b

For different SDRAM bank sizes, refer to Chapter 3 the UT700 Functional Manual for more information.

4.3 SDRAM Memory Map

Table 7 shows the use case of SDRAM only in the shared SRAM/SDRAM space. $\overline{\text{SDCS}}$ [0] selects the lower 512MB of address space and **$\overline{\text{SDCS}}$ [1]** selects the upper 512MB of address space. **Table 8** indicates the register field settings for the case shown in **Table 7.**

Table 7: SDRAM Memory Map

Start Address	SDRAM Bank Sizes 512MB
0x7C00_0000	$\overline{\text{SDCS}}$[1]
0x7800_0000	
0x7400_0000	
0x7000_0000	
0x6C00_0000	
0x6800_0000	
0x6400_0000	
0x6000_0000	
0x5C00_0000	$\overline{\text{SDCS}}$[0]
0x5800_0000	
0x5400_0000	
0x5000_0000	
0x4C00_0000	
0x4800_0000	
0x4400_0000	
0x4000_0000	

4.3.1 SDRAM Bank Configuration

Table 8 shows a 512MB SDRAM blank size configuration using the **MCFG2.**

Table 8: SDRAM Memory Configuration

SDRAM Bank Size	SI	DE	SZ	DZ
512MB	1	1	X	111B

For different SDRAM bank sizes, refer to **Chapter 3** of the UT700 Functional Manual for more information.

Note: For any SDRAM bank size smaller than 512MB, use **$\overline{\text{SDCS}}$ [0]** only.

4.3.2 UT700 and SDRAM Interface Pinout

Table 9 shows the correct pins correction between the UT700 and the SDRAM. Other pin connection between the UT700 and the SDRAM that are obvious are not shown here.

Table 9: UT700 and SDRAM Interface Pinout Assignment

UT700	SDRAM	Remarks
ADDR[14:2]	A[12:0]	Row and column addresses
ADDR[16:15]	BA[1:0]	Internal bank select
SDCS[1:0]	CSB,CSA	Chip select **(Table 7)** CSA and CSB from different SDRAM devices mapped on the upper and lower external banks

5.0 Summary and Conclusion

After going through this AN, the reader should know how to configure the different memory bank sizes using the **MCFG2** register and how to associate the memory select pins to the respective memory banks.

For more information about our UT700 LEON 3FT/SPARC™ V8 Microprocessor and other products please visit our website, https://www.frontgrade.com or email us at https://www.frontgrade.com/contact-us.

Revision History

Date	Revision #	Author	Change Description	Page #
03/12/2017	1.0.0	MTS	Initial Release	
07/31/2017	1.0.1	MTS	Table 1	2
09/27/2017	1.0.2	MTS	Table 5	5
11/21/2019	1.0.3	MTS	Table 1, I/O address	2