FRONTGRADE

APPLICATION NOTE

Creating Certus-NX-RT Project in Radiant Software

3/18/2022

Version #: 1.0.0

Table 1: Cross Reference of Applicable Products

Product Name	Manufacturer Part Number	Device Type
Lattice Certus-NX-RT FPGA	UT24C407	RL01

1.0 Overview

This document details the process of creating a **Certus-NX-RT** FPGA project using the **Lattice Radiant** software tools. For the purposes of this document, create a project named **led_brightness** and configure the **Radiant** tools to include all the source modules required for a successful build. Using this template, projects are created using (a) the preferred application source directory structures and (b) the directory structure for the **Radiant**-supplied files. **Figure 1** shows the block diagram of the design, with the switches SW[3:0] controlling the duty cycle to the pwm output, which controls the brightness to LED[0]; LED[7:4] are used as heartbeat of the system.

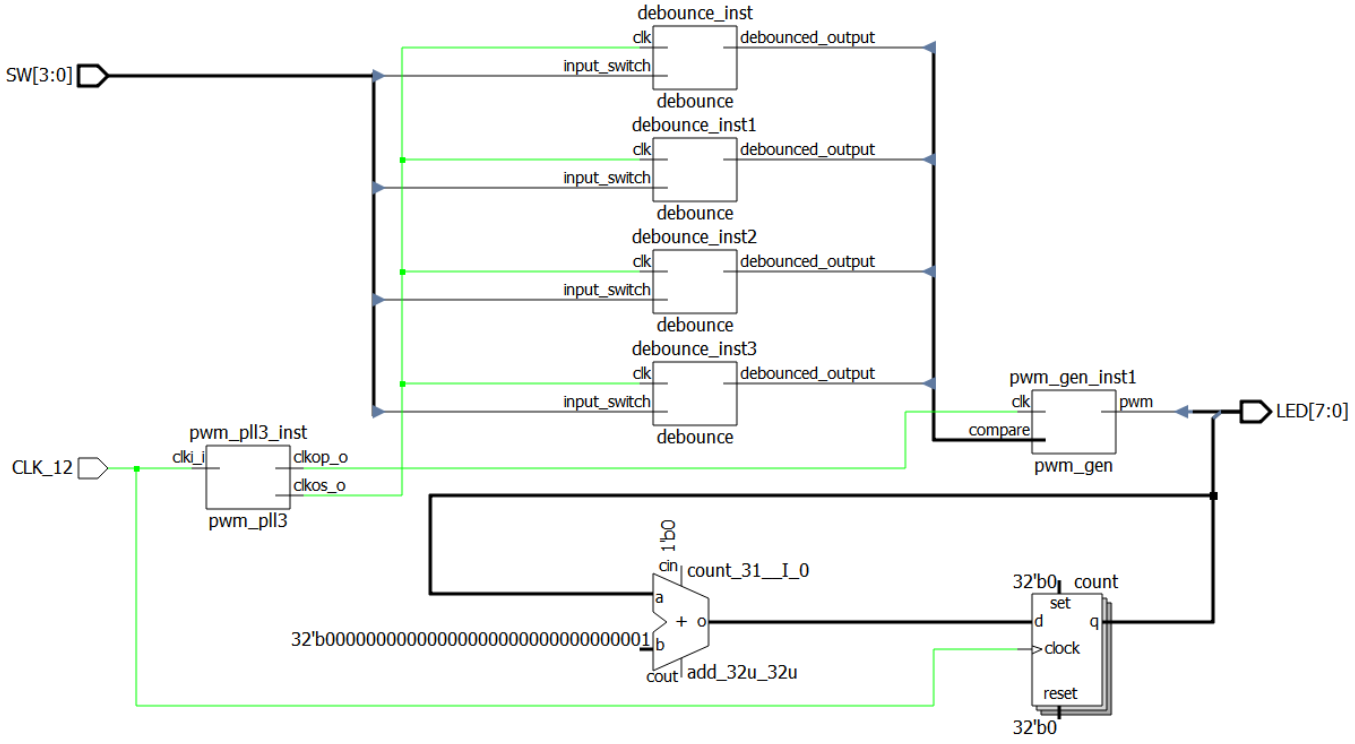

Figure 1: An Example Netlist View

2.0 Creating a Design Project with Radiant Software

1. Download **CreatingRadiantProject.zip** from frontgrade.com.
2. Launch **Radiant Software**
3. From the File menu, select **New > Project….**
4. Specify the project name as **led_brightness,** navigate to the **location** of your choice and click **Next,** see **Figure 2.**

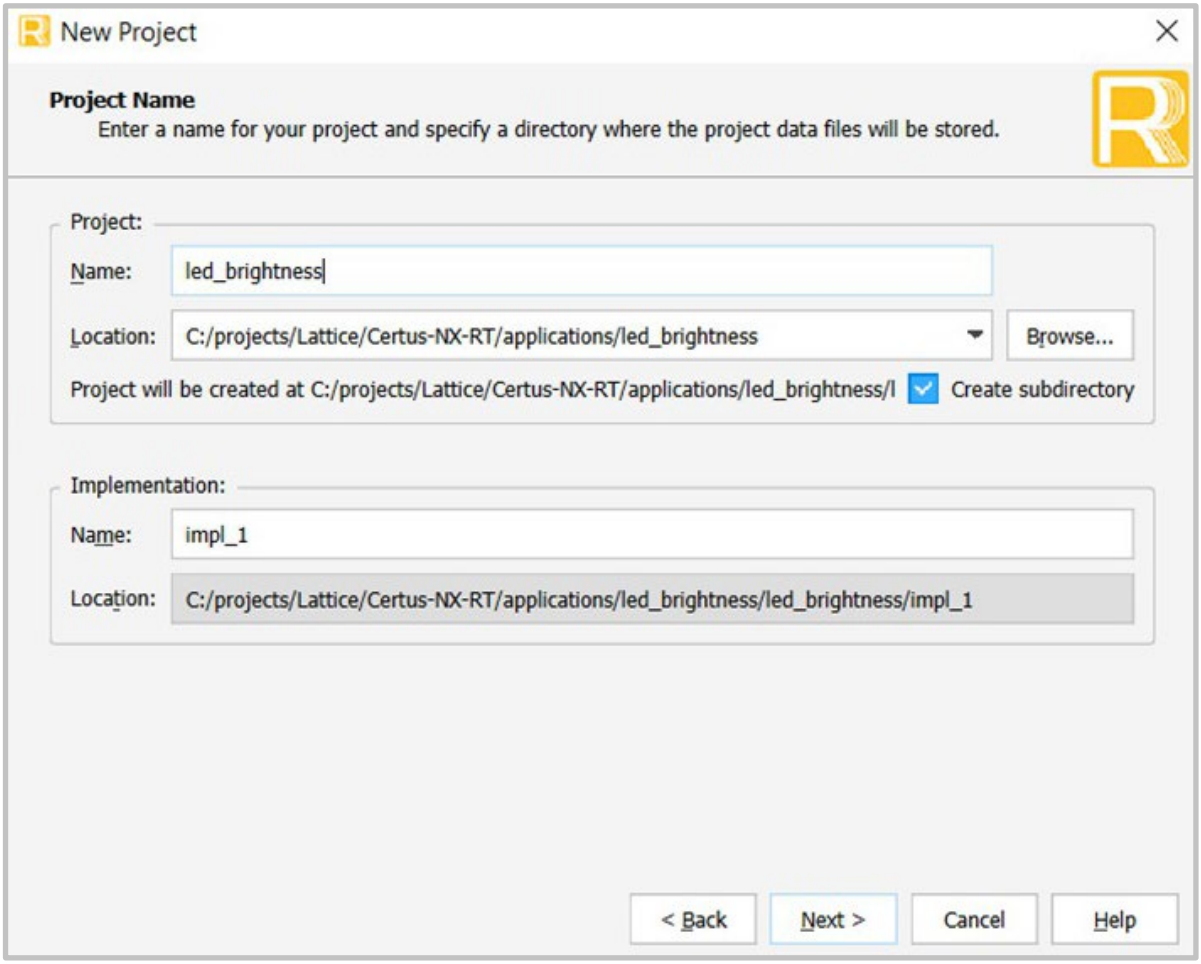

Figure 2: Creating a Radiant Design Project

5. Select **Add Source…** and click **Open,** see **Figure 3** and **Figure 4,** click Next.

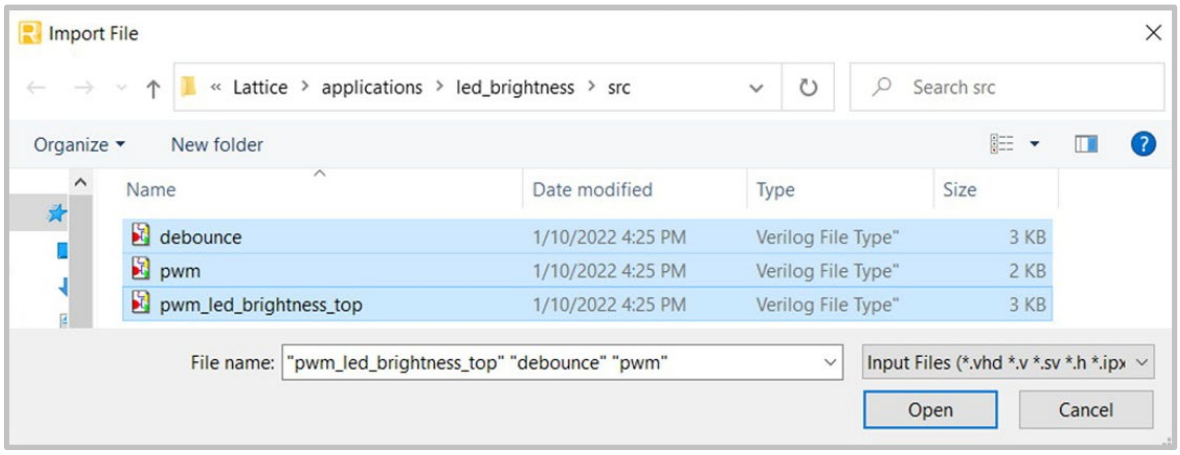

Figure 3: Selecting Sources

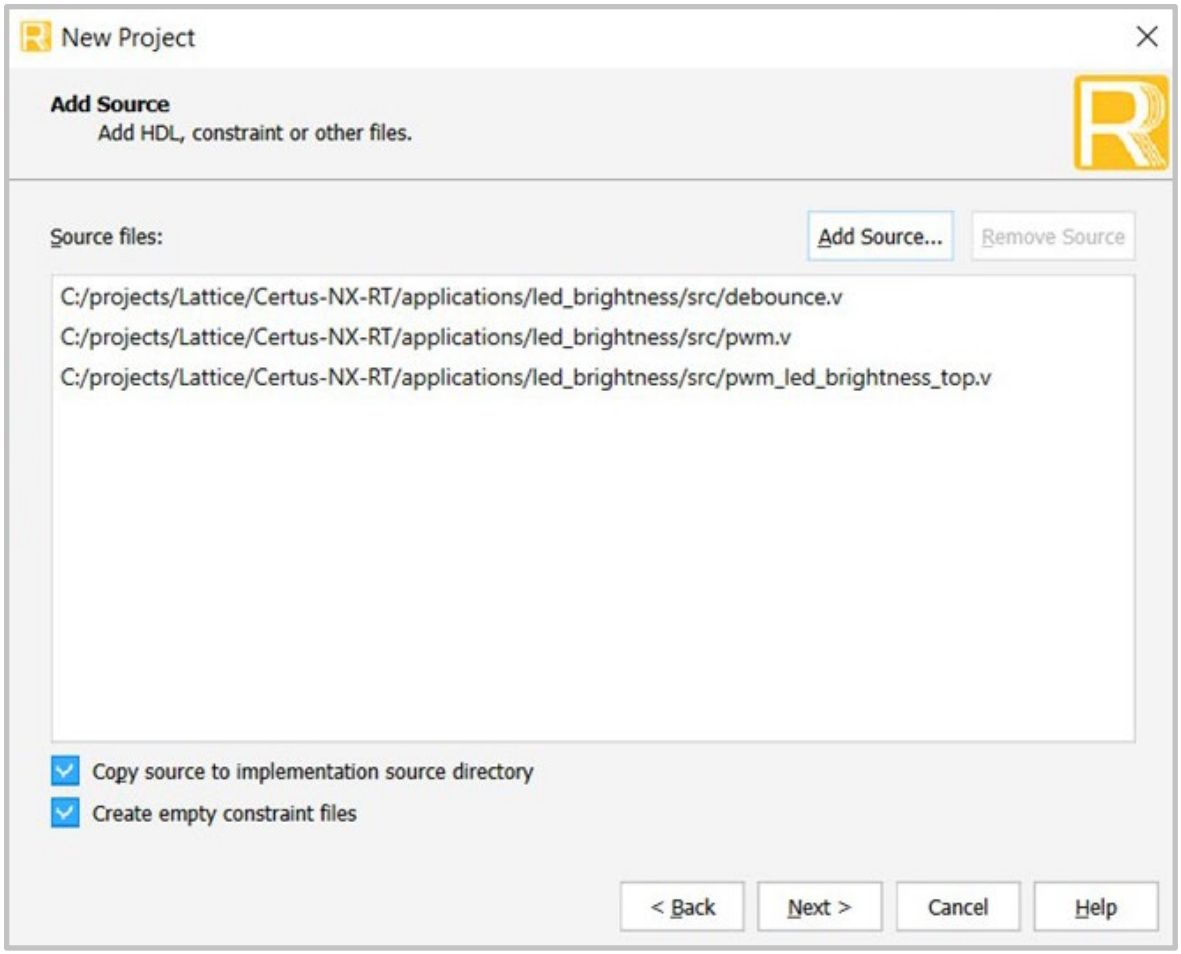

Figure 4: Adding Sources

6. Select the appropriate device, click **Next** and choose **Lattice LSE;** click **Next** and **Finish,** see **Figure 5.**

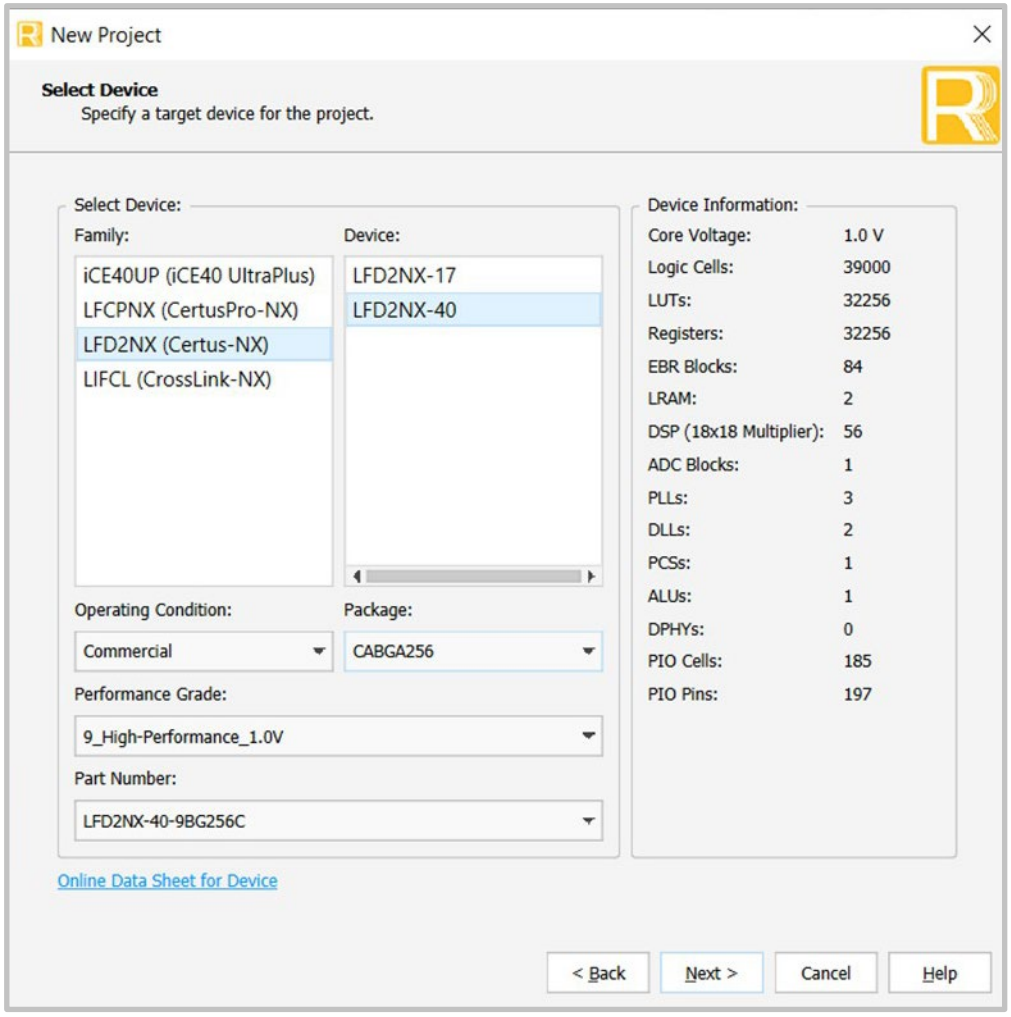

Figure 5: Selecting the FPGA Device

Figure 6: Selecting the Synthesis Tool

7. The initial project with the provided files should look like **Figure 7.**

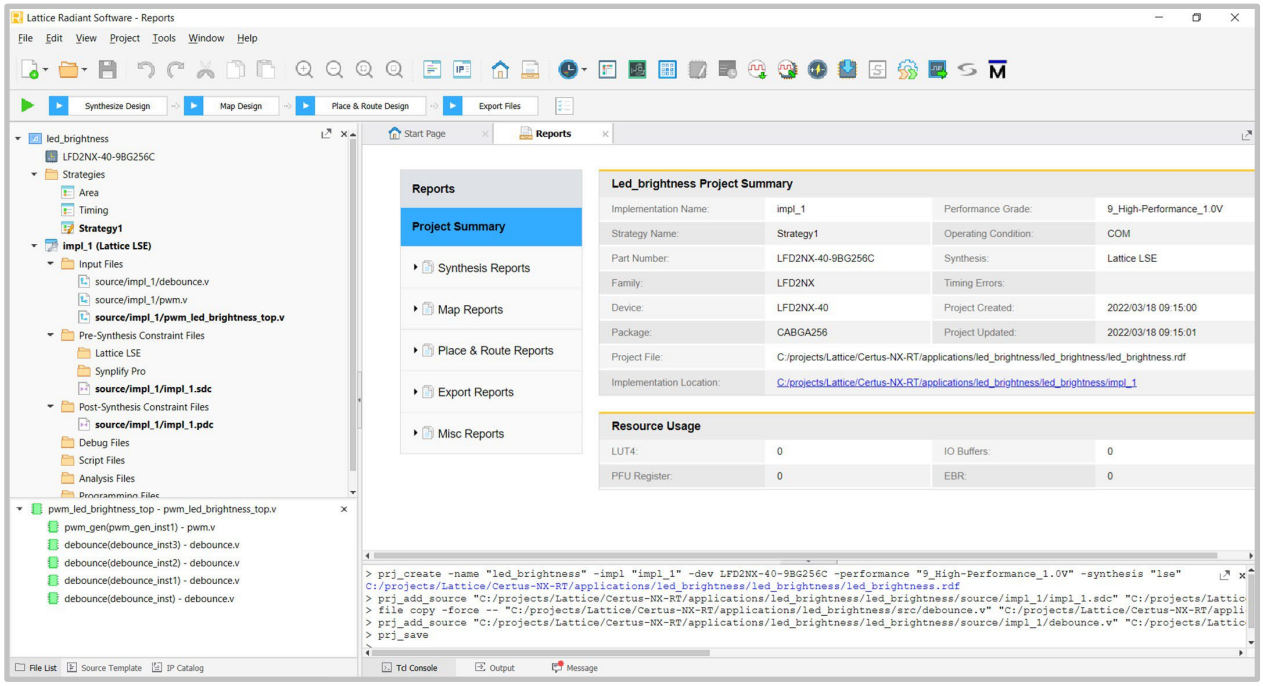

Figure 7: An Example of an Initial Project

8. From **IP Catalog,** add a **PLL** with the options below and name it **pwm_pll3,** see **Figure 8** and **Figure 9.**

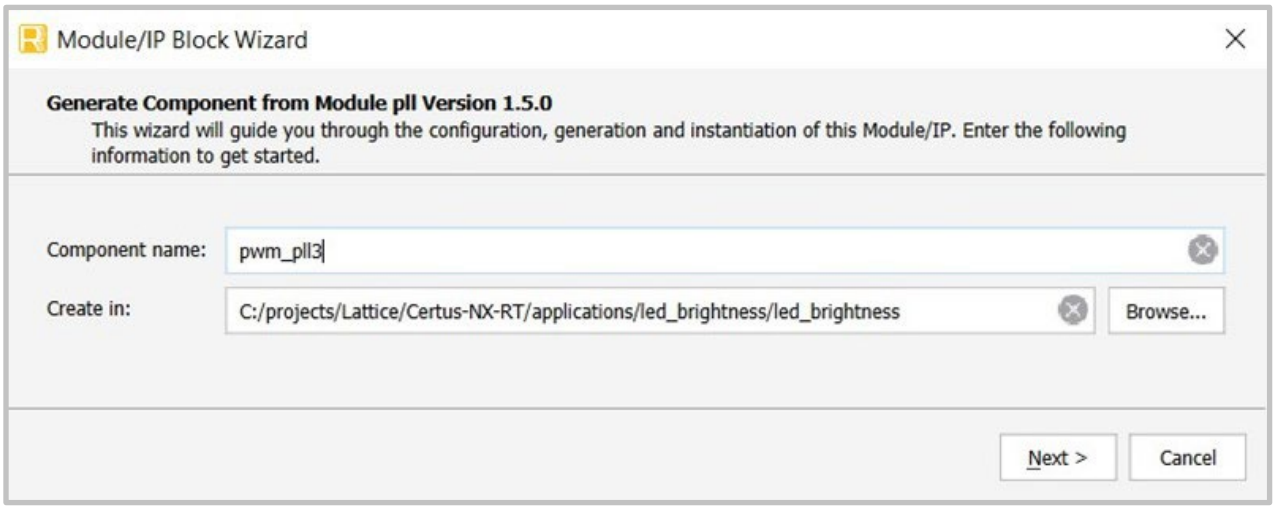

Figure 8: Opening the IP Catalog

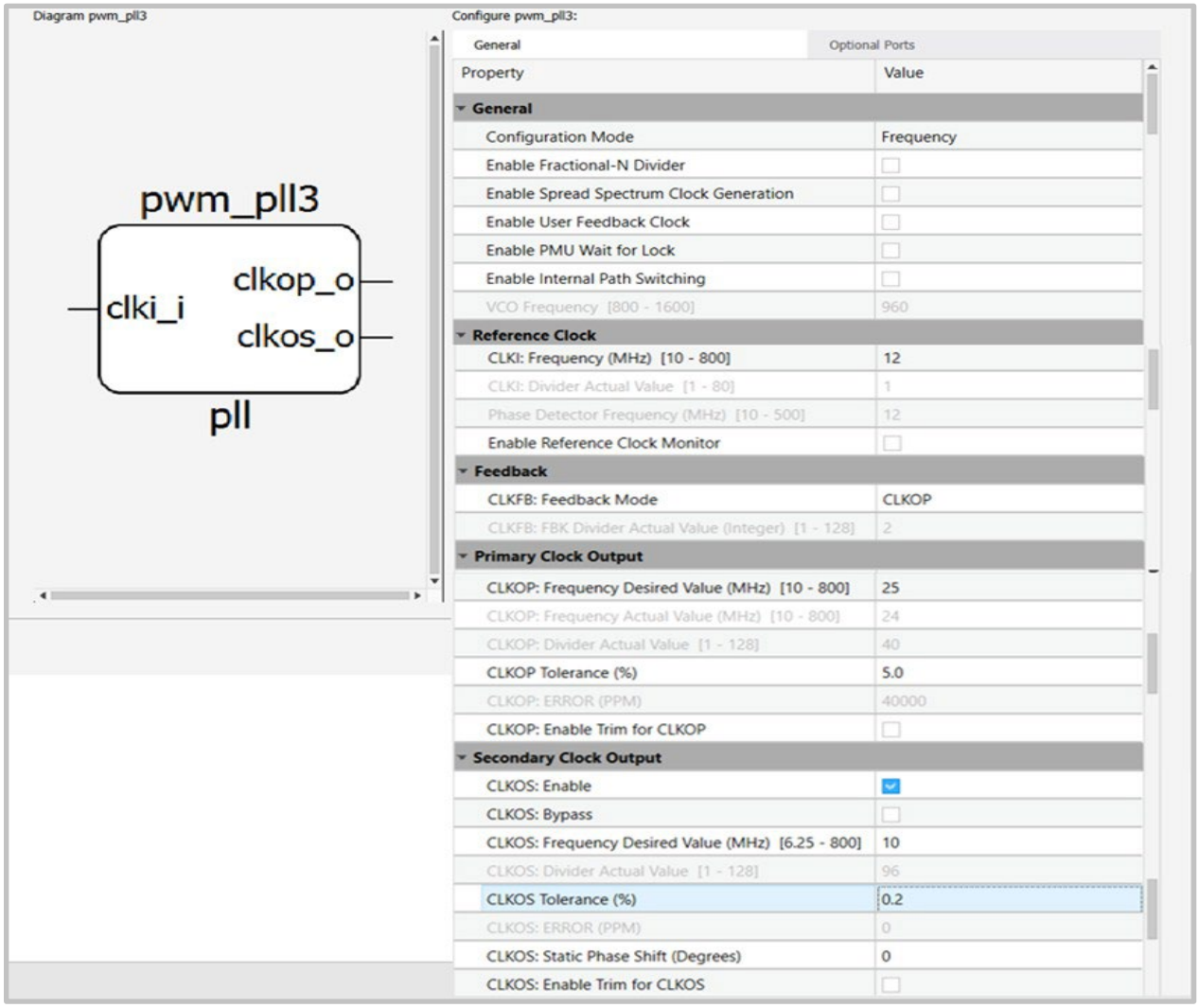

Figure 9: Adding a PLL from the IP Catalog

9. Once the **PLL** is created, it is added to the project files, see **Figure 10.**

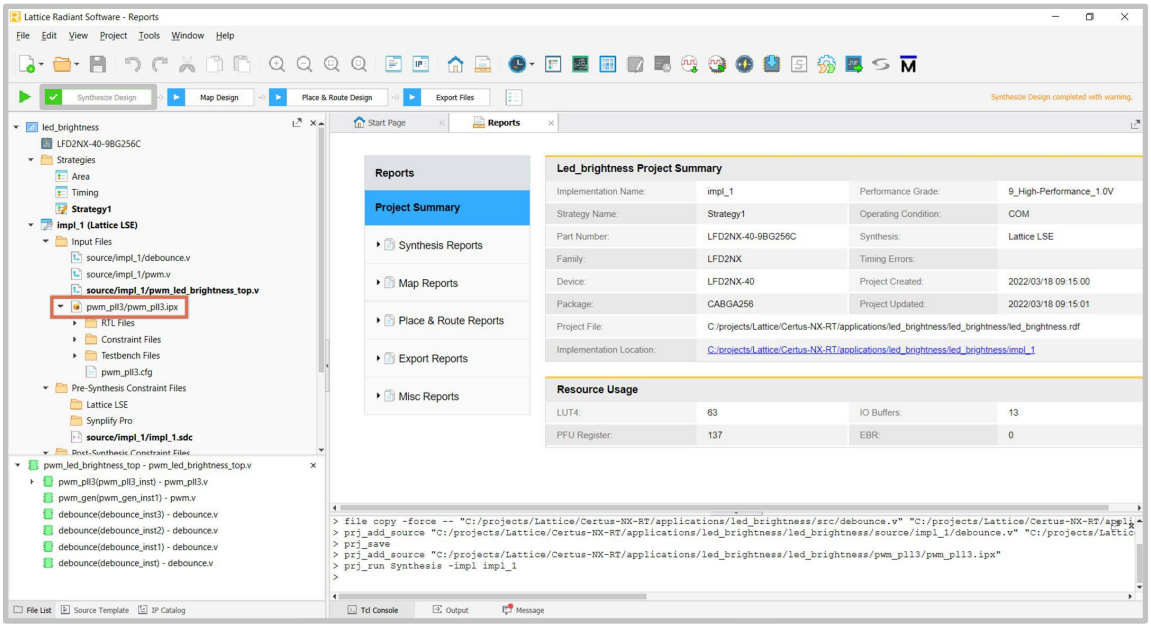

Figure 10: Looking at the Recently Added PLL IP

3.0 Compile Design using Radiant Software

3.1 Set Top Level File

10. From the **Project** menu, select **Active Implementation > Set Top-Level Unit…** and set **pwm_led_brightness_top.v** as the top level file, see **Figure 11.**

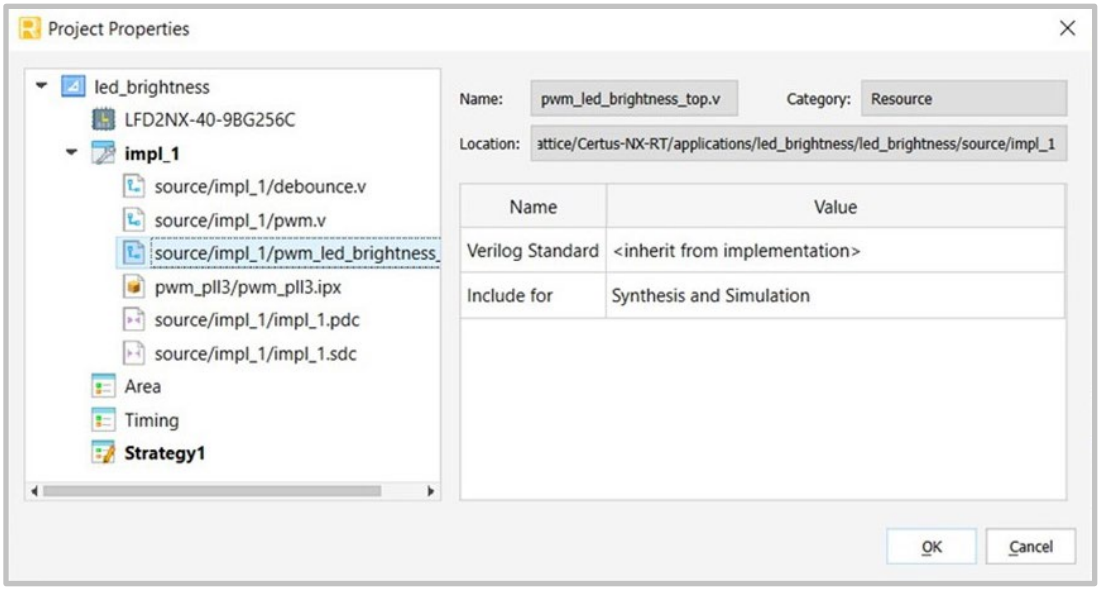

Figure 11: Setting a Top Level File

3.2 Synthesize Design

11. Synthesize the design by clicking on the **Synthesize Design** arrow, see **Figure 12.**

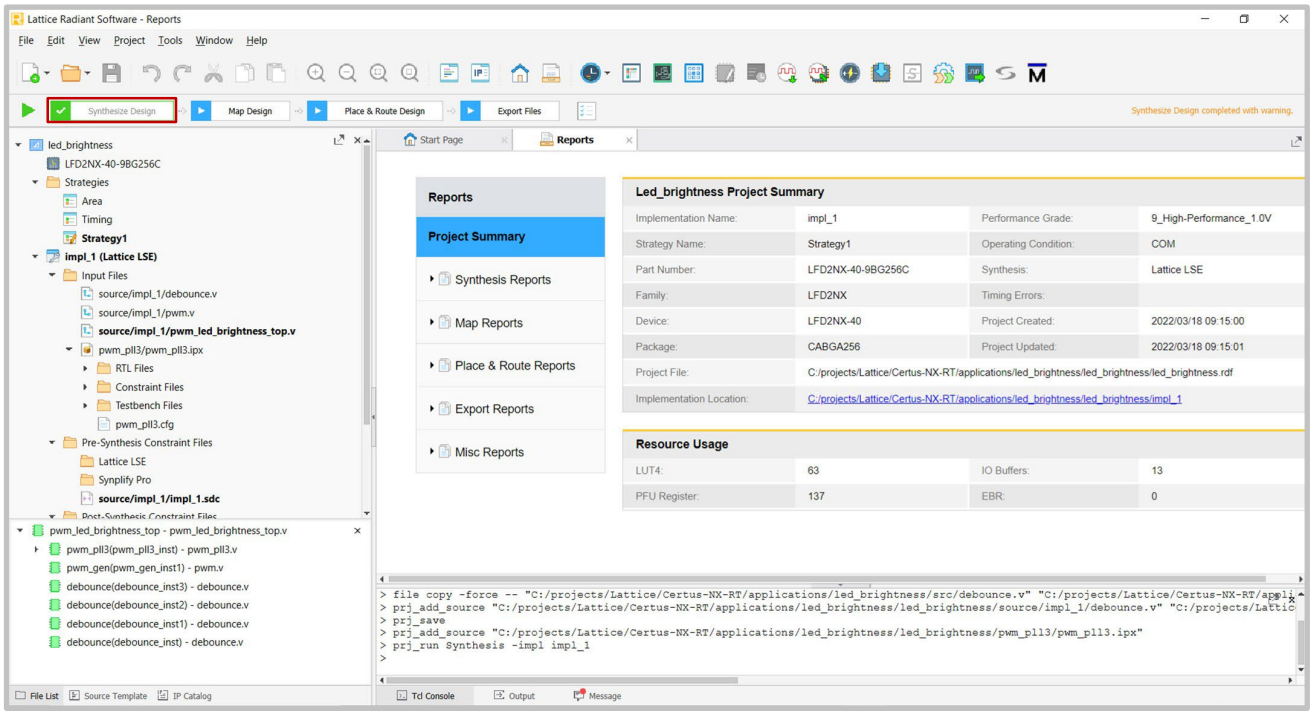

Figure 12: Synthesizing the Design

3.3 Pin Assignment (Device Constraint Editor)

12. Once the design has been synthesized, assign the pin numbers to their respective signals, see **Figure 13.**

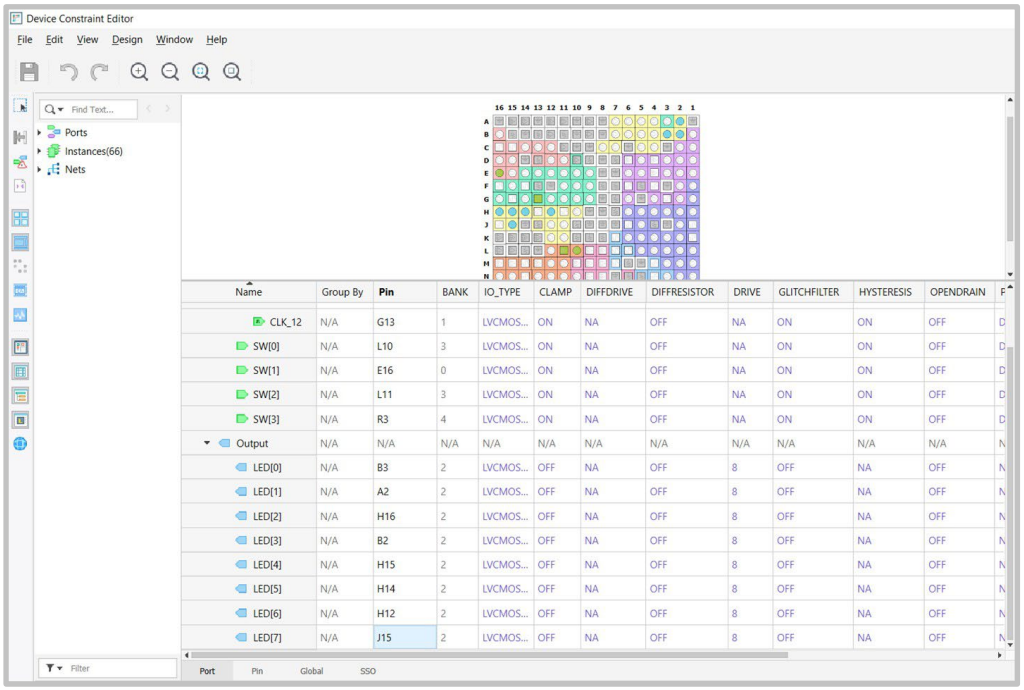

Figure 13: Performing Pin Assignment

3.4 Compile Design

13. Compile the design by clicking on the **Run All** arrow, see **Figure 14.**

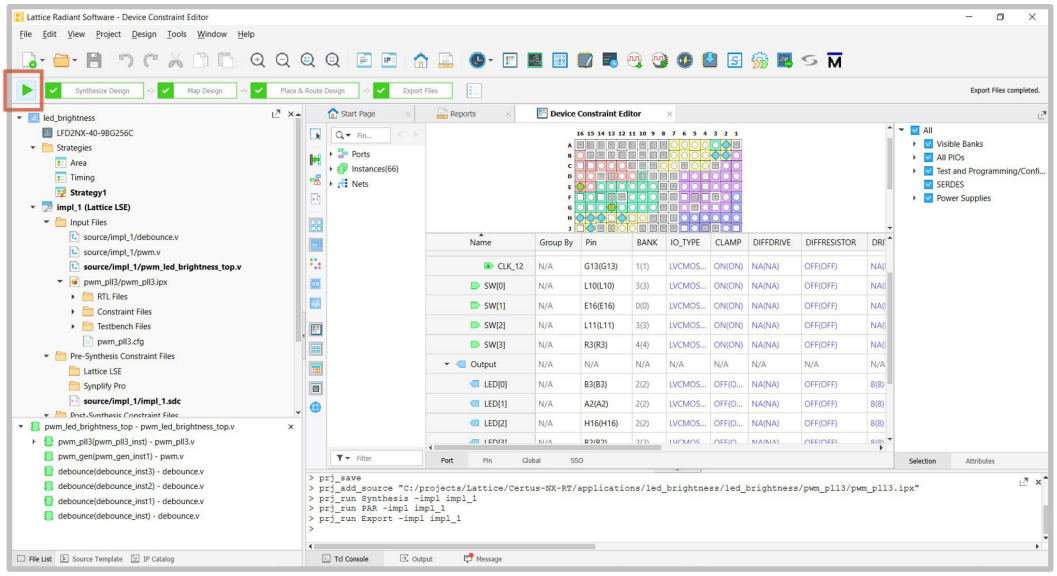

Figure 14: Compiling the Design

3.4 Simulate Design

14. From the **Tools** menu, select **Simulation Wizard** and click **Next,** see **Figure 15.**

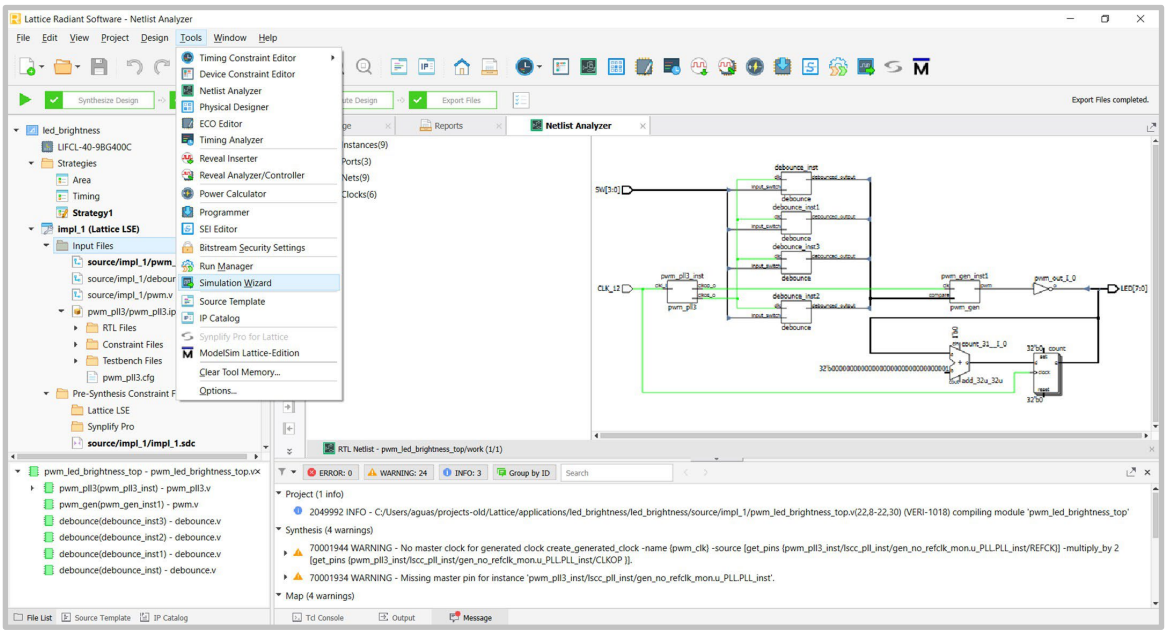

Figure 15: Simulating the Design

15. Name the project **led_brightness_sim** and click **Next,** see **Figure 16.**

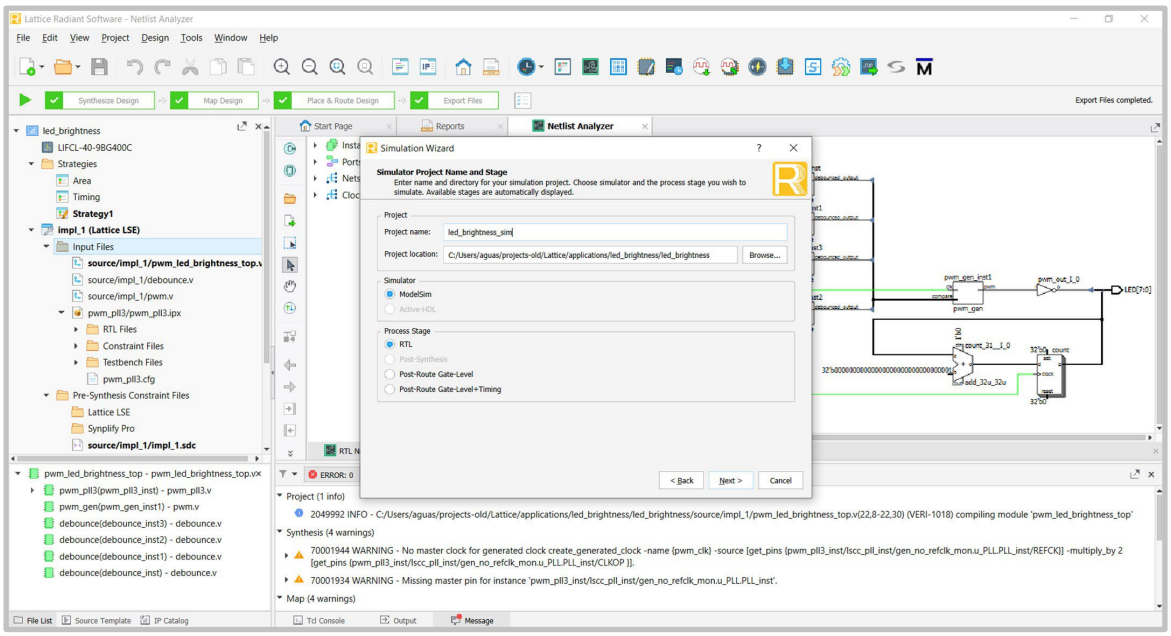

Figure 16: Naming the Simulation

16. When finished, **ModelSim** will open and run the simulation, see **Figure 17.**

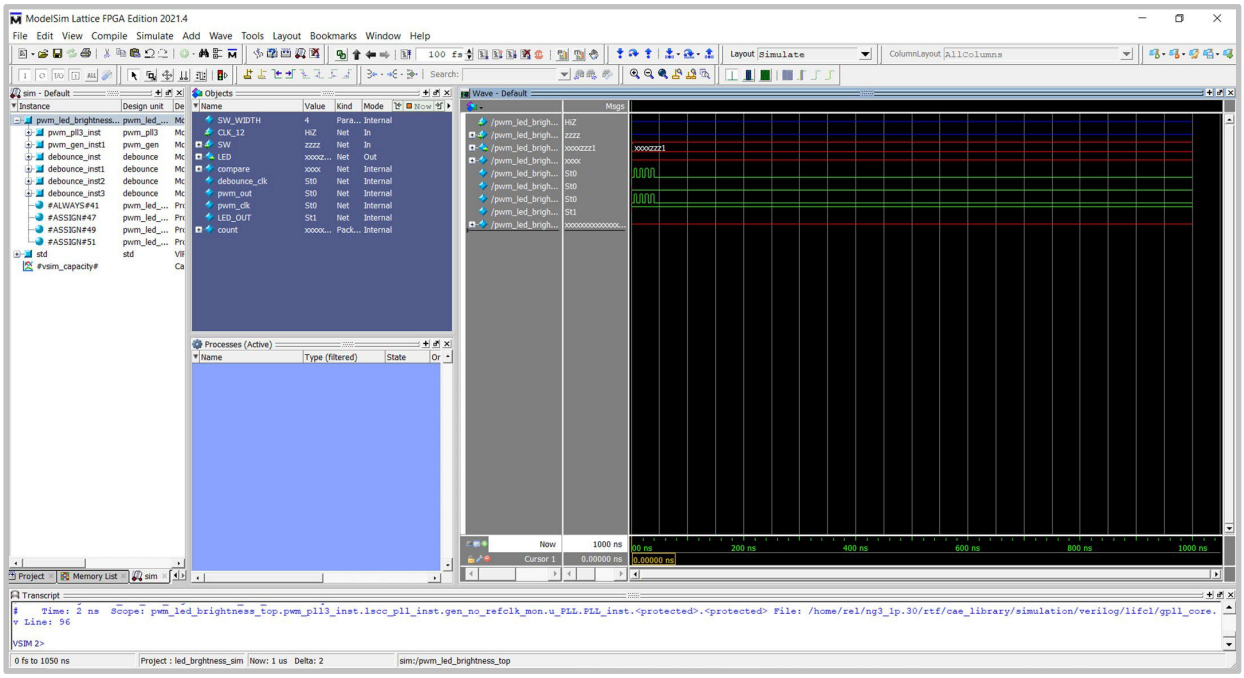

Figure 17: The ModelSim Simulation Wave View

4.0 Program the Device with Radiant Programmer

17. From the **Tools** menu, select **Programmer** and a new window opens, see **Figure 18.** Once the cable is detected and settings are set, program the device by clicking the Program Device icon  , **Figure 18.**

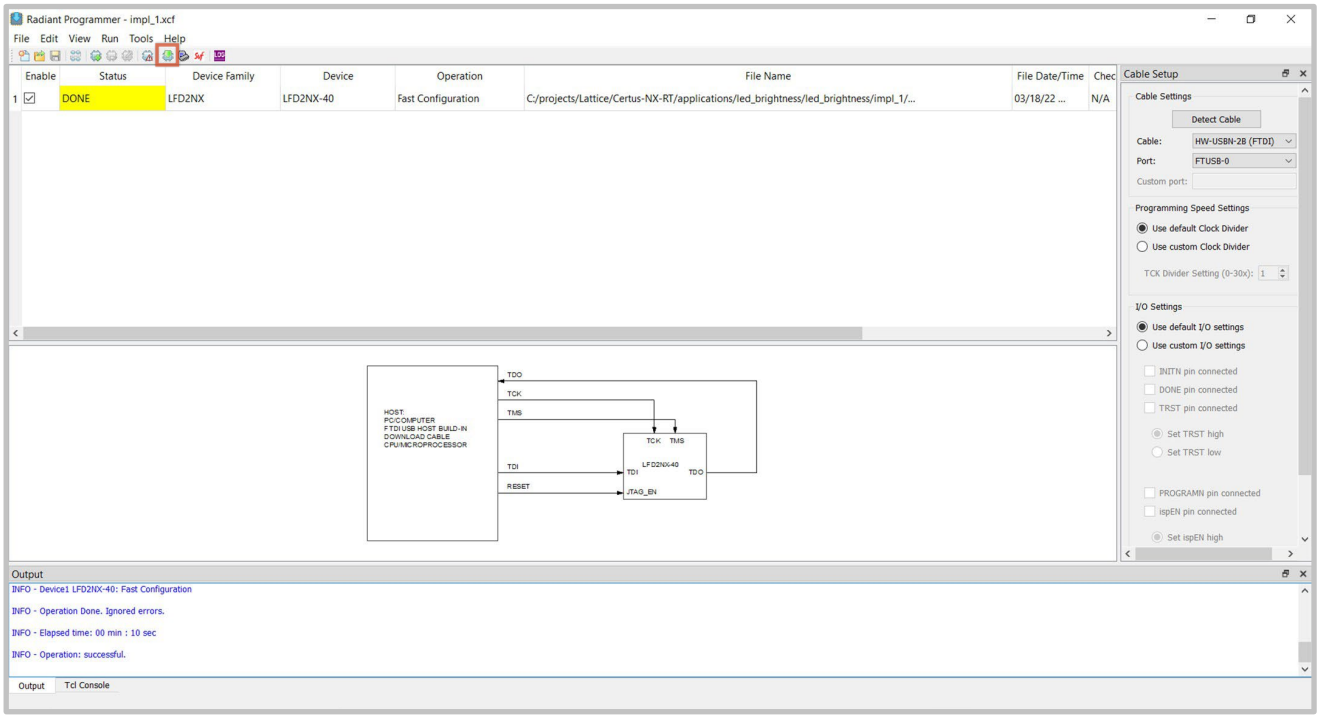

Figure 18: Programming the FPGA

Revision History

Date	Revision #	Author	Change Description	Page #
3/18/2022	1.0.0	JA	Initial Release.	

Datasheet Definitions

	Definition
Advanced Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the **datasheet is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final.**
Preliminary Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.