### **APPLICATION NOTE**

**Creating Certus-NX-RT SoC Project in Radiant Software** 

> 4/8/2022 Version #: 1.0.0

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#### **Table 1: Cross Reference of Applicable Products**

Product Name	Manufacturer Part Number	Device Type
Certus-NX-RT	UT24C407	FPGA

#### **1.0 Overview**

This document details the process of creating a **Certus-NX-RT SoC FPGA** project using the **Lattice Propel** software tools. For the purposes of this document, create a project named **Hello\_World\_SoC** and **Hello\_World** using **Propel Build** tools to include all the source modules required for a successful build. Using this template, projects are created using (a) the preferred application source directory structures and (b) the directory structure for the Radiant-supplied files. **Figure 1** shows the block diagram of the design.



Figure 1: Example Design Block Diagram

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#### 2.0 Lattice Propel: Software Development Tools

Lattice provides software development tools for system-on-chip (SoC) designs: Lattice Propel Development Suite, which provides software build tools (SBT) for Eclipse. Eclipse is an integrated development environment (IDE) featuring:

- Creating and debugging applications.
- Using Lattice SBT, allows automatic creation of a board support package (BSP) for the given SoC.
- The BSP allows communication to the different peripherals in the SoC.
- The Lattice SBT automatically creates the make files for building the application.
- Lattice Propel for Eclipse software development kit (SDK) provides:
  - a GUI for code editing, compiling, and debugging using the GNU toolchain, which provides the compiler, assembler and linker, see Figure 2.

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Figure 2: Lattice Propel

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#### 3.0 Lattice Propel Builder

Lattice Propel Builder allows for easy design of a SoC by simply dragging and dropping modules into a schematic view. Propel Builder provides:

- **GUI** for designing a **SoC** system.
- Generate the **SoC** design.
- Integrate the SoC design with Lattice Radiant Software.



Figure 3: Lattice Propel Builder

### 4.0 Lattice Propel: Creating a SoC Design Project



1. Launch Lattice Propel and choose the workspace directory, see Figure 4.

📀 Lattice Propel Launcher		×
Select a directory as workspace		
Lattice Propel uses the workspace director	ry to store its preferences and developme	ent artifacts.
(c)		
Workspace: C\projects\Lattice\workspace	× .	Browse
Use this as the default and do not ask a	gain	
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Figure 4: Setting a Workspsace Directory

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2. From the **Project Explorer**, select **Create a new Lattice SoC Design Project**, see **Figure 5**.



Figure 5: Creating a new Propel Design Project

3. Specify the project name as Hello\_World\_CNX\_SoC and click Finish, see Figure 6.

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Figure 6: Hello World Project Setup

4. After clicking Finish, Propel Builder opens with a view of the template SoC design, see Figure 7.

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Figure 7: Default Propel Builder View

5. Design View shows all the components for creating the template SoC design, see Figure 8.



Figure 8: Design View of SoC Design

6. For the provided template, the default **SoC** design is sufficient; hit **Generate C** to generate the different files used by the software, see **Figure 9**.

NOTE: Depending on the Synthesis tool used, the PLL frequencies might need to be adjusted to compile the design.



Figure 9: Generating the Default SoC Design

 Back in Lattice Propel, create a software project. From the File menu, select New > Lattice C/C++ Project and click Next, see Figure 10.

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Project type: C					v
System information					
Device Family LFD2NX	CPU Name riscv_mc	Instance Name cpu0_inst			
3		< Back	jext >	Einish .	Cancel

Figure 10: Creating a New Software Project

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8. Name the project Hello\_World and accept all defaults, click Next and Finish, see Figure 11.

/C++ Project			1	4
Create C/C++ project of selected type				
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> 🕞 Shared Library				
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Figure 11: Naming the Project

9. The template creates the source code for the "Hello World" project and the BSP based on the RISC-V SoC design, see Figure 12.

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> 😂 bsp	54 extern struct uart instance *g_stdio_uart;		
> 🖻 main.c	<pre>55 g_stdio_uart = &amp;uart_core_uart;</pre>		
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Figure 12: Generated Hello World Project

10. To build the "Hello World" project, right click on **Hello\_World\_CNX** and select **Build Project.** The compiler builds the project and generates the necessary output files, see **Figure 13.** 



Figure 13: Building the Software Project

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- 11. Back in the **Project Explorer**, highlight **Hello\_World\_CNX\_SoC** and select run **Lattice Radiant**, **Lattice Radiant Software** opens in a new window, see **Figure 14**.



Figure 14: Opening the Project in Lattice Radiant

**APPLICATION NOTE** 

Q.▼ Find Text	Name	Group By	Pin	BANK	IO_TYPE	CLAMP	DIFFDRIVE	DIFFRESISTOR	DRIVE	GLITCHFILTER	HYST '	All
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	led_o[3]	N/A	B2(B2)	2(2)	LVCMOS	ON(ON)	NA(NA)	OFF(OFF)	8(8)	ON(ON)	ON(O	
	led_o[4]	N/A	H15(H15)	2(2)	LVCMOS	ON(ON)	NA(NA)	OFF(OFF)	8(8)	ON(ON)	ON(O	
	led_o[5]	N/A	H14(H14)	2(2)	LVCMOS	ON(ON)	NA(NA)	OFF(OFF)	8(8)	ON(ON)	ON(O	
	led_o[6]	N/A	H12(H12)	2(2)	LVCMOS	ON(ON)	NA(NA)	OFF(OFF)	8(8)	ON(ON)	ON(O	
	led_o[7]	N/A	J15(J15)	2(2)	LVCMOS	ON(ON)	NA(NA)	OFF(OFF)	8(8)	ON(ON)	ON(O	

**12.** Before compiling the entire design, assign the proper pin number to the signals based on the eval board schematics, see **Figure 15.** 

Figure 15: Pin Assignment

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- - 13. Compile the design by clicking on the Run All arrow, see Figure 16.

Lattice Radiant Software - Reports					- 0 ×		
<u>File Edit View Project Tools Window H</u> elp							
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Synthesize Design 🗠 🗸 Map Design 🗠 🗸 F	lace & Route Design 🗠 🖌 Export Files				Export Files completed.		
▼ Mello_World_SoC	🗙 🏠 Start Page 🛛 🚔 Reports	× Device Constraint Edi	tor ×		Ŀ		
LFD2NX-40-8BG256C							
Strategies	Reports	Hello_World_SoC Proje	ct Summary				
1 Timing		Implementation Name:	impl_1	Performance Grade:	8_High-Performance_1.0V		
5 Strategy1	Project Summary	Strategy Name:	Strategy1	Operating Condition:	COM		
impl_1 (Lattice LSE)     Input Files	Sunthania Banarta	Part Number:	LFD2NX-40-8BG256C	Synthesis:	Lattice LSE		
Hello_World_SoC/Hello_World_SoC.v	, Synthesis Reports	Family:	LFD2NX	Timing Errors:	Place & Route, 0 (setup), 0 (hole		
Pre-Synthesis Constraint Files	Map Reports	Device:	LFD2NX-40	Project Created:	2022/04/08 04:41:52		
Synplify Pro		Package:	CABGA256	Project Updated:	2022/04/08 04:41:53		
💌 🚞 Post-Synthesis Constraint Files	<ul> <li>Place &amp; Route Reports</li> </ul>	Project File:	C:/projects/Lattice/Certus-NX-	RT/workspace/Hello_World_SoC/Hel	llo_World_SoC.rdf		
Debug Files	Export Reports	Implementation Location:	C:/projects/Lattice/Certus-NX-	RT/workspace/Hello_World_SoC/imp	1		
Analysis Files	Misc Reports	Resource Usage					
Programming Files     Autor files		LUT4:	4358	IO Buffers:	11		
been source/ mpr_1.cci		PFU Register:	2073	EBR:	18		
Hello World SoC - Hello World SoC.y	×* 4						
uart0(uart0_inst) - uart0.v	▼ ▼ 🔕 ERROR: 0 🔺 WARNING: 331 0 INFO	: 157 Group by ID Search	< >		∠" ×		
Bysmem0(pysmem0,inst) - sysmem0.v     Map (4 warnings)     Mop (4 warnings)     Mop (4 warnings)     Mop (4 warnings)     A S101063 WARNING - IO instance secured_instance_80_104 is not connected to any port, it is ignored.     P gipto(pjoto)_inst - piptoV     Export (2 info)							
<ul> <li>If cpu0(cpu0_inst) - cpu0.v</li> <li>If apb0(apb0_inst) - apb0.v</li> <li>If ahbl2apb0(ahbl2apb0 inst) - ahbl2apb0.v</li> </ul>	35400233 INFO - This design contains sec	ured IP object(s), so output file Hello_	World_SoC_impl_1_vo.vo has been enco	rypted.			
File List      Source Template      IP Catalog	🗔 Tcl Console 🔄 Output 📑 Mer	ssage					

Figure 16: Compiling the Lattice Radiant Design

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#### **5.0 Program the Device with Radiant Programmer**

From the **Tools** menu, select **Programmer** and a new window opens.

Once the cable is detected and settings are set correctly, program the device by clicking the **Program Device** icon, see **Figure 17.** 

Radiant Pro	ogrammer - imp	ol_1.xcf *								- 0	×
Pile Edit V		is Help									
Enable	Status	Device Family	Device	Operation	File Name	File Date/Time	Checksum	USERCODE	Cable Setup		đΧ
1 🗹 🛛 🛛 РАЗ	ss	LFD2NX	LFD2NX-40	Erase, Program, Verify	C:/projects/Lattice/Certus-NX-RT/workspace/Hello_World_SoC/impl_1/	04/08/22	N/A	0x00000000	Cable Setting	IS	^
										Detect Cable	
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									Port:	FTUSB-0	~
									Custom port		
									Programming	Speed Settings	
									O Use defa	ult Clock Divider	
									Use cust	om Clock Divider	
									TCK Divide	r Setting (0-30x):	10 🗘
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									Use defa	ult I/O settings	
				-	DO				O Use cust	om I/O settings	
					TCK				INITN I	oin connected	
				PC/COMPUTER	Th/S				DONE (	oin connected	
				DOWNLOAD CABLE CPU/MCROPROCESSOR	TCK TMS				TRST r	oin connected	
					TDI LFD2N640 TDO				) Set T	RST high	
				_	RESET JTAG_EN_COLXCESEVE SD				🔘 Set 7	RST low	
					CLK (CS DI DO SPI Serial Flash				PROGR	AMN pin connected	(      ,
									<		>
Output											đΧ
Disabling											^
Verifying											
INFO - Execution	time: 00 min : 14	sec									
INFO - Elapsed t	ime: 00 min : 19 s	ec									
INFO - Operation	1: successful.										
	ACT 11010 (1987)										~
Output Td	Console										

Figure 17: Programming the FPGA

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Back in Lattice Propel, right click on the "	Hello World"	project and choose <b>I</b>	Debug Configuration;	eave the default
configurations and click debug, see Figure	e <b>18.</b>			

S Debug Configurations			- 0 ×				
Create, manage, and run configurations			Ś				
· · · · · · · · · · · · · · · · · · ·	Name: Hello_World_CNX Debug						
	🗋 Main 📄 CableConn 🎋 Debugger 🕨 Startup 🦆 Sou	urce 🔲 Common 😹 SVD Path					
C/C++ Application	Project:						
C/C++ Attach to Application	Hello World CNX						
C/C++ Remote Application	C/C++ Application:						
Cü C/C++ Unit	Debug/Hello World CNX eff						
GDB Hardware Debugging     GDB OpenOCD Debugging		<u>V</u> ariables Searc <u>h</u> P	roject B <u>r</u> owse				
Hello_World_CNX Debug	Build (if required) before launching						
Launch Group (Deprecated)	Build Configuration: Select Automatically		~				
	O Enable auto build	<ul> <li>Disable auto build</li> </ul>					
	Use workspace settings	Configure Workspace Settings					
Filter matched 10 of 12 items		Reg	ert Apply Dug Close				

Figure 18: Debug Configurations

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The debugger opens the Debug perspective; set a breakpoint at line 59 to print "Hello RISC-V world from Frontgrade!" message on Tera Term terminal, see Figure 19. Variable values can be seen in the Variables window. As with any other IDE running C code, you can Step Into 3, Step Over 3 and Step Out 3.

<b>^</b>				
workspace - Hello_World_CNX/src/main.c - Lattice Propel				🔟 COM9 - Tera Term VT
Ele Edit Source Refactor Navigate Search Project Run LatticeTools Window Help				File Edit Setup Control Window Help
		▼ ỗ  ▼ \$ <b>\$ \$ \$ \$</b> \$ \$ <b>▼</b> \$ \$ <b>▼</b>   <b>2</b>		
🗱 Debug 🖾 💫 Project Explorer 🛛 🖻 🙀 🔹 🖱 🗖	🖻 main.c 🖾 🕞 utils.h 📄 💽 (gdb[35].proc[42000].thr	eadGroup[i1],gdb[35].proc[42000].C	Sthread[1] 📄 Sys_platform.h	Hello RISC-V world from CAES?
Field_World_CNX Debug [GDB OpenOCD Debugging]	<pre>49 static uint8_t idx = 0;</pre>			
<ul> <li>Hello_World_CNX.elf</li> </ul>	50			
<ul> <li>Pread #1 (Suspended : Signal : 0:Signal 0)</li> </ul>	52 Uart_init(&uart_core_uart, UAKI0_	INST_BASE_ADDR, CPU_FREQUEN	Y, UARIO_INSI_BAUD_RAIE	
main() at main.c:59 0x23a	53 #ifdef LSCC STDIO UART APB			
J openocd.exe	54 extern struct uart_instance *g_st	dio_uart;		
📓 riscv-none-embed-gdb	<pre>55 g_stdio_uart = &amp;uart_core_uart;</pre>			
	56 #endif			
	58 printf("\r\nHello RISC-V world fr	om CAESI\r\n"):		
	259 LED_SET(ALL_OFF);			
	60			
	61 while (true) {			
	63			
	64 if (++idx == LED_COUNT) {			
	65 idx = 0;			
	66 }			
	68 if (BTL STM) {			
	69 delayMS(1);			
	70 } else {			
	<pre>delavMS(500);</pre>			
	Console 22 III Registers Terminal Problems	C Everytables R Debugger Conso	e 🖪 Memoni 🛷 Search	
	Hello World CNX Debug (GDR OpenOCD Debugging) or	executables ag Debugger consc	e o wentory / search	
	(901) mip (/32)			
	(1985) mtohost (/32)			
	(1986) mfromhost (/32)			
	(1987) mreset (/32)			
	(1989) miobase (/32)			
	(3137) cycle (/32)			
	(3138) time (/32)			
	(3139) instret (/32)			
	(3266) timeh (/32)			
	(3267) instreth (/32)			
	(3922) mvendorid (/32)			
	(3923) march1d (/32)			
	(2554) mimbro (125)			
	<			
		Writable Smart	Insert 82 : 33 : 2886	203M of 305M

Figure 19: Debug Perspective

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#### **Revision History**

Date	Revision #	Author	Change Description	Page #
4/8/2022	1.0.0	JA	Initial Release.	

#### **Datasheet Definitions**

	Definition	
Advanced Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the <b>datasheet is subject to change</b> . Specifications can be <b>TBD</b> and the part package and pinout are <b>not final</b> .	
Preliminary Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.	
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.	

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