FRONTGRADE AEROSPACE DATA EXCHANGE PROGRAM TRANSMITTAL PROBLEM ADVISORY 1. TITLE 2. DOCUMENT NUMBER UT24CP1008 CertusProTM-NX-RT FPGA Family: SERDES SPO-2023-PA-0003 functional capability limitation when channel 3 is used and PMA clock divider is set to >=23. DATE (Year, Month, Date) 2023 DECEMBER 13 5. MANUFACTURER POINT OF CONTACT NAME 4. MANUFACTURER NAME AND ADDRESS Jose Betancourt FRONTGRADE TECHNOLOGIES 6. MANUFACTURER POINT OF CONTACT TELEPHONE 4350 CENTENNIAL BOULEVARD COLORADO SPRINGS, COLORADO 80907-3486 719-208-9662 7. MANUFACTURER POINT OF CONTACT EMAIL jose.betancourt@frontgrade.com 8. CAGE CODE 9. LDC START 10. LDC END 11. PRODUCT IDENTIFICATION CODE 12. BASE PART **RL02** 65342 B3112T03 B3112T03 UT24CP1008 13. BLANK 14. SMD NUMBER 15. DEVICE TYPE DESIGNATOR ALL N/A 17. QML LEVEL 16. RHA LEVELS ALL ALL 18. NON QML LEVEL 19. GIDEP NUMBER GB4-PA-2023-0001 ALL

20. PROBLEM DESCRIPTION / DISCUSSION / EFFECT

Frontgrade's UT24CP1008 CertusProTM-NX-RT FPGA is based on wafer/die manufactured by Lattice Semiconductor for their LFCPNX-100 automotive grade devices. The wafer/die is then packaged and qualified under Frontgrade's Space PEM Flow to add the critical space flight assurance and rad-tolerance required for harsh environments.

Lattice Semiconductor has published Product Change Notices (PCN) 01A-23 and 01B-23 indicating that an issue has been identified and documented in the Automotive grade wafer/die currently used in Frontgrade's UT24CP1008 CertusProTM-NX-RT FPGA. Refer to <u>https://www.latticesemi.com/Support/PCN.aspx</u> to download the subject PCN.

The issue identified pertains to SERDES functional capability limitation when using channel 3 and the PMA clock divider is set to >=2.

Block 20 Continued on page 2. 21. ACTION TAKEN / PLANNED

Corrective Actions:

PCNs 01A-23 and 01B-23 are Lattice Semiconductor notices of their intent to utilize an alternate qualified mask set on future versions of the wafer/die.

The use of this alternate qualified mask set will not change form or fit. The alternate qualified mask set will correct the Channel 3 with PMA clock divider >=2 functional capability.

Next Steps:

Frontgrade will use wafer/die utilizing the alternate qualified mask set in future versions and Lot ID of the UT24CP1008 CertusProTM-NX-RT FPGA.

22. DISPOSITIONARY RECOMMENDATION:	CHECK &		CONTACT		REMOVE &		CORRECT &	\boxtimes
	USE AS IS		MANUFACTURER		REPLACE		USE AS SPECIFIED	

20. PROBLEM DESCRIPTION / DISCUSSION / EFFECT (CONTINUED)

Effect:

If you currently use UT24CP1008 and do NOT utilize Channel 3, no further actions are required.

If you USE channel 3 (numbering is 0,1,2,3) and do NOT use PMA clock divider >=2, no further actions are required.

Continue to order the standard ordering part number.

Future UT24CP1008 device product versions/Lot IDs may utilize either of the qualified mask sets.

If you currently use UT24CP1008 AND utilize Channel 3 with PMA clock divider >=2, please contact Frontgrade to determine availability of future Lot ID of the UT24CP1008 with the new mask set.

Table 1 documents the affected part number.

Table 1: Affected Part Number

Plastic package
UT24CP1008RBLA

UT24CP1008 device product versions marked with Lot ID = B3112T03 (shown in diagrams below) are affected by this limitation.

Diagrams 1 and 2 document the packaged UT24CP1008 device and Lot ID identification scheme and marking showing the Lot ID location.

Diagram 1: Device Identification

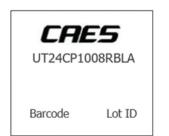


Diagram 2: Device Marking

