## AEROSPACE DATA EXCHANGE PROGRAM TRANSMITTAL



## PRODUCT CHANGE NOTICE

1. TITLE		2. DOCUMENT NUMBER		
RAD-HARD 8-BIT MSI LOGIC WITH SCHMITT TRIGGER INPUTS – NEW SPEC. PARAMETER INPUT TR/TF MAX.		SPO-2018-PCN-0003		
		3. DATE (Year, Month, Date) 2018 NOV 27		
4. MANUFACTURER NAME AND ADDRESS		5. MANUFACTURER POINT OF CONTACT NAME		
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CAES		6. MANUFACTURER POINT OF CONTACT TELEPHONE		
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		Bruce.Massey@cobhamaes.com		
8. CAGE CODE	9. EFFECTIVE DATE	10. PRODUCT IDENTIFICATION CODE	11. BASE PART	
65342	2018, NOV, 27	See Table 1, SHEET 2	See Table 1, SHEET 2	
12. BLANK		13. SMD NUMBER	14. DEVICE TYPE DESIGNATOR	
		See Table 1, SHEET 2	See Table 1, SHEET 2	
		15. RHA LEVELS	16. QML LEVEL	
		R, F, G, H	Q, V	
		17. NON QML LEVEL	18. GIDEP	
40. DDODUOT OUANO		N/A	GB4-C-19-001	

19. PRODUCT CHANGE

All 8-bit Rad-Hard Medium Scale Integrated (RHMSI) Logic devices with Schmitt Trigger Inputs, listed in Table 1, SHEET 2 (below) will have parameters tR, tF (20%/80% input rise, fall times) added to the RECOMMENDED OPERATING CONDITIONS section, for both Data Sheets and SMD documents, with a limit value of <1µs. This change applies as of the EFFECTIVE DATE listed in section 9 (above).

A Product Advisory was issued in February, 2015, describing the issue and notifying device users via the CAES 8-bit RHMSI Logic webpage. The document link and Section 5, Summary and Conclusion, are provided below in italics for reference. However, in order to ensure that all users of the devices listed under Table 1 receive notification, CAES is issuing this ADEPT PCN.

Standard Products Product Advisory RHMSI with Schmitt Trigger Inputs: Recommended Max. Input Rise/Fall Time February 2015

www.cobhamaes.com/HiRel

## 5. Summary and Conclusion

There are maximum input rise/fall (tR,tF) time requirements for RHMSI products with Schmitt Trigger inputs that are not currently reflected in the product datasheets. The common practice for Schmitt Trigger inputs is to provide immunity to noise and slow rise/fall times. However, operating the referenced parts with input edges slower than 1µs (0-100%) may lead to anomalous output behavior. Limiting the logic input signal tR,tF to a maximum value of 1µs (0-100%) will avoid the risk of this undesired output behavior.

Additional UT54ACTS132 device measurements have been performed over voltage (V) and temperature (T). Based on all measurements and a review of general circuit characteristics, the maximum value of 1µs (0-100%) is representative of worst-case circuit operation for the referenced RHMSI with Schmitt Trigger input parts. Therefore, it is assumed that these findings and recommendations may be applied to all similar parts in this logic family. (Continued on SHEET 2)

20. DISPOSITIONARY RECOMMENDATION:	CHECK &	CONTACT	REMOVE &	CORRECT &
	USE AS IS	MANUFACTURER	REPLACE	USE AS SPECIFIED
21. ADEPT REPRESENTATIVE	22. SIGNATURE			23. DATE
Robert Polk				2019 FEB 26

## 5. Summary and Conclusion (Continued)

If the input signal is RC filtered sufficiently it will inherently filter any noise on the input and under these conditions the anomaly has not been observed.

Note: This PCN does not apply to the UT54ACS2S99S Dual and UT54ACS3G99S Triple ManyGate 8-bit RHMSI Logic devices with Schmitt Trigger Inputs, which have an input edge specification limit value of tR,tF<1s.

Table 1. Affected Part Numbers Under This PCN

Description	SMD Number	Device Type	CAESPart Number	CAES PIC Number
	5962-96524	01	UT54ACS14	CA014
Hex Inverter	5962-96524	02, 03	UT54ACS14E	CE014
Schmitt Trigger Inputs	5962-96525	01	UT54ACTS14	LA014
	5962-96525	02, 03	UT54ACTS14E	LE014
	5962-96542	01	UT54ACS132	CA132
Quad 2-In NAND Gate	5962-96542	02, 03	UT54ACS132E	CE132
Schmitt Trigger Inputs	5962-96543	01	UT54ACTS132	LA132
	5962-96543	02, 03	UT54ACTS132E	LE132
Octal Bus Transceivers	5962-96572	01	UT54ACS245S	CA45S
Schmitt Trigger Inputs	5962-96572	02, 03	UT54ACS245SE	CE45S

REVISON DATE: 05/28/2014 REVISION: C SHEET 2