

# PRODUCT INFORMATION NOTICE

<b>1. TITLE</b> UT8MR8M8 64M MRAM Multi-Bit Error (MBE) detect pin behavior and functionality		<b>2. DOCUMENT NUMBER</b> SPO-2016-PIN-0001	
		<b>3. DATE (Year, Month, Date)</b> 2016, January 15 <sup>th</sup>	
<b>4. MANUFACTURER NAME AND ADDRESS</b> CAES 4350 CENTENNIAL BOULEVARD COLORADO SPRINGS, COLORADO 80907-3486		<b>5. MANUFACTURER POINT OF CONTACT NAME</b> Michelle Mundie	
		<b>6. MANUFACTURER POINT OF CONTACT TELEPHONE</b> (719) 594-8052	
		<b>7. MANUFACTURER POINT OF CONTACT EMAIL</b> Michelle.mundie@cobhamaes.com	
<b>8. CAGE CODE</b> 65342	<b>9. BLANK</b>	<b>10. PRODUCT IDENTIFICATION CODE</b> MQ09	<b>11. BASE PART</b> UT8MR8M8
<b>12. BLANK</b>		<b>13. SMD NUMBER</b> 5962-13207	<b>14. DEVICE TYPE DESIGNATOR</b> 01,02
		<b>15. RHA LEVELS</b> R, F, G, H	<b>16. QML LEVEL</b> Q,V
		<b>17. NON QML LEVEL</b> N/A	<b>18. BLANK</b>

**19. DESCRIPTION (FOR NEW PRODUCTS, PROVIDE AVAILABILITY DATE AND LEAD TIME)**

This Product Information Notice is to notify users of QML grade UT8MR8M8 64M MRAMs of the Multi-Bit Error (MBE) detection pin behavior.

The UT8MR8M8 64M MRAM is a Multi-Chip Module (MCM) made up of four 16M MRAM die. Each die has its own open drain MBE pin and these pins are wire or connected within the UT8MR8M8 package. The MBE output is not defined after power up or after coming out of sleep until the MRAM is enabled for the first time. In order for the MBE pin to have guaranteed valid data, all die within the package must be accessed. This can be accomplished by toggling the four separate enable pins (/E[3:0]) or by toggling through A[22:21] with /En\_All held low. This behavior was not clearly described in the product datasheet.

CAES is currently in process of updating its documentation to comprehend this behavior. Timing diagrams that will be included in the final datasheet are attached.

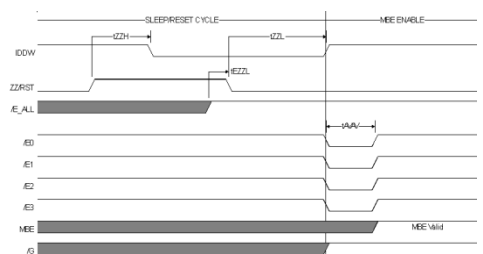


Figure 1: Post Reset MBE enable using enable pins /E[3:0]

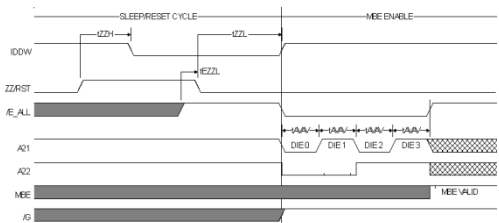


Figure 2: Post Reset MBE enable using A[22:21] and /En\_All

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<b>20. ADEPT REPRESENTATIVE</b> Lin-Chi Huang	<b>21. SIGNATURE</b> 	<b>22. DATE</b> January 18, 2016
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