QLE Programming Notes
256Kb PROMs

Table 1: Cross Reference of Applicable Products

Product Name	Manufacturer Part Number	SMD #	Device Type	Internal PIC* Number
32K x 8, 5V PROM	UT28F256QLE	5962-96891	09 and 10	WE50 / WE60
32K x 8, 3.3V PROM	UT28F256LVQLE	5962-01517	04,05,and 06	WE30 / WE40
32K x 8 5V PROM	UT28F256QLEL	NA	NA	WE20
32K x 8, 3.3V PROM	UT28F256LVQLEL	NA	NA	WE10

* PIC = Frontgrade internal Product Identification Code

Important Notice: Before programming any device, please verify that device is properly aligned in carrier per Figure 1 paying attention to key position with respect to top and bottom of device. With single carrier key to the left (as shown in Figure 1), the bottom of the device should be visible. When inserted into programmer socket module, the single key will only fit one way with part markings (top of device) being visible. Devices not aligned in proper slot locations will fail continuity. Device in the proper slot locations, but incorrect with respect to top and bottom, will pass continuity but fail blank check.

1.0 Overview

The following information is provided to assist users during programming of the Frontgrade Radiation Hardened 256K 5V and 3.3V PROMs listed in Table 1.

2.0 PROM Technical Background

The devices listed in Table 1 are 256Kbit PROMs organized as 32K x 8bits. The PROM devices feature a redundant ViaLinkTM structure for each memory cell which provides unprecedented reliability. The redundant ViaLinkTM creates a parallel path. During the programming phase, both primary and redundant paths must program and verify successfully. During device operation, either or both paths will result in valid data.

2.1 One Time Programmable

The Frontgrade PROMS are one time programmable devices. When programming is complete (successful or otherwise), a security fuse is blown which disables the test modes used during programming. The programming algorithm will not start a device with disabled test modes. For this reason, it is important to program each device correctly and completely.

3.0 Programming Time

Due to the redundant cell structure, the programming time of the Frontgrade 256K PROMs may take longer than other industry compatible PROM devices. Frontgrade believes the increased programming time is warranted for systems demanding higher reliability. Programming times will vary depending on the amount of bits being programmed. The devices are supplied in an all 0's state which is the native state of each memory cell. Only bits requiring 1's data are programmed. Bits remaining as 0's retain the native clear state. Therefore, the fewer set bits in the source code, the shorter the programming time. Some industry comparable devices recommend that set data be programmed into the unused memory space. This is not recommended for Frontgrade PROMs. Frontgrade recommends leaving unused areas in the default clear state. Default programming large areas with 1's data increases programming time and increases the chances of programming yield loss. Page two of the QLE Programming Guide notes that programming time can vary and may take up to 4 hours to complete programming a typical program with full utilization of the PROM's addressable space. For reference, it takes approximately 85msec to program each set bit.

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3.1 Programming Instructions and Equipment

Frontgrade QLE PROMs are programmed using a BPM Microsystems' programmer in conjunction with Frontgrade QLE Programming Guide [1]. BPM Microsystems provides several models supporting these devices. The programmer information can be found at BPM Microsystems' Website [2]. BPM provides both single and multi socket programmers which can program up to 6 devices concurrently for increased throughput (provided they are using the same source code). Current manual model numbers 1710 (single site) or 2710 (2, 4, or 6 sites) support Frontgrade PROM programming requirements.

Programming setup per Frontgrade QLE Programming Guide, enables a continuity and blank check prior to programming. If a continuity fail occurs, reseat the device in the socket and restart. If continuity fails persist, please inspect device pins and socket for any signs of contaminants or damage. Devices should be supplied in carriers to properly interface with the programmer's socket. If continuity problems persist, verify the device is orientated correctly in the carrier per Figure 1. Continuity test uses a low voltage low current load sense. Continuity failures, for any reason, will not cause stress to the device. However, devices aligned in proper slots but inserted incorrectly with respect to top and bottom of the device will pass continuity but fail subsequent blank check. This situation should be considered as possible stress to the device and should not be used in flight hardware. Blank check verifies the device contains all native 0's data. If blank check fails, the device may contain some data, implying it has been programmed previously. After a successful blank check, device programming begins. Once this occurs, the programming must complete without interruption. Any interruption in programming renders the device unusable. When programming is complete (successful or otherwise) a security fuse is programmed and the device cannot be programmed again. Devices failing to verify during the programming phase are considered failing devices. Due to the nature of one time programmable devices, some small programming yield loss may occur.

Devices also contain a factory programmed device code designed to correlate to the correct programming algorithm. If the device code does not match the algorithm code, the programmer aborts programming and a fail message "Failed to perform operation on device. Cannot program" or similar, will quickly be displayed. If this occurs, please verify the correct algorithm has been selected for the applicable device type. Device security fuse is not affected by internal device code to algorithm mismatches.

3.1.0 Programming Failures and Yield

Frontgrade PROM devices contain test rows and columns, which are used by Frontgrade production test programs to verify the ability to program all rows and columns of the memory array structure. Individual memory cells, necessarily cannot be tested. This is inherent with unprogrammed devices. Because memory cells are not verified, some small programming yield loss may occur. During the programming phase, the set bits are programmed and verified serially from the beginning of the programming buffer through the end. If at any point during programming, a cell cannot be verified correctly, the programming will halt. An error message similar to, "Failed to perform operation on device. Cannot program" will be displayed. This can occur at any time during the programming depending on when an un-programmable ViaLinkTM is encountered. When programming and verification completes successfully, the green "pass" LED on the socket module will illuminate and a, "function complete" statement will appear in the lower left corner of the BPwin programming window.

4.0 Conclusion

Frontgrade PROMs contain redundant ViaLinksTM for higher reliability. Because of this, it may take several hours to program a device. Devices are one time programmable. Once programming starts, allow programming to complete uninterrupted. To guarantee the highest reliability, Frontgrade PROMs contain a security fuse to inhibit reprogramming. Frontgrade PROMs contain an internal device code to assure use of the correct programming algorithm.

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5.0 References

1) QLE Programming Guide https://Frontgrade.com/sites/default/files/documents/App-Note-256Kb-PROM-ProgrammingGuide.pdf
2) BPM Microsystems Website: at https://bpmmicro.com

Systems Technical Support UT28F256QLE/L AND UT28F256LVQLE/L PROM Alignment Within Carrier

The following diagram shows the alignment of the UT28F256QLE/L and UT28F256LVQLE/L PROMs within its carrier. It is very important that the PROM is properly aligned in the carrier during programming. If you attempt to program the PROM when it is not properly aligned, the BP Microsystems programmer will fail continuity check.

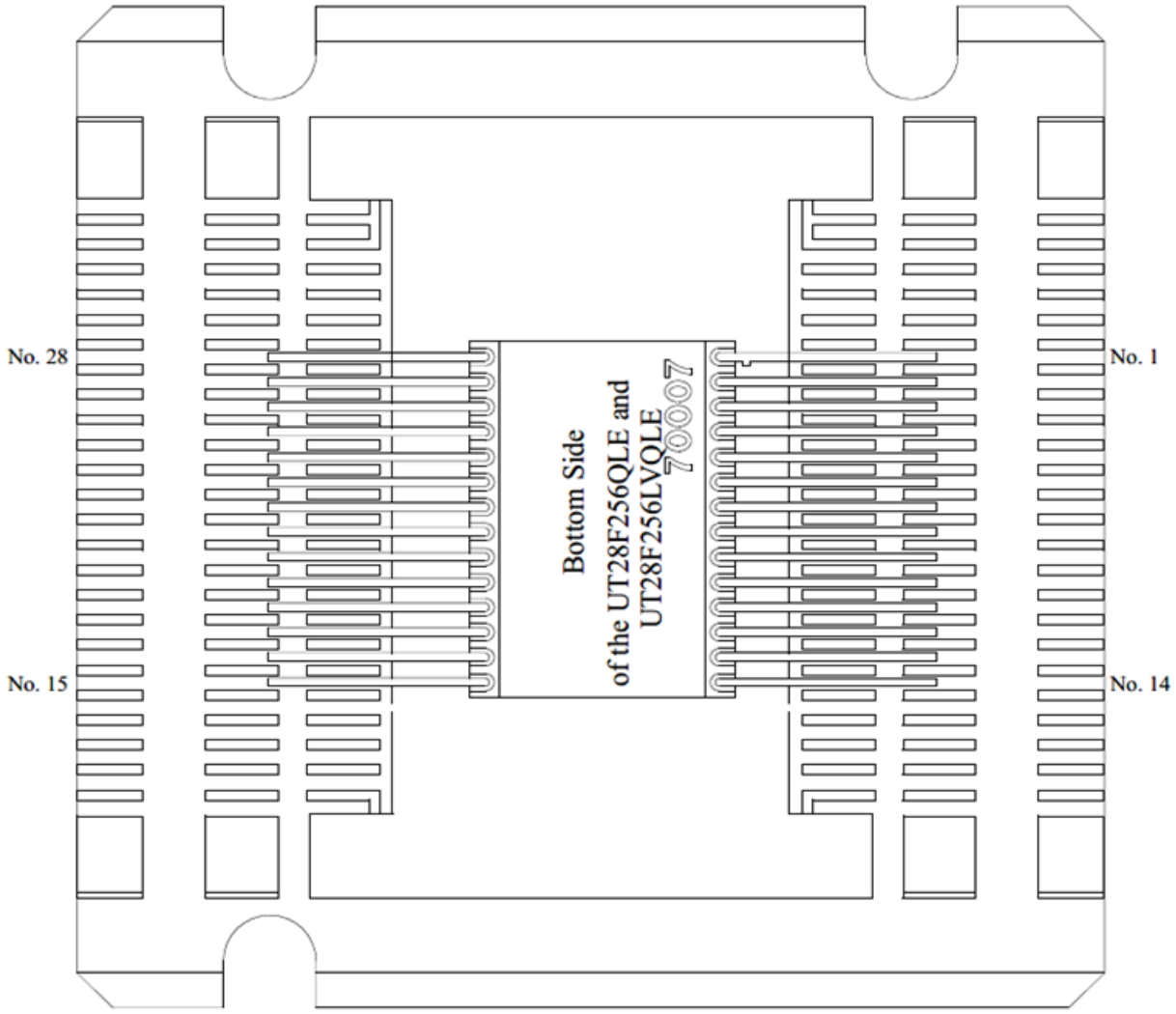

Figure 1. Diagram of the UT28F256QLE/L and UT28F256LVQLE/L PROM 28-Pin Flat Pack in Carrier

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Revision History

Date	Revision	Author	Change Description
04/07/2011	1.0.0	MJL	Initial Release
06/15/2011	1.1.0	MJL	Converted format to current Frontgrade Template. Added UT28F256QLEL and UT28F256LVQLEL product for Suntek. Updated Frontgrade and BP links.
4/20/2023	1.2.0	MJL	Added Important Notice to (page 1). Clarified continuity failures will not cause stress but flipped device blank check may (page 2). Changed all ref to CAES to Frontgrade. Correct link to Frontgrade sec 5.0.

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