DATASHEET

REV L: 02/18/21

SCD8692

7.5 Amp LDO Adjustable Positive Voltage Regulators

VRG8691/92

Features

- Radiation performance
  - Total dose: 100 krad(Si),
    Dose rate = 50-300 rad(Si)/s
- Output voltage adjustable: 1.0V to 3.3V
- Output current: 7.5A
- Dropout voltage: 0.5V at 7.5Amps
- Voltage reference: 1.0V ±0.5%
- Load regulation: 0.5% max
- Line regulation: 0.2% max
- Ripple rejection: >80dB
- Enable Input - TTL / CMOS Compatible
- Slow Start capability
- Stable with multiple ceramic output capacitors
- Packaging – Hermetic metal
  - Thru-hole or Surface mount
  - 12 Leads, 0.900"L x 1.000"W x .205"Ht
  - Power package
  - Weight - 18 gm max
- Designed for aerospace and high reliability space applications
- **Radiation Hardness Assurance Plan: DLA Certified to MIL-PRF-38534, Appendix G.**

Description

The VRG8691/92 is capable of supplying in excess of 7.5Amps over the output voltage range as defined under recommended operating conditions. The regulator is exceptionally easy to set-up, requiring only 2 external resistors to set the output voltage. The module design has been optimized for excellent regulation and low drop-out voltage. Figures 2 through 5 illustrate setting output voltage, setting current limits and choosing a slow start capacitor. The VRG8691/92 serves a wide variety of applications including local on-card regulation, programmable output voltage regulation or precision current regulation.

The VRG8691/92 has been specifically designed to meet exposure to radiation environments. The VRG8691 is configured for a Thru-Hole 12 lead metal power package and the VRG8692 is configured for a Surface Mount 12 lead metal power package. It is guaranteed operational from -55°C to +125°C. Available screened to MIL-STD-883, the VRG8691/92 is ideal for demanding military and space applications.

Current Limit (I_{CL})

The VRG8691/92 features internal current limiting making them virtually blowout-proof against overloads. The limit is nominally 11.5A @ Vin = 5V (see Table 2), but may be increased or decreased with the addition of one external resistor (see Application Note 2).

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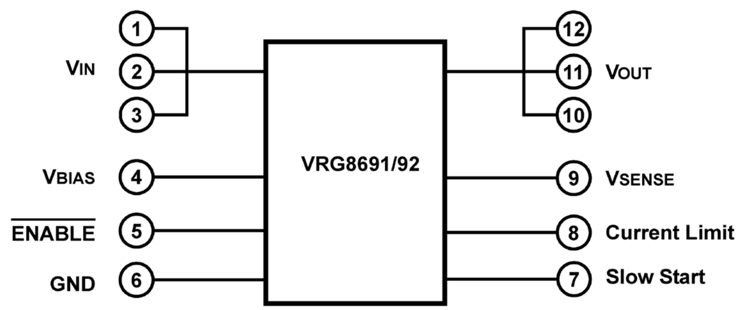

Figure 1 – Block Diagram / Schematic

Absolute Maximum Ratings

Parameter	Range	Units
Operating (Junction) Temperature Range	-55 to +150	°C
Lead Temperature (soldering, 10 sec)	300	°C
Storage Temperature Range	-65 to +150	°C
V_{BIAS}, V_{IN}	7	V
Thermal Resistance (Junction to case Θ_{JC})	1	°C/W
Power	25 1/	W

1/Based on pass transistor limitations of (V_{IN} - V_O) x I_O and Θ_{JC} < 1°C/W with 25°C max T_J rise and T_C = +125°C.

Notice:

1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; functional operation beyond the "Operation Conditions" is not recommended and extended exposure beyond the "Operation Conditions" may effect device reliability.

Recommended Operating Conditions

Parameter	Range	Units
Output Voltage Range	1.0 to 3.3	V_{DC}
Case Operating Temperature Range	-55 to +125	°C
Output Current	0 to 7.5	A
V_{BIAS}	3.3 to 5.5 1/	V_{DC}
V_{IN}	1.8 to 5.5 2/	V_{DC}

Notes:

1) V_{BIAS} must maintain a level equal or above V_{IN} but not fall below 3.3V
2) Depending upon V_{OUT} setting.

Electrical Performance Characteristics 1/

Parameter	SYM	Conditions	MIN	MAX	Units
Reference Voltage	V_{REF}	$V_{IN} = V_{BIAS} = 5V$, $\overline{ENABLE} = 0$, $0A \le I_{OUT} \le 7.5A$	0.985	1.015	V
Line Regulation	$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	$2V \le V_{IN} \le 3V$, $V_{OUT} = 1.0V$, $C_{IN} \ge 47\mu F$, $4.3V \le V_{IN} \le 5.3V$, $V_{OUT} = 3.3V$, $C_{OUT} \ge 47\mu F$,	-	0.2	%/V
Load Regulation	$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	$0A \le I_{OUT} \le 7.5A$, $C_{IN} \ge 47\mu F$, $C_{OUT} \ge 47\mu F$,	-	0.5	%
Ripple Rejection Ratio		$f = 120Hz$, $C_{LOAD} = 47\mu F$, $V_{IN} + V_{RIP} \ge V_{OUT} + V_{DROP(MAX)}$ @ 5A, $V_{IN} = 4.3V$, $V_{RIP} = 1V_{P-P}$, $V_{OUT} = 3.3V$	80	-	dB
Dropout Voltage	V_{DROP}	@$\Delta V_{OUT} = 1\%$, $0A \le I_{OUT} \le 7.5A$	-	0.5	V
Adjustment Pin Current	I_{ADJ}		-	100	pA
Minimum Load Current	I_{MIN}		-	0	mA
Current Limit 2/	I_{CL}		9.5	13.5	A
Long Term Stability 3/	$\frac{\Delta V_{OUT}}{\Delta T_{IME}}$		-	1	%
Supply Current (V_{BIAS})	I_{BIAS}		-	15	mA

Notes:

1) Unless otherwise specified, these specifications apply for post radiation: $V_{BIAS} = V_{IN} = 5V$, $V_{OUT} = 3.3V$, $I_{OUT} = 7.5A$ and 55°C < T_C <+125°C, Min Input/Output capacity of 47µF Tant with 1µF ceramic in parallel.
2) Current Limit is adjustable as shown in Application Note 2, Figures 3 and 4.
3) Not tested. Shall be guaranteed to the specified limits after 1000hr life test.

Application Note 1

Basic Set-Up

Setting the output voltage (V_{OUT}):

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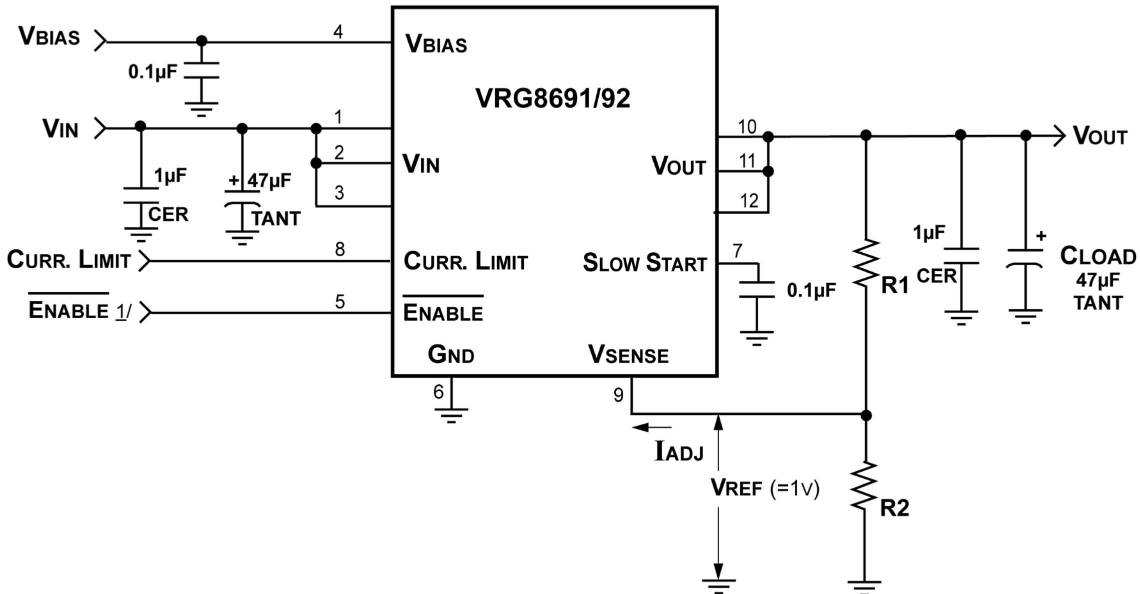

Figure 2 –Setting Output Voltage

To set the output voltage for a particular V_{OUT}:

- Choose an R2 value. (Recommended value = 1kΩ)
- Then use the following formula to determine the value of R1.

$$R1 = R2 \times \frac{V_{OUT} - V_{REF}}{(R2 \times I_{ADJ}) + V_{REF}}$$, where $V_{REF} = 1_V$, I_{ADJ} typ = 10pA

Table 1 shows example values for R1 and R2 to achieve some standard voltages.
Table 2 shows the nominal current limit settings if the 'CURR. LIMIT' function (pin 8) is left open.

Table 1

Example R1 & R2 for typical V_{OUT}

V_{OUT}	R2	R1
3.3V	1kΩ	2.3kΩ
2.5V	1kΩ	1.5kΩ
1.8V	1kΩ	800Ω
1.0V	1kΩ	0Ω

Table 2

2/

V_{IN}	$I_{CL\ NOM}$
5V	11.5A
3.3V	7.5A
2.5V	5.7A
1.8V	4.1A

Notes:

1) $\overline{ENABLE}$ should be asserted after both V_{IN} and V_{BIAS} are applied.
   (See Application Note 3, Figure 5 for the configuration where a separate $\overline{ENABLE}$ control line is NOT required).
2) I_{CL} varies directly with V_{IN}.
   (See Application Note 2 for adjusting the Current Limit, I_{CL}).

Application Note 2

Setting the Current Limit

To Increase the Current Limit (I_{CL}):

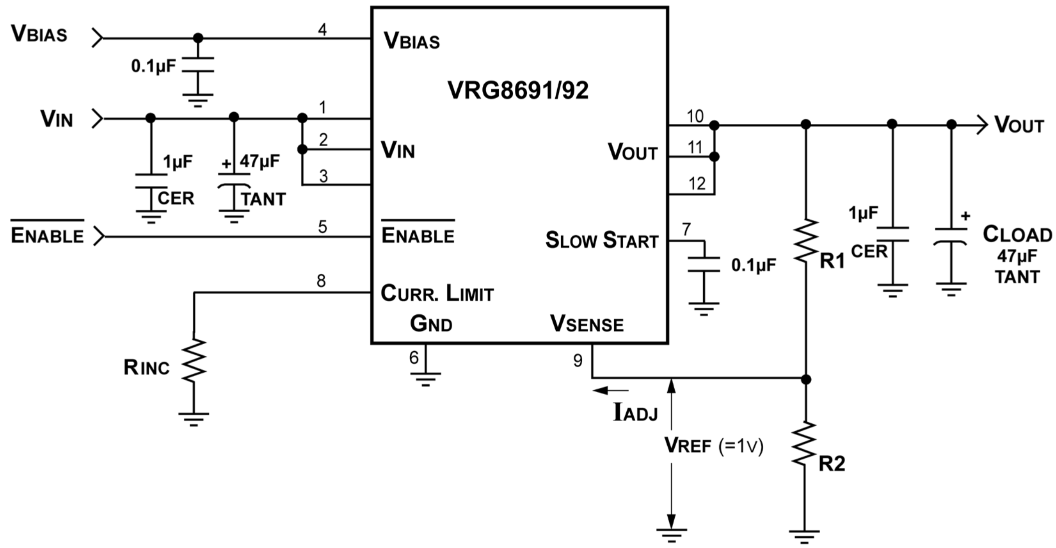

Figure 3 – Increasing the Current Limit (I_{CL})

- If the 'CURR. LIMIT' function (pin 8) is left open, the I_{CL} decreases from 11.5 $A_{(NOM)}$ as V_{IN} is decreased from 5V (Table 3).

Table 3

V_{IN}	R_{INC}	$I_{CL\ NOM}$
5V	Open	11.5 A
3.3V	Open	7.5 A
2.5V	Open	5.7 A
1.8V	Open	4.1 A

- To increase the current limit above the nominal setting for any V_{IN} and I_{CL} combination, use the following formula:

$$R_{INC(K\text{-}OHMS)} = \frac{30 \times V_{IN}}{\left(\frac{30 \times I_{CL}}{69}\right) - V_{IN}}$$

- To maintain I_{CL} at the 11.5 A setting, for commonly found V_{IN} voltages, apply R_{INC} value found in Table 4.

Table 4

V_{IN}	R_{INC}	$I_{CL\ NOM}$
5V	Open	11.5 A
3.3V	56kΩ	11.5 A
2.5V	30kΩ	11.5 A
1.8V	16kΩ	11.5 A

Application Note 2 (continued)
Setting the Current Limit

To Decrease the Current Limit (I_{CL}):

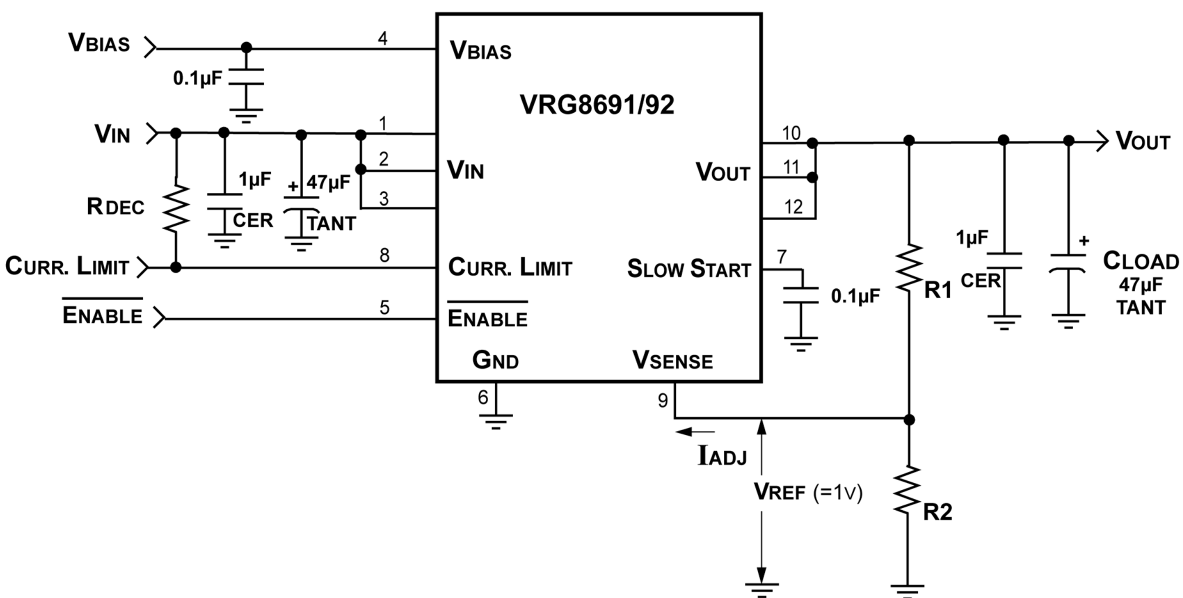

Figure 4 – Decreasing the Current Limit (I_{CL})

- As shown in Table 3, if the 'CURR. LIMIT' function (pin 8) is left open, the I_{CL} decreases from 11.5 $A_{(NOM)}$ as V_{IN} is decreased from 5V.
- To achieve any I_{CL}, less than nominal, use R_{DEC} which can be calculated using the following formula:

$$R_{DEC(K\text{-}OHMS)} = \frac{31 \times V_{IN}}{\left(\frac{69 \times V_{IN}}{30}\right) - I_{CL}}$$

Application Note 3
Start Up Sequence

Recommended Power Supply Sequencing Options:

- OPTION 1: Controlling the $\overline{\text{ENABLE}}$ line with a Digital signal (TTL / CMOS compatible).
  - Prior to applying power, disable the regulator by setting the $\overline{\text{ENABLE}}$ control line to a HIGH state.
  - Apply V_{IN} and V_{BIAS}. 1/
  - Wait until both V_{IN} and V_{BIAS} supplies have reached their operating levels.
  - Toggle the $\overline{\text{ENABLE}}$ control line to a LOW state to turn on V_{OUT} of the regulator.
- OPTION 2: Controlling the $\overline{\text{ENABLE}}$ line using the C_{DELAY} feature.
  - Connect a C_{DELAY} capacitor between V_{BIAS} and the $\overline{\text{ENABLE}}$ as shown in Figure 5 below. 2/
  - Apply V_{IN} and V_{BIAS}. 1/
  - C_{DELAY} causes the regulator to self-enable after V_{BIAS} has reached operating level.

Note:

1) The $\overline{\text{ENABLE}}$ should always be asserted AFTER V_{IN} and V_{BIAS} have reached operating level.

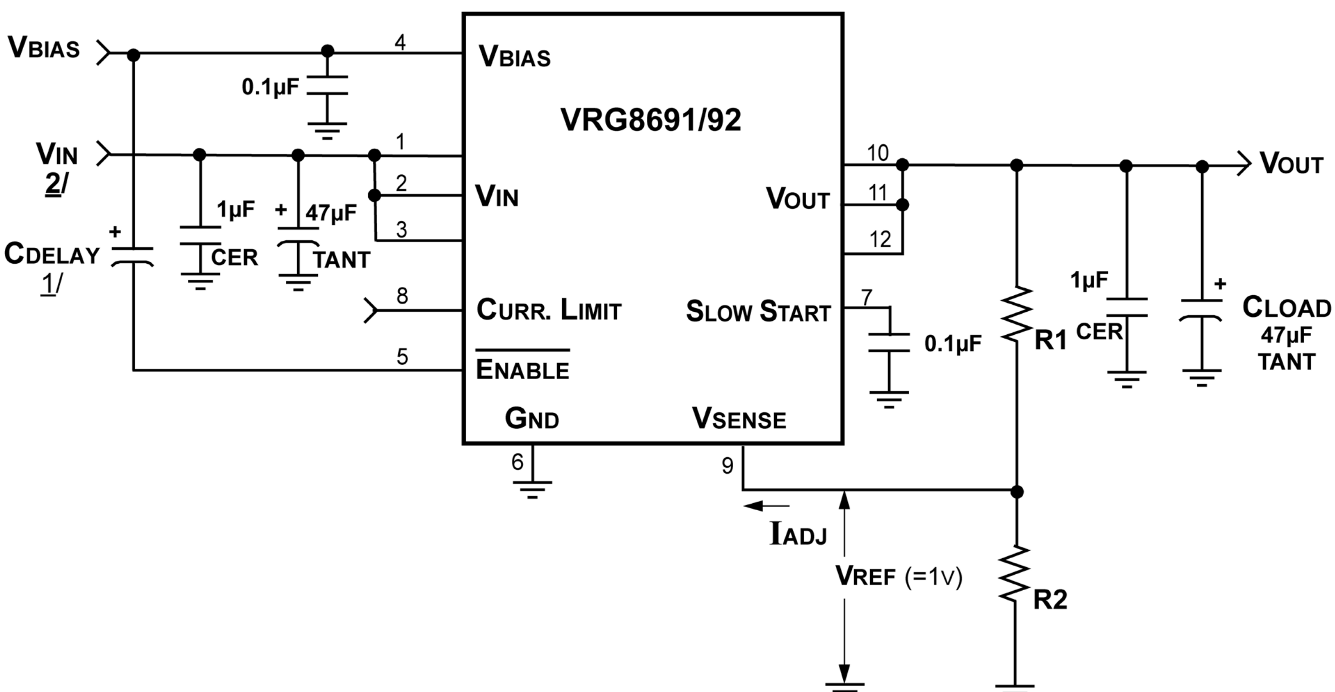

Figure 5 – Delayed Enable

Notes:

1) V_{IN} should be applied before V_{BIAS} if the Slow Start feature is used.
2) C_{DELAY} capacitor of 10uF is adequate for V_{BIAS} rise times of up to 50ms.

Application Note 4

<u>V_{OUT} Start Up Rise Time Control</u>

Utilizing the Slow Start option:

When the VRG8691/92 is first powered up, using the Slow Start function controls the rate at which V_{OUT} rises to the required voltage set by R1 and R2.

Note:

1) V_{IN} should be applied before V_{BIAS} when the Slow Start feature is used.

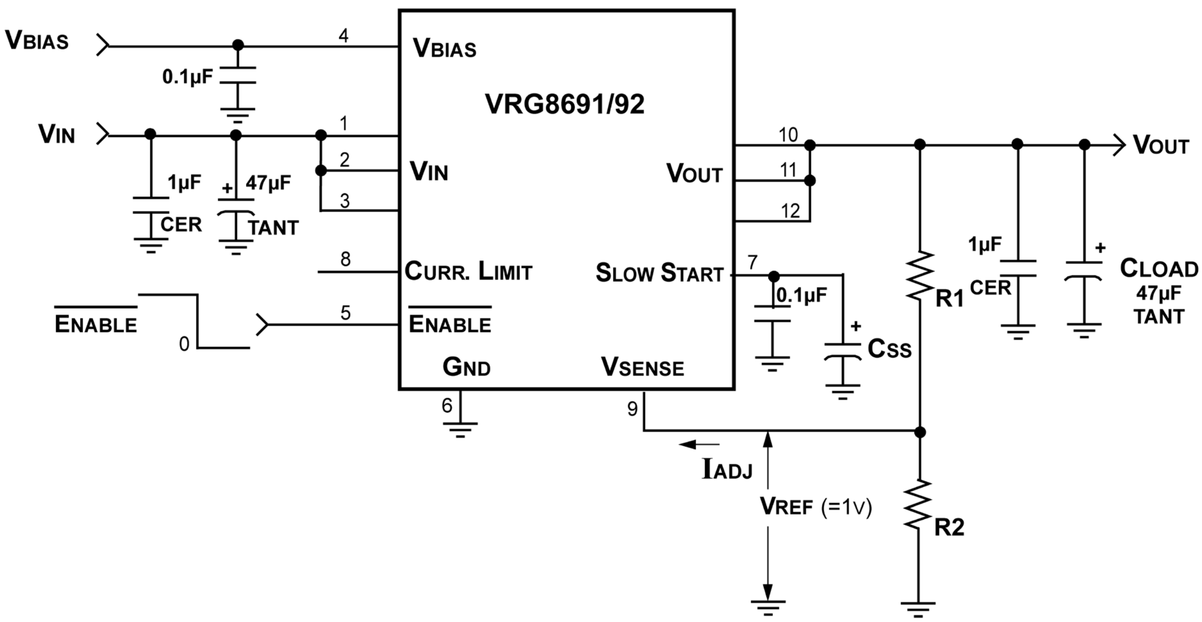

Figure 6 – Slow Start

If it is desirable to control the output rise time, a capacitor (C_{SS}) can be asserted on the Slow Start pin to adjust the rise time for the following:

A. Large load capacitance will cause high surge currents which will trip the current limit circuitry. The use of C_{SS} will allow the output voltage to rise slowly thus mitigate the surge current phenomenon.

$$\frac{C_{SS}}{C_{LOAD}} > \frac{V_{OUT\ NOM}}{I_{CL} - I_{LOAD\ NOM}} \text{ X } (0.4 \text{ X } 0.0014)$$

B. C_{SS} may be used solely to control V_{OUT} RISE TIME (Tr), when C_{LOAD} is not an issue.

$$T_R = \left(\frac{C_{SS} \text{ X } 2.5}{0.0014}\right) \quad \text{Note: } C_{SS} \text{ in Farads and } T_R \text{ in seconds.}$$

C. C_{SS} is effective only when V_{IN} is applied prior to V_{BIAS} or $\overline{\text{ENABLE}}$.

Pin Numbers vs Function

Pin	Function	Pin	Function
1	V_{IN}	7	Slow Start
2	V_{IN}	8	Current Limit
3	V_{IN}	9	V_{SENSE}
4	V_{BIAS}	10	V_{OUT}
5	$\overline{\text{ENABLE}}$	11	V_{OUT}
6	GROUND	12	V_{OUT}

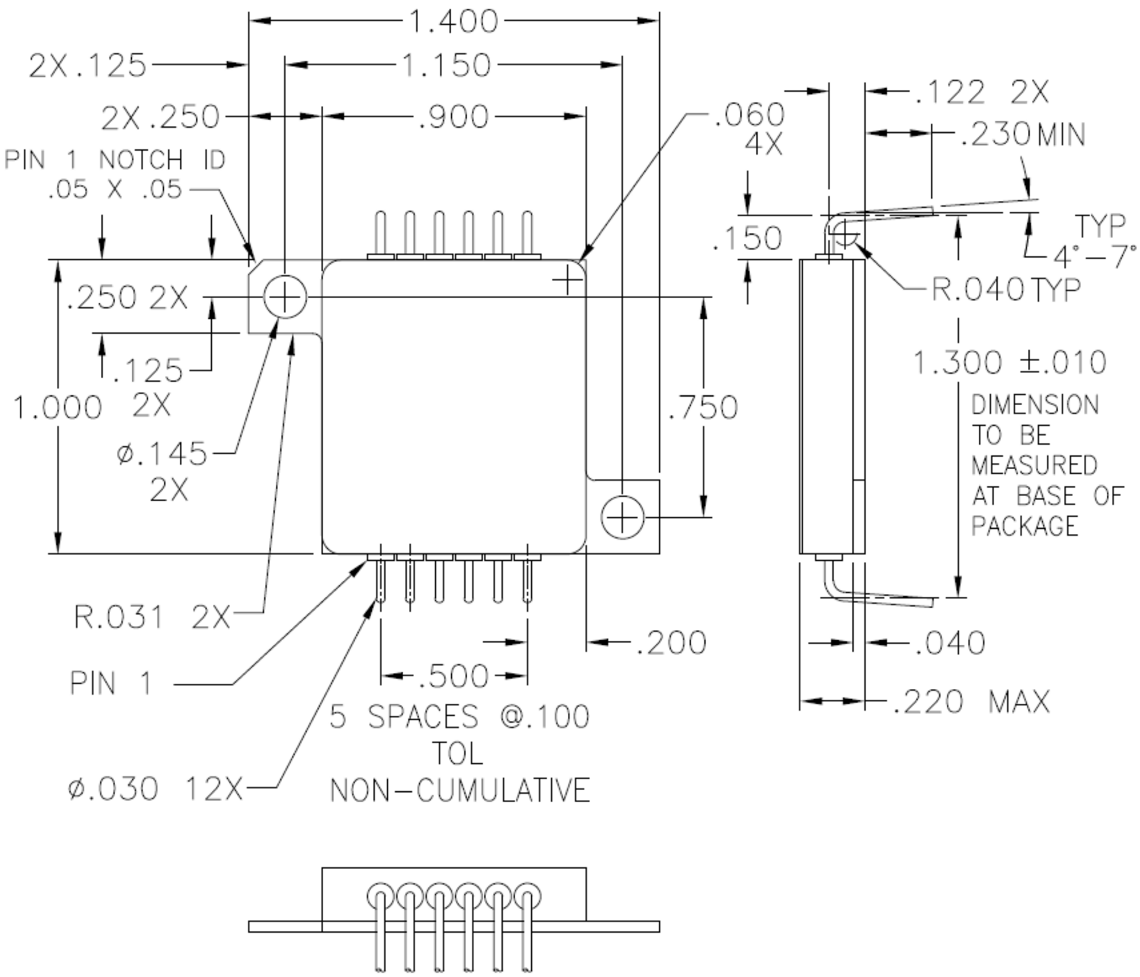

Figure 7– Package Outline — VRG8691 Thru-Hole Power Package

Notes:

1) Dimension Tolerance: ±.005 inches
2) Package contains BeO substrate
3) Case electrically isolated

Pin Numbers vs Function

Pin	Function	Pin	Function
1	V_{IN}	7	Slow Start
2	V_{IN}	8	Current Limit
3	V_{IN}	9	V_{SENSE}
4	V_{BIAS}	10	V_{OUT}
5	$\overline{ENABLE}$	11	V_{OUT}
6	GROUND	12	V_{OUT}

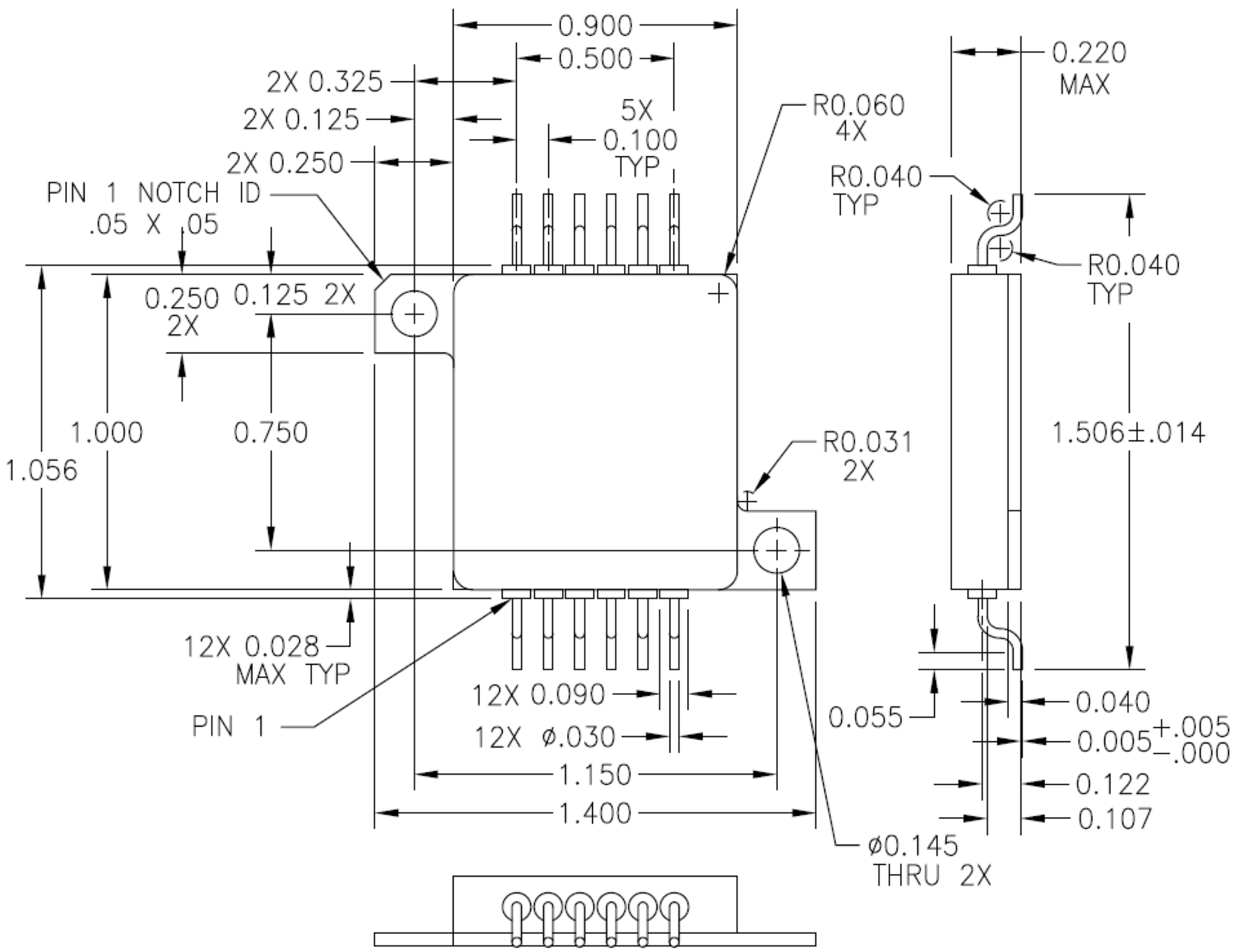

Figure 8– Package Outline — VRG8692 Surface Mount Power Package

Notes:

1) Dimension Tolerance: ±.005 inches
2) Package contains BeO substrate
3) Case electrically isolated

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Ordering Information

Model	DLA SMD #	Screening	Package
VRG8691 - 7	-	Commercial Flow, +25°C testing only	12 Lead Thru-Hole Power Pkg
VRG8691 - S	-	Military Temperature, -55°C to +125°C Screened in accordance with the individual Test Methods of MIL-STD-883 for Space Applications	
VRG8691- 201-1S	5962-0923701KXC	In accordance with DLA SMD	
VRG8691- 201-2S	5962-0923701KXA		
VRG8691- 901-1S	5962R0923701KXC	In accordance with DLA Certified RHA Program Plan to RHA Level "R", 100 krad(Si)	
VRG8691- 901-2S	5962R0923701KXA		
VRG8692 - 7	-	Commercial Flow, +25°C testing only	12 Lead Surface Mount Power Pkg
VRG8692 - S	-	Military Temperature, -55°C to +125°C Screened in accordance with the individual Test Methods of MIL-STD-883 for Space Applications	
VRG8692- 201-1S	5962-0923701KYC	In accordance with DLA SMD	
VRG8692- 201-2S	5962-0923701KYA		
VRG8692- 901-1S	5962R0923701KYC	In accordance with DLA Certified RHA Program Plan to RHA Level "R", 100 krad(Si)	
VRG8692- 901-2S	5962R0923701KYA		

Revision History

Date	Revision	Change Description
03/24/2016	J	Import into CAES format
02/18/2021	L	REVISED PER ECN 23515

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Datasheet Definitions

	DEFINITION
Advanced Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet **is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final**.
Preliminary Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

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