

64Megabit Non-Volatile MRAM

UT8MR8M8

Features

- Single 3.3-V power supply
- Fast 50ns read/write access time
- Functionally compatible with traditional asynchronous SRAMs
- Equal address and chip-enable access times
- HiRel temperature range (-40°C to +105°C)
- Automatic data protection with low-voltage inhibit circuitry to prevent writes on power loss
- CMOS and TTL compatible
- Data non-volatile for > 20 years (-40°C to +105°C)
- Read/write endurance: Unlimited for 20 years (-40°C to +105°C)
- 64-pin ceramic flatpack package (21.99 grams)
- Operational environment:
 - Total dose: 1Mrad(Si)
 - SEL Immune: 112 MeV-cm²/mg @125°C
 - SEU Immune: Memory Cell 112 MeV-cm²/mg @25°C
- Standard Microelectronics Drawing (SMD) - 5962-13207
 - QML Q, Q+, and V

Introduction

The Frontgrade 64Megabit Non-Volatile magnetoresistive random access memory (MRAM) is a high-performance memory multichip module (MCM) compatible with traditional asynchronous SRAM operations, organized as either four 2M words by 8 bits or one 8M words by 8 bits.

The MRAM is equipped with five chip enables (/En), a single write enable (/W), and a single output enable (/G) pins, allowing for significant system design flexibility without bus contention. Data is non-volatile for > 20 years at temperature and data is automatically protected against power loss by a low voltage write inhibit.

The 64Mb MRAM is designed specifically for operation in HiREL environments. As shown in Table 4, the magnetoresistive bit cells are immune to Single Event Effects (SEE). To guard against transient effects, an Error Correction Code (ECC) is included within the device. ECC check bits are generated and stored within the MRAM array during writes. The MBE (multiple-bit-error) pin identifies that ECC logic has detected two bit errors during the current read cycle.

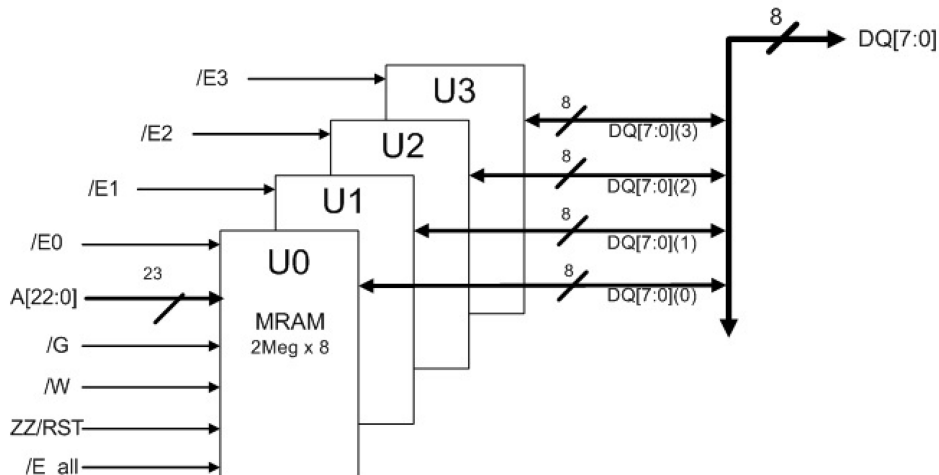


Figure 1. UT8MR8M8 MRAM Block Diagram

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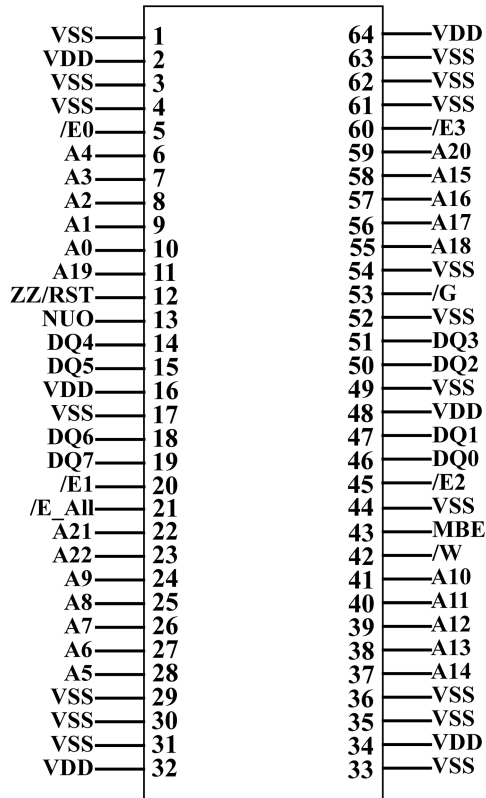


Figure 2. 40ns MRAM Pinout (64)

Pin Names

Table 1. 8M x 8 Pin Functions

Signal Name	Function
A[22:0]	Address Input
/E[3:0] ¹	Chip Enable
/E_All	Chip Enable All
/W	Write Enable
/G	Output Enable
DQ[7:0]	Data I/O
VDD	Power Supply
VSS	Ground
ZZ/RST	Deep Power Down/Reset (Internal pull down)
MBE ²	Multi-Bit Error Flag
NUO	Not used output Do not connect Driven internally

*Notes:

- 1) Only one /E[3:0] pin may be active at any time.
- 2) **MBE pin is not functionally tested for prototypes.**

Device Operation

The UT8MR8M8 has control inputs called Chip Enable (E[3:0]), Chip Enable All (/E_ALL), Write Enable (/W), Output Enable (/G), and sleep/reset mode (ZZ/RST); 23 address inputs, A[22:0]; eight bidirectional data lines, DQ[7:0]; and a Multi-bit Error Flag (MBE). /E[3:0] controls device selection, active, and standby modes. Asserting /E[3:0] enables the device, causes IDD to rise to its active value, and decodes the 21 address inputs, A[20:0], to select one of 16,777,216 words in the memory. **Note:** Only one Chip Enable may be active at any time. Asserting /E_ALL allows the device to be addressed as a single, 64Mb memory using address bits A21 and A22 to decode and select 1 of 4 MRAM die. /W controls read and write operation. During a read cycle, /G must be asserted to enable the outputs. ZZ/RST controls the sleep/reset mode operation and provides device reset capability. Enabling sleep/reset mode causes all other inputs to be don't cares. ZZ/RST places all die into internal low power even while system power is still applied to VDD. The MBE pin is an open drain output pin which allows for wired-OR of multiple MBE when using multiple MRAMs. The MBE pin requires an external pull up to reach the high inactive state. See MRAM FAQ to determine the resistor value. After MBE initialization and only during data output valid time, an MBE low indicates that a two bit error exists for the read cycle..

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Table 2. Chip Enable Functions Table

/E_ALL	/E_0	/E_1	/E_2	/E_3	A22	A21	Comment
0	1	1	1	1	0	0	MRAM Die 0 Enabled
0	1	1	1	1	0	1	MRAM Die 1 Enabled
0	1	1	1	1	1	0	MRAM Die 3 Enabled
0	1	1	1	1	1	1	MRAM Die 2 Enabled
1	0	1	1	1	X	X	MRAM Die 0 Enabled
1	1	0	1	1	X	X	MRAM Die 1 Enabled
1	1	1	0	1	X	X	MRAM Die 2 Enabled
1	1	1	1	0	X	X	MRAM Die 3 Enabled

***Note:**

1) Only one /E[3:0] pin may be active at any time.

Table 3. Device Operation Truth Table

ZZ/ RST	/E[3:0]*	/G	/W	Mode	VDD Current	DQ[7:0]
H	X	X	X	Deep Sleep/ Reset Mode	Q_{IZZ}	HI-Z
L	H	X	X	Not Selected	Q_{IDD}	HI-Z
L	L	H	H	Output Disabled	I_{DDR}	HI-Z
L	L	L	H	Byte Read	I_{DDR}	D_{OUT}
L	L	X	L	Byte Write	I_{DDW}	D_{IN}

***Note:**

1) Only one /E[3:0] pin may be active at any time.

Read Cycle

A combination of /W greater than V_{IH} (min) and a single /En less than V_{IL} (max) defines a read cycle. Read access time is measured from the latter of chip enable, output enable, or valid address to valid data output.

MRAM Read Cycle 1, the Address Access in Figure 4a, is initiated by a change in address inputs after a single /En is asserted, /G asserted and /W deasserted. Valid data appears on data outputs DQ[7:0] after the specified t_{AVQV} is satisfied. Outputs remain active throughout the entire cycle. As long as a single chip enable and output enable are active, the address inputs may change at a rate equal to the minimum read cycle time (t_{AVAV}).

MRAM Read Cycle 2, the Chip Enable-controlled Access in Figure 4b, is initiated by a single /En going active while /G remains asserted, /W remains deasserted, and the addresses remain stable for the entire cycle. After the specified t_{ELQV} is satisfied, the eight-bit word addressed by A[20:0] is accessed and appears at the data outputs DQ[7:0].

Write Cycle

A combination of /W and a single /En less than V_{IL} (max) defines a write cycle. The state of /G is a “don’t care” for a write cycle. The outputs are placed in the high-impedance state when either /G is greater than V_{IH} (min), or when /W is less than V_{IL} (max).

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Write Cycle 1, the Write Enable-controlled Access in Figure 5a, is defined by a write terminated by /W going high, with a single /En still active. The write pulse width is defined by t_{WLWH} when the write is initiated by /W, and by t_{ETWH} when the write is initiated by a single /En. Unless the outputs have been previously placed in the high-impedance state by /G, the user must wait t_{WLQZ} before applying data to the nine bidirectional pins DQ[7:0] to avoid bus contention.

Write Cycle 2, the Chip Enable-controlled Access in Figure 5b, is defined by a write terminated by a single /En going inactive. The write pulse width is defined by t_{WLEH} when the write is initiated by /W, and by t_{ELEH} when the write is initiated by a single /En going active. For the /W initiated write, unless the outputs have been previously placed in the high-impedance state by /G, the user must wait t_{WLQZ} before applying data to the eight bidirectional pins DQ[7:0] to avoid bus contention.

Operational Environment

The UT8MR8M8 MRAM incorporates special design and layout features which allows operation in harsh environments.

Table 4. Operational Environment Design Specifications

Parameter	Limit	Units
TID	1	Mrad(Si)
SEL Immunity ¹	≤ 112	MeV-cm ² /mg
SEU Memory Cell Immunity ²	≤ 112	MeV-cm ² /mg

Notes:

- 1) SEL test performance at $V_{DD} = 3.6V$ and temperature= 125°C.
- 2) SEU test performance at $V_{DD} = 3.0V$ and unpowered at room temperature.

Power Up and Power Down Sequencing

The MRAM is protected from write operations whenever V_{DD} is less than V_{WI} . As soon as V_{DD} exceeds $V_{DD}(min)$, there is a startup time of 2 ms before read or write operations can start. This time allows memory power supplies to stabilize. The /En and /W control signals should track V_{DD} on power up to $V_{DD}-0.2 V$ or V_{IH} (whichever is lower) and remain high for the startup time. In most systems, this means that these signals should be pulled up with a resistor so the signal remains high if the driving signal is Hi-Z during power up. Any logic that drives /En and /W should hold the signals high with a power-on reset signal for longer than the startup time. During power loss or brownout where V_{DD} goes below V_{WI} , writes are protected and a startup time must be observed when power returns above $V_{DD}(min)$.

The MRAM supports sleep/reset mode operation using the ZZ/RST control pin. To enter sleep mode/reset, ZZ/RST must be pulled high. The device will enter sleep/reset mode within 40ns. In order to exit sleep/reset mode, /En and /W must be high before ZZ/RST is pulled low. As soon as ZZ/RST is driven low, the user must allow 100us before performing any other operation in order for the device to properly initialize. Frontgrade recommends designing a system level method to toggle the ZZ/RST pin in order to reset the MRAM device.

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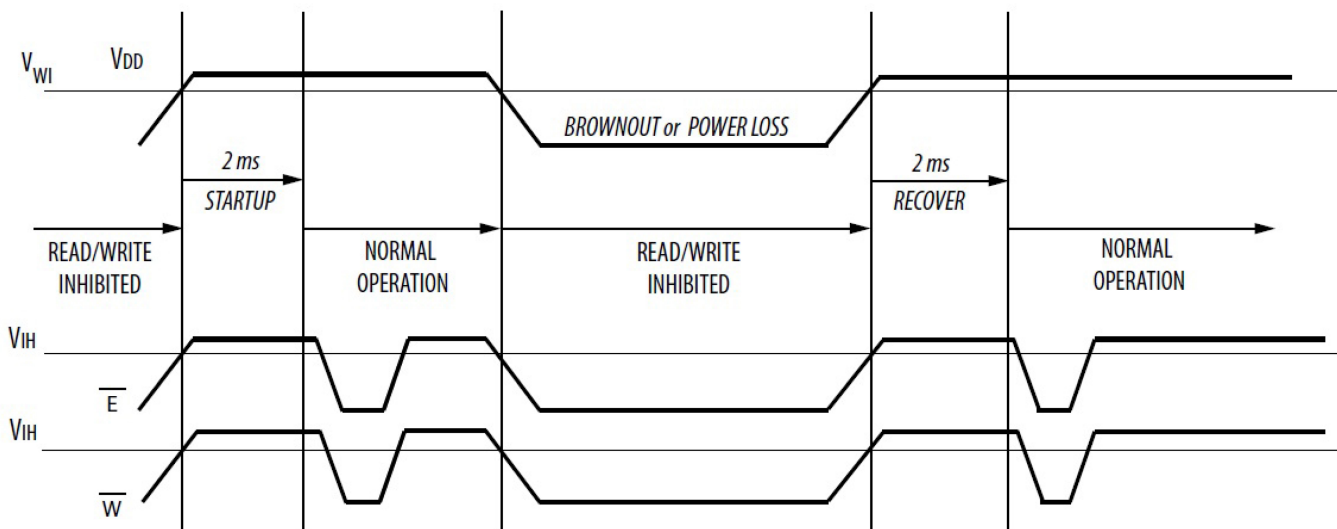
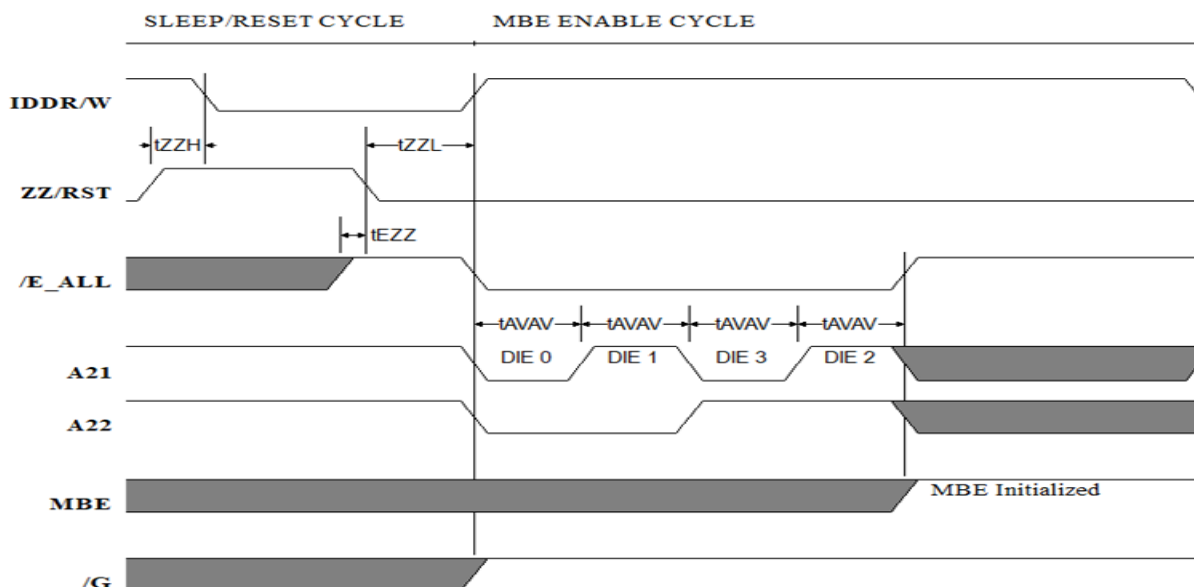


Figure 4. UT8MR8M8 Power Up and Power Down Sequencing Diagram

MBE Output Initialization

The 64M MRAM is a Multi-Chip Module (MCM) made up of four 16M MRAM die. Each die has its own open drain MBE output. These four MBE outputs are wired-OR connected within the UT8MR8M8 package to produce a single MCM MBE output. This MBE output is not defined after power up or after coming out of sleep/reset until the MRAM is enabled for the first time. In order to initialize the MBE pin after power up or reset, all die within the package must be accessed. This can be accomplished by toggling the four separate enable pins ($/\text{En}[0:3]$), or by toggling through $\text{A}[22:21]$ with $/\text{En_ALL}$ held low. After initialization, MBE is a device output with the same valid time as the data outputs. Spurious MBE low pulses can occur during the initiation of any read cycle. MBE is only valid if low after the minimum read access time has been satisfied (t_{AVAV} or t_{ELQV}). It is suggested that users poll the MBE pin at the same time the data is being polled (see Figures 5 and 6).

Figure 5. Post Reset MBE Initialization using A21, A22, & $/\text{E_All}$

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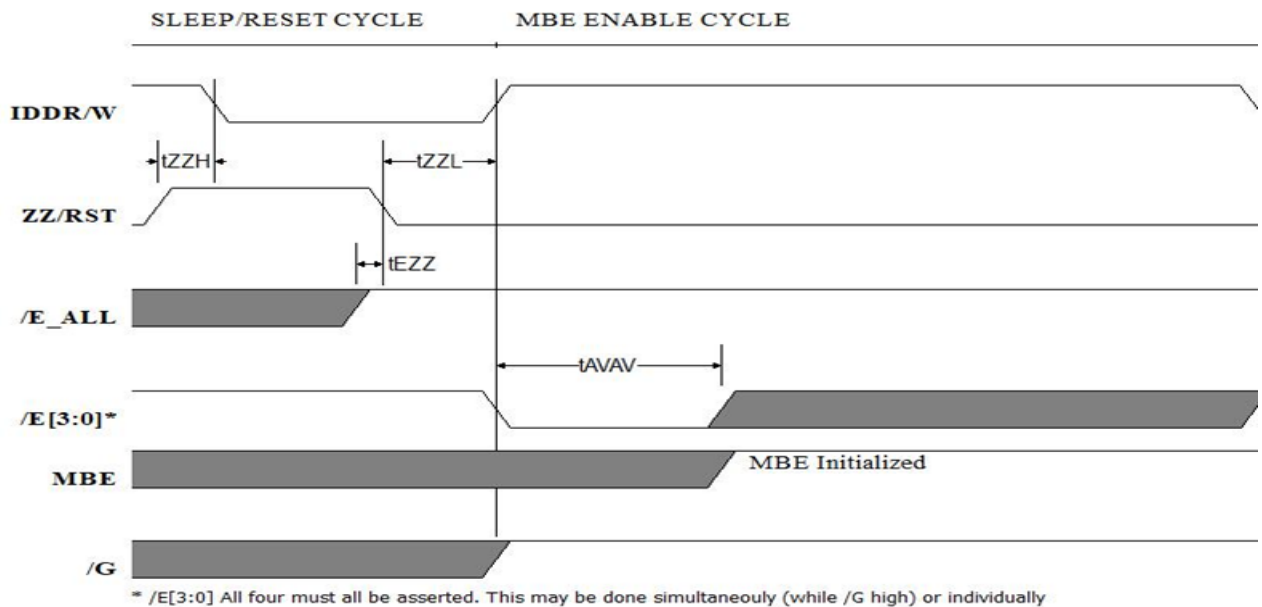


Figure 6. Post Reset MBE Initialization using enable pins /E[3:0]

Absolute Maximum Ratings¹(Referenced to V_{SS})

The device contains protection against magnetic fields. Precautions should be taken to avoid device exposure of any magnetic field intensity greater than specified.

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage ²	-0.5 to 4.3	V
V_{IN}	Voltage on any pin ²	-0.5 to $V_{DD}+0.5$	V
I_{IO}	DC I/O current per pin @ $T_J = 125^\circ$ for 20yrs	± 20	mA
P_D	Package power dissipation ³	9	W
T_J	Maximum junction temperature	+150	$^\circ\text{C}$
Θ_{JC}	Thermal resistance junction to case - Single Die	5	$^\circ\text{C}/\text{W}$
T_{STG}	Storage temperature	-65 to +125	$^\circ\text{C}$
ESD_{HBM}	ESD	>2000	V
H_{max_write}	Maximum magnetic field during write	8000	A/m
H_{max_read}	Maximum magnetic field during read or standby	8000	A/m

Notes:

- 1) Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to recommended operating conditions. Exposure to excessive voltages or magnetic fields could affect device reliability.
- 2) All voltages are referenced to V_{SS} .
- 3) Per MIL-STD-883, Method 1012, Section 3.4.1 $P_D = \frac{(T_J(\text{max}) - T_C(\text{max}))}{\Theta_{JC}}$

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Recommended Operating Conditions

Symbol	Parameter	Limits
T_C	Operating case temperature	-40°C to +105°C
V_{DD}	Operating supply voltage	3.0V to 3.6V
V_{WI}	Write inhibit voltage	2.5V to 3.0V ^{1, 2}
V_{IH}	Input high voltage	2.0V to $V_{DD}+0.3V$
V_{IL}	Input low voltage	$V_{SS}-0.3V$ to 0.8V

Notes:

- 1) After power up or if V_{DD} falls below V_{WI} , a waiting period of 2 ms must be observed, and /En and /W must remain high for 2 ms. Memory is designed to prevent writing for all input pin conditions if V_{DD} falls below minimum V_{WI} .
- 2) The MRAM is guaranteed to activate write inhibit below 2.5V, but may enter write inhibit mode anywhere within this voltage range. It is guaranteed to exit write inhibit mode once recommended operating voltage range is reached.

DC Electrical Characteristics (Pre and Post-Radiation) *

$V_{DD} = 3.0V$ to $3.6V$; Unless otherwise noted, T_c is per the temperature ordered ^{5, 6}

Symbol	Parameter	Condition	MIN	MAX	Unit
V_{IH}	High-level input voltage		2.0		V
V_{IL}	Low-level input voltage			0.8	V
V_{OL1}	Low-level output voltage	$I_{OL} = 4mA, V_{DD} = V_{DD} (min)$		0.4	V
V_{OL2}	Low-level output voltage	$I_{OL} = +100\mu A, V_{DD} = V_{DD} (min)$		$V_{SS}+0.2$	V
V_{OH1}	High-level output voltage	$I_{OH} = -4mA, V_{DD} = V_{DD} (min)$	2.4		V
V_{OH2}	High-level output voltage	$I_{OH} = -100\mu A, V_{DD} = V_{DD} (min)$	$V_{DD}-0.2$		V
C_{IN}^1	Input capacitance	$f = 1MHz @ 0V$		50	pF
C_{IO}^1	Bidirectional I/O capacitance	$f = 1MHz @ 0V$		60	pF
I_{IN}	Input leakage current	$V_{IN} = V_{DD}$ and V_{SS}	-1	+1	μA
I_{INZZ}	Input leakage current ZZ/RST	$V_{IN} = V_{DD}$ and V_{SS}	-0.25	0.25	mA
I_{OZ}	Three-state output leakage current	$V_O = V_{DD}$ and V_{SS} , $V_{DD} = V_{DD} (max)$ $/G = V_{DD} (max)$	-1	+1	μA
$I_{OS}^{2, 3}$	Short-circuit output current	$V_{DD} = V_{DD} (max), V_O = V_{DD}$ $V_{DD} = V_{DD} (max), V_O = V_{SS}$	-100	+100	mA
I_{DDR}	Active read supply current	Read mode $f = MAX$ ($I_{OUT} = 0mA; V_{DD} = max$)		140	mA
I_{DDW}	Active write supply current	Write mode $f = 10 MHz$ ($V_{DD} = max$)		140	mA
Q_{IDD}	Quiescent supply current	CMOS leakage current ($/E = V_{DD}$; all other inputs equal V_{SS} or V_{DD} ; $V_{DD} = max$)	-40°C +25°C	30	mA
			+105°C	35	mA
Q_{IZZ}^4	Deep power down and reset supply current	CMOS leakage current ($/E = V_{DD}$; all other inputs equal V_{SS} or V_{DD} ; $V_{DD} = max$)		1	mA

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Notes:

*For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

- 1) Measured only for initial qualification and after process or design changes that could affect input/output capacitance.
- 2) Supplied as a design limit but not guaranteed or tested.
- 3) Not more than one output may be shorted at a time for maximum duration of one second.
- 4) Allow 100 μ s to exit sleep/reset mode before performing any other operation.
- 5) MBE pin is an open drain, tested functionally.
- 6) Testing performed with Error Correction Code enabled (ECC-ON), customer use case always utilizes ECC-ON.

AC Characteristics Read Cycle ¹ (Pre and Post-Radiation) *

$V_{DD} = V_{DD}(\min)$; Unless otherwise noted, T_c is per the temperature ordered ^{5, 6}

Symbol	Parameter	MIN	MAX	Unit
t_{AVAV}	Read cycle time	50		ns
t_{AVQV}	Address access time		50	ns
t_{ELQV}^2	Enable access time		50	ns
t_{GLQV}^3	Output enable access time		25	ns
t_{AXQX}	Output hold from address change	3		ns
t_{ELQX}^4	Enable low to output active	3		ns
t_{GLQX}^4	Output enable low to output active	0		ns
t_{EHQZ}^4	Enable high to output Hi-Z	0	15	ns
t_{GHQZ}^4	Output enable high to output Hi-Z	0	15	ns

Notes:

*For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

- 1) /W is high for read cycle. Power supplies must be properly grounded and decoupled, and bus contention conditions must be minimized or eliminated during read or write cycles.
- 2) Address valid before or at the same time /En goes low.
- 3) t_{GLQV} output enable valid time unless t_{AVAV} or t_{AVQV} have not been satisfied.
- 4) Transition is measured at +/-400mV from the steady-state voltage.
- 5) MBE pin is an open drain, tested functionally.
- 6) Testing performed with Error Correction Code enabled (ECC-ON), customer use case always utilizes ECC-ON.

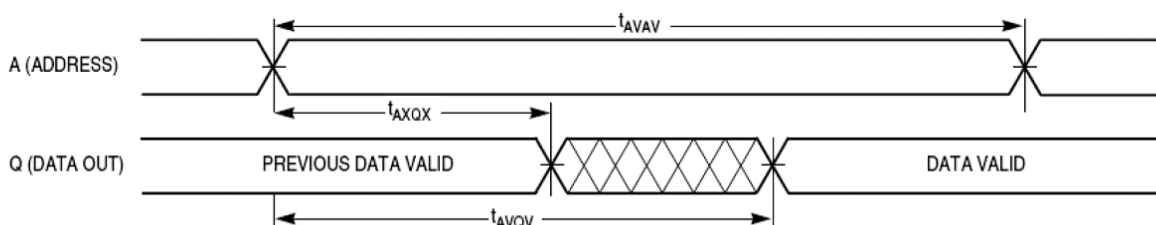


Figure 7a. MRAM Read Cycle 1

Note:

- 1) Devices is continuously selected ($/\text{En} \leq V_{IL}$, $\overline{\text{G}} \leq V_{IL}$).

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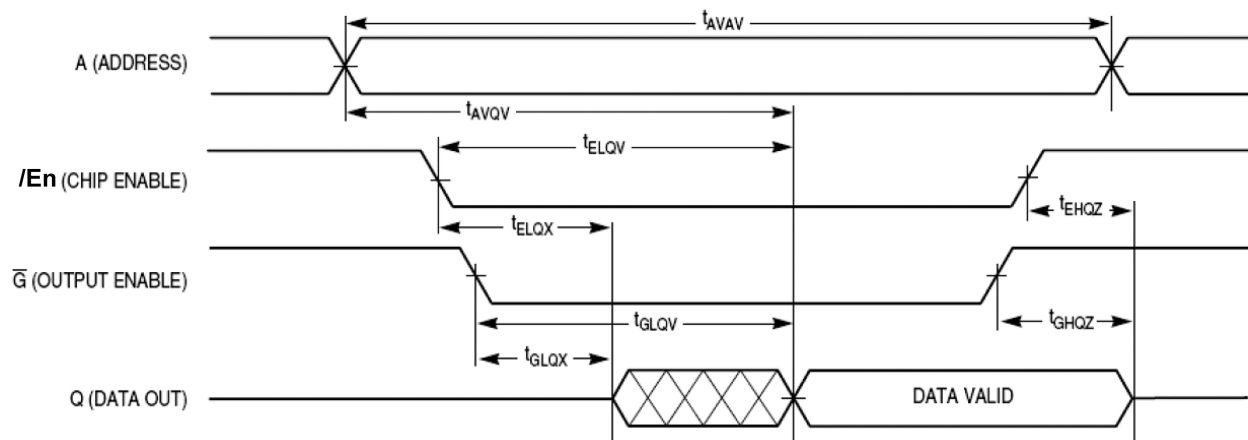


Figure 7b. MRAM Read Cycle 2

AC Characteristics /W Controlled Write Cycle (Pre and Post-Radiation) *

$V_{DD} = V_{DD}(\min)$; Unless otherwise noted, T_c is per the temperature ordered ^{4, 5}

Symbol	Parameter	MIN	MAX	Unit
t_{AVAV}^2	Write cycle time	50		ns
t_{AVWL}	Address set-up time	0		ns
t_{AVWH}	Address valid to end of write (/G high)	28		ns
t_{AVWL}	Address valid to end of write (/G low)	28		ns
t_{WLWH} t_{WLEH}	Write pulse width (/G high or low)	28		ns
t_{DVWH}	Data valid to end of write	10		ns
t_{WHDX}	Data hold time	0		ns
t_{WLQZ}^3	Write low to data Hi-Z	0	15	ns
t_{WHQX}^3	Write high to output active	3		ns
t_{WHAX}	Write recovery time	16		ns

Notes:

*For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

- 1) All write occurs during the overlap of /En low and /W low. Power supplies must be properly grounded and decoupled, and bus contention conditions must be minimized or eliminated during read or write cycles. If /G goes low at the same time or after /W goes low, the output will remain in a high impedance state.
- 2) All write cycle timings are referenced from the last valid address to the first transition address.
- 3) Transition is measured +/-400mV from the steady-state voltage.
- 4) MBE pin is an open drain, tested functionally.
- 5) Testing performed with Error Correction Code enabled (ECC-ON), customer use case always utilizes ECC-ON.

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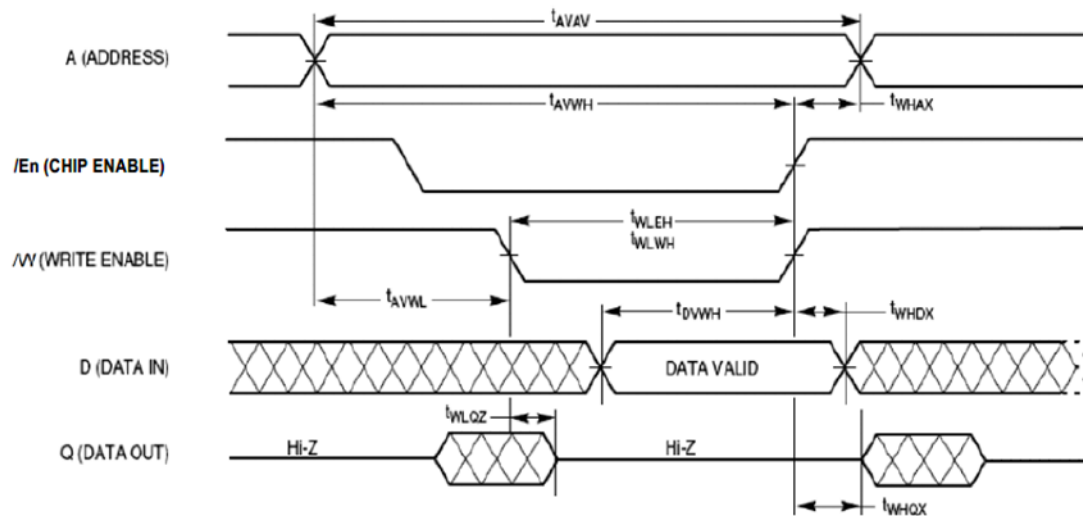


Figure 8a. MRAM Write Cycle 1 (/W Controlled Access)

AC Characteristics /En Controlled Write Cycle ¹ (Pre and Post-Radiation) * $V_{DD} = V_{DD}(\text{min})$; Unless otherwise noted, T_c is per the temperature ordered ^{5,6}

Symbol	Parameter	MIN	MAX	Unit
t_{AVAV}^2	Write cycle time	50		ns
t_{AVEL}	Address set-up time	0		ns
t_{AVEH}	Address valid to end of write (/G high)	28		ns
t_{AVEH}	Address valid to end of write (/G low)	28		ns
t_{ELEH} t_{ELWH}	Enable to end of write (/G high)	28		ns
t_{ELEH}^3 t_{ELWH}^3	Enable to end of write (/G low)	28		ns
t_{DVEH}	Data valid to end of write	10		ns
t_{EHDX}^4	Data hold time	0		ns
t_{EHAX}^4	Write recovery time	16		ns

Notes:

*For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

- 1) All write occurs during the overlap of /En low and /W low. Power supplies must be properly grounded and decoupled, and bus contention conditions must be minimized or eliminated during read or write cycles. If /G goes low at the same time or after /W goes low, the output will remain in a high impedance state.
- 2) All write cycle timings are referenced from the last valid address to the first transition address.
- 3) If /En goes low at the same time or after /W goes low, the output will remain in a high-impedance state. If /En goes high at the same time or before /W goes high, the output will remain in a high-impedance state.
- 4) Transition is measured +/-400mV from the steady-state voltage.
- 5) MBE pin is an open drain, tested functionally.
- 6) Testing performed with Error Correction Code enabled (ECC-ON), customer use case always utilizes ECC-ON.

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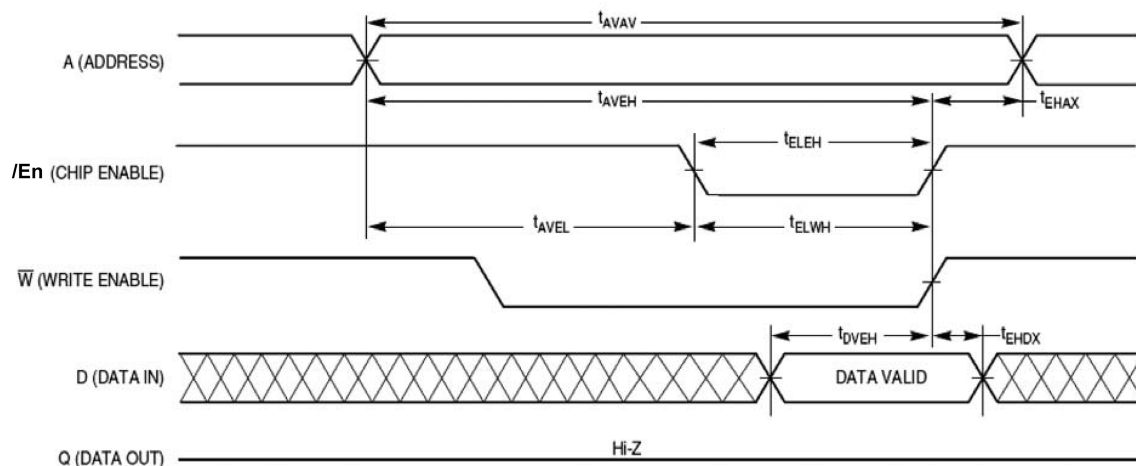


Figure 8b. MRAM Write Cycle 2 (/En Controlled)

AC Characteristics SLEEP/RESET Mode (Pre and Post-Radiation) * $V_{DD} = V_{DD}(\text{min})$; Unless otherwise noted, T_c is per the temperature ordered ^{4,5}

Symbol	Parameter	MIN	MAX	Unit
$t_{zZL}^{1,3}$	Sleep/reset mode exit delay		100	μs
$t_{zZH}^{2,3}$	Sleep/reset mode access time	50		ns
t_{EZZ}^3	Sleep/reset mode exit setup time	0		ns
t_{zZS}^3	Sleep/reset mode settle time		200	μs

Notes:

*For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

- 1) /En and /W must be high for the entire time when ZZ/RST is pulled low in order to exit sleep/reset mode.
- 2) ZZ/RST must be high for 40ns in order to enter sleep/reset mode.
- 3) Parameters are supplied as a design limit, but are not tested nor guaranteed.
- 4) MBE pin is an open drain, tested functionally.
- 5) Testing performed with Error Correction Code enabled (ECC-ON), customer use case always utilizes ECC-ON.

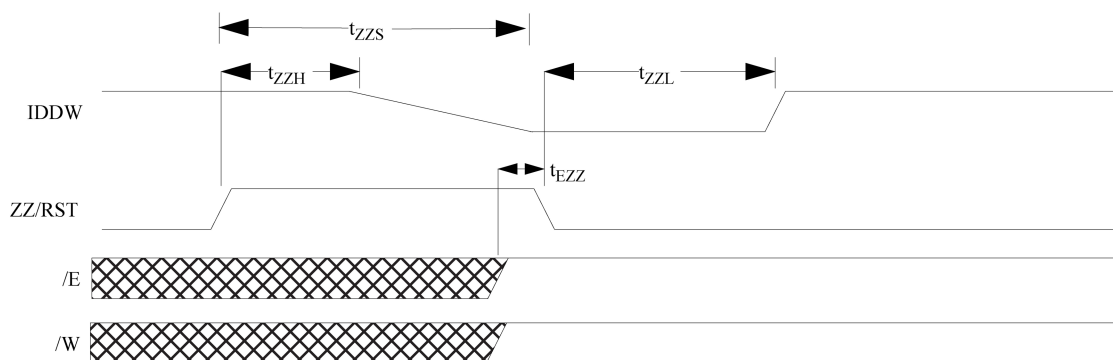


Figure 9. MRAM Sleep/Reset Mode Timing Diagram

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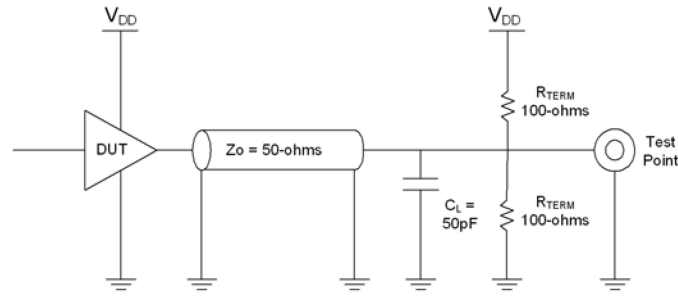


Figure 10. AC Output Test Load or Equivalent

Note:

- 1) Measurement of data output occurs at the low to high or high to low transition mid-point, typically, $V_{DD}/2$.

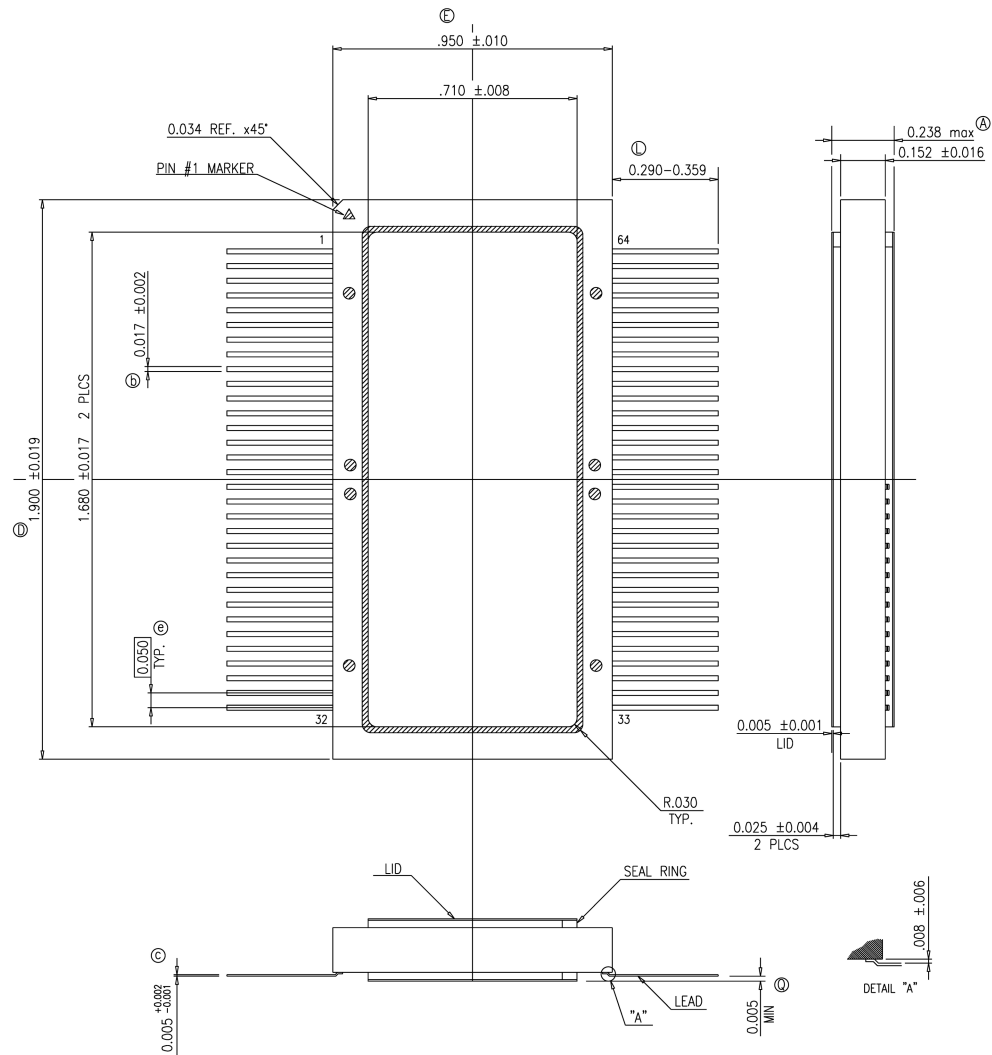


Figure 11. 64-Pin Ceramic Flatpack

Notes:

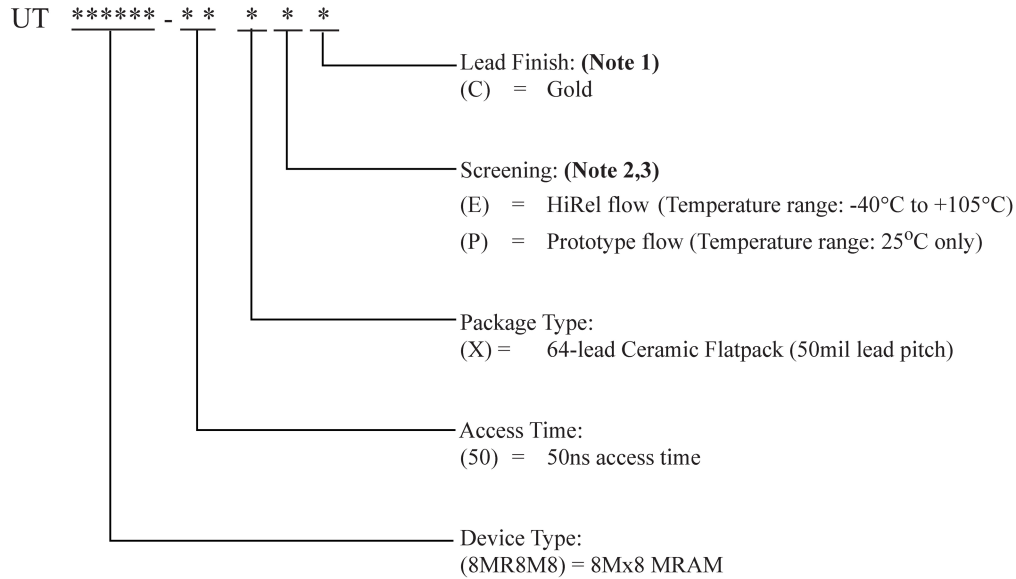
- 1) Lid is connected to VSS
- 2) Units are in inches

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Ordering Information

8M x 8 MRAM:



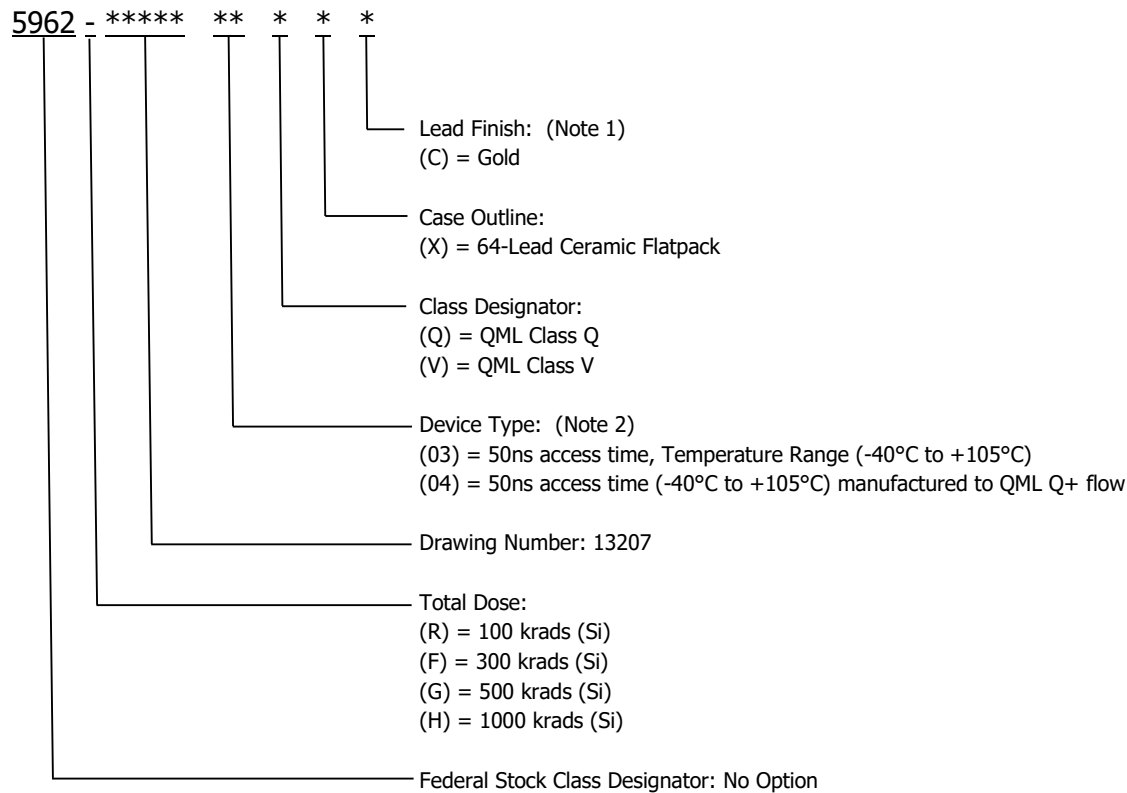
Notes:

- 1) Lead finish is "C" (Gold) only.
- 2) Prototype flow per Frontgrade Colorado Springs Manufacturing Flows Document. Radiation neither tested nor guaranteed.
- 3) HiRel Temperature Range flow per Frontgrade Colorado Springs Manufacturing Flows Document. Radiation neither tested nor guaranteed.

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8M x 8 MRAM: SMD



Notes:

- 1) Lead finish is "C" (Gold) only.
- 2) Frontgrade Q+ flow, as defined in Section 4.2.2d of SMD, provides QML-Q product through the SMD that is manufactured with Frontgrade standard QML-V flow.

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Data Sheet Revision History

Revision Date	Description of Change	Page(s)
January 2016	Added new CAES datasheet template, QML V Achieved, added ZZ/RST description of internal pull-down, updated maximum junction temperature to 150C, changed unit from uA to mA for the IINZZ specification, and added MBE Functionality verbiage and diagrams.	All
November 2017	Removed (T) Prototype flow (Temperature range: -40 to +105C) as an ordering option.	14
July 2018	Added package weight. Edited Device Operation paragraph. Edited MBE Pin Functionality and Sequencing paragraph. Edited Recommended Operating Conditions VIH and added note 2.	1,4,6,8
Sept 2019	Marked QML V from page 1 features list as pending. Replaced device type 01 and 02 with 03 and 04 and noted QML V option on page 16 "pending contact factory". Added note 3. to page 7 for tGLQV clarification. Previous note 3 is now 4.	1,2,4,6,12
Dec 2020	Removed note from page 1 and page 15 that QML V pending, replaced the word aeroflex with Cobham in body of document. Changed PD from 4W to 9W in abs max table, also changed note 3 for abs max table to more common PD= $T_{jmax} - T_{cmax} / \theta_{JC}$, added notes that MBE is open drain and tested functionally along with ECC-ON always enabled to all DC and AC char tables. Correct figure 8a as it was distorted in previous datasheet.	
Nov 2022	Changed format to Frontgrade (all pages). Added (multiple-bit-error) definition after MBE, pg1. Removed yellow border figure 2, clarified MBE low statement under device operation, pg 2. Changed paragraph name MBE Pin Functionality and Sequencing to MBE Output Initialization, made several editorial clarifications in paragraph, corrected figure 5 changing MBE valid to MBE initialization, pg5. Corrected figure 6 MBE valid to initialization, pg6.	1,2,5,6 MJL

64Megabit Non-Volatile MRAM

UT8MR8M8

Datasheet Definitions

	DEFINITION
Advanced Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet is subject to change . Specifications can be TBD and the part package and pinout are not final .
Preliminary Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

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