FRONTGRADE DATASHEET RELEASED 03/23

Monolithic 16M SRAM

UT8ER512K32

Features

- 20ns Read, 10ns Write maximum access times
- Functionally compatible with traditional 512K x 32 SRAM devices
- CMOS compatible input and output levels, three-state bidirectional data bus
  - I/O Voltage 3.3 volt, 1.8 volt core
- Operational environment:
  - Total-dose: 100 krad(Si)
  - SEL Immune: ≤111 MeV-cm^2/mg
  - SEU error rate = 8.1x10^{-16} errors/bit-day assuming geosynchronous orbit, Adam's 90% worst environment, and 6600ns default Scrub Rate Period (=97% SRAM availability)
- Packaging options:
  - 68-lead ceramic quad flatpack (6.898 grams)
- Standard Microcircuit Drawing 5962-06261
  - QML Q & V

Introduction

The UT8ER512K32 is a high-performance CMOS static RAM organized as 524,288 words by 32 bits. Easy memory expansion is provided by active LOW and HIGH chip enables ($\overline{E1}$, E2), an active LOW output enable ($\overline{G}$), and three-state drivers. This device has a power-down feature that reduces power consumption by more than 90% when deselected.

Writing to the device is accomplished by driving chip enable one ($\overline{E1}$) input LOW, chip enable two (E2) HIGH and write enable ($\overline{W}$) input LOW. Data on the 32 I/O pins (DQ0 through DQ31) is then written into the location specified on the address pins (A0 through A18). Reading from the device is accomplished by taking chip enable one ($\overline{E1}$) and output enable ($\overline{G}$) LOW while forcing write enable ($\overline{W}$) and chip enable two (E2) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The 32 input/output pins (DQ0 through DQ31) are placed in a high impedance state when the device is deselected ($\overline{E1}$ HIGH or E2 LOW), the outputs are disabled ($\overline{G}$ HIGH), or during a write operation ($\overline{E1}$ LOW, E2 HIGH and $\overline{W}$ LOW).

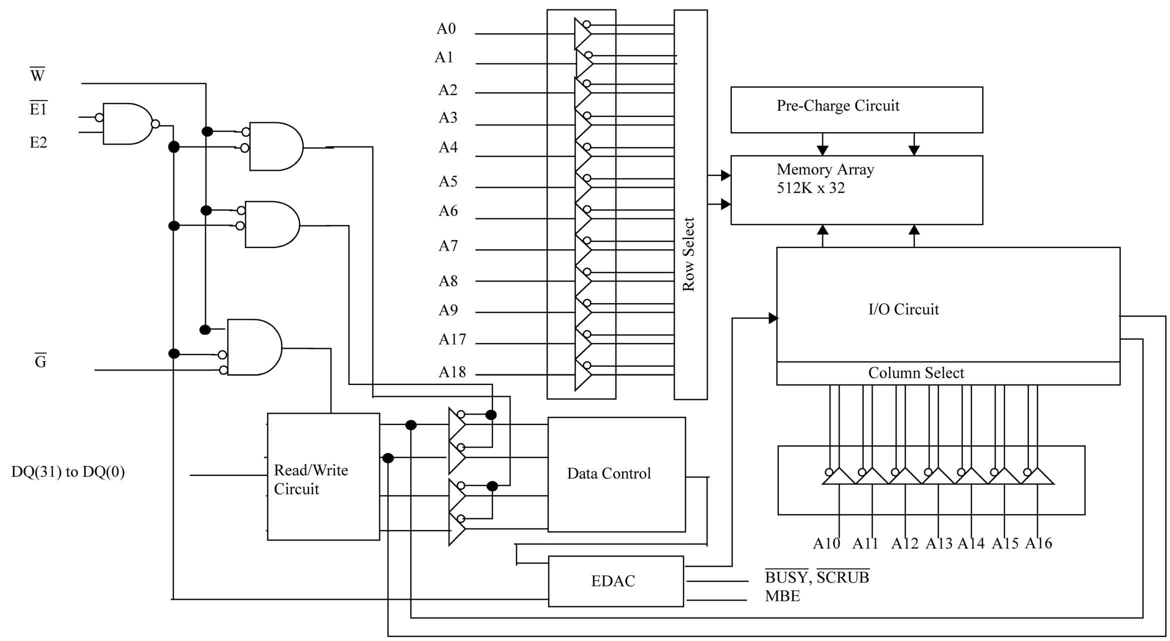


Figure 1. UT8ER512K32 SRAM Block Diagram

UT8ER512K32 Master or Slave Options

To reduce the bit error rates, the UT8ER512K32 employs an embedded EDAC (error detection and correction) with user programmable auto scrubbing options. The UT8ER512K32 device automatically corrects single bit word errors in event of an upset. During a read operation, if a multiple bit error occurs in a word, the UT8ER512K32 asserts the MBE (multiple bit error) output to notify the host.

The UT8ER512K32 is offered in two options: Master (UT8ER512K32M) or Slave (UT8ER512K32S). The master is a full function device which features user defined autonomous EDAC scrubbing options. The slave device employs a scrub on demand feature.

The UT8ER512K32M (master) and UT8ER512K32S (slave) device pins $\overline{\text{SCRUB}}$ and $\overline{\text{BUSY}}$ are physically different. The $\overline{\text{SCRUB}}$ pin is an output on master devices, but an input on slave devices. The master $\overline{\text{SCRUB}}$ pin asserts low when a scrub cycle initiates, and can be used to demand scrub cycles from multiple slave units when connected to the $\overline{\text{SCRUB}}$ input of slave(s). The $\overline{\text{BUSY}}$ pin is an output for the master device and can be used to generate wait states by the memory controller. The $\overline{\text{BUSY}}$ pin is a no connect (NC) for slave units.

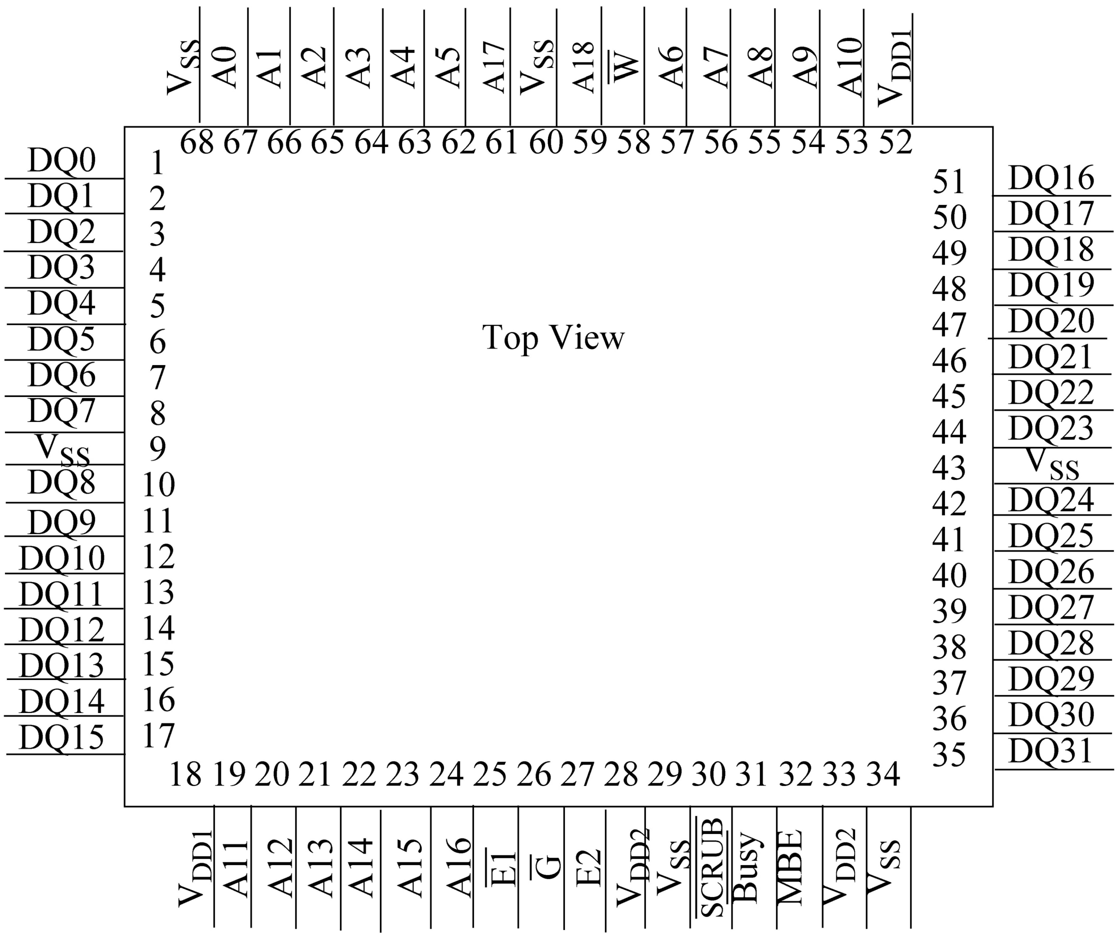


Figure 2. 20ns SRAM Pinout (68)

Note:

1) Pin 31 on the UT8ER512K32S (Slave) is a no connect (NC).

Pin Descriptions

Pins	Type	Description
A(18:0)	I	Address
DQ(31:0)	BI	Data Input/Output
$\overline{E1}$	I	Enable (Active Low)
E2	I	Enable (Active High)
$\overline{W}$	I	Write Enable
$\overline{G}$	I	Output Enable
V_{DD1}	P	Power (1.8)
V_{DD2}	P	Power (3.3V)
V_{SS}	P	Ground
MBE	BI	Multiple Bit Error
$\overline{SCRUB}$	I	Slave SCRUB Input
$\overline{SCRUB}$	O	Master SCRUB Output
$\overline{BUSY}$	NC	Slave No Connect
$\overline{BUSY}$	O	Master Wait State Control

Device Operation

The UT8ER512K32 has four control inputs called Enable 1 ($\overline{E1}$), Enable 2 (E2), Write Enable ($\overline{W}$), and Output Enable ($\overline{G}$); 19 address inputs, A(18:0); and 32 bidirectional data lines, DQ(31:0). $\overline{E1}$ and E2 device enables control device selection, active, and standby modes. Asserting $\overline{E1}$ and E2 enables the device, causes I_{DD} to rise to its active value, and decodes the 19 address inputs to select one of 524,288 words in the memory. $\overline{W}$ controls read and write operations. During a read cycle, $\overline{G}$ must be asserted to enable the outputs.

Table 1. SRAM Device Control Operation Truth Table

$\overline{G}$	$\overline{W}$	E2	$\overline{E1}$	I/O Mode	Mode
X	X	X	H	DQ(31:0) 3-State	Standby
X	X	L	X	DQ(31:0) 3-State	Standby
L	H	H	L	DQ(31:0) Data Out	Word Read
H	H	H	L	DQ(31:0) All 3-State	Word Read [2]
X	L	H	L	DQ(31:0) Data In	Word Write

Notes:
1) "X" is defined as a "don't care" condition.
2) Device active; outputs disabled.

Table 2. EDAC Control Pin Operation Truth Table

MBE	$\overline{SCRUB}$	$\overline{BUSY}$	I/O Mode	Mode
H	H	H	Read	Uncorrectable Multiple Bit Error
L	H	H	Read	Valid Data Out
X	H	H	X	Device Ready
X	H	L	X	Device Ready / Scrub Request Pending
X	L	X	Not Accessible	Device Busy

Notes:

1) "X" is defined as a "don't care" condition
2) $\overline{BUSY}$ signal is a "NC" for UT8ER512K32S slave device and is an "X" don't care.

Read Cycle

A combination of $\overline{W}$ and E2 greater than V_{IH} (min) and $\overline{E1}$ and $\overline{G}$ less than V_{IL} (max) defines a read cycle. Read access time is measured from the latter of device enable, output enable, or valid address to valid data output. Read cycles initiate with the assertion of chip enable or any address change while chip enable is asserted.

SRAM Read Cycle 1, the Address Access in Figure 3a, is initiated by a change in address inputs while $\overline{E1}$ and E2 are asserted, $\overline{G}$ is asserted, and $\overline{W}$ is deasserted. Valid data appears on data outputs DQ(31:0) after the specified t_{AVQV} is satisfied. Outputs remain active throughout the entire cycle. As long as device enable and output enable are active, the minimum time between valid address changes is specified by the read cycle time (t_{AVAV}). Changing addresses prior to satisfying tAVAV minimum results in an invalid operation. Invalid read cycles will require re-initialization.

SRAM Read Cycle 2, the Chip Enable-controlled Access in Figure 3b, is initiated by the latter of either $\overline{E1}$ and E2 going active while $\overline{G}$ remains asserted, $\overline{W}$ remains deasserted, and the addresses remain stable for the entire cycle. After the specified t_{ETQV} is satisfied, the 32-bit word addressed by A(18:0) is accessed and appears at the data outputs DQ(31:0).

SRAM Read Cycle 3, the Output Enable-controlled Access in Figure 3c, is initiated by $\overline{G}$ going active while $\overline{E1}$ and E2 are asserted, $\overline{W}$ is deasserted, and the addresses are stable. Read access time is t_{GLQV} unless t_{AVQV} or t_{ETQV} (reference Figure 3b) have not been satisfied.

SRAM EDAC Status Indications during a Read Cycle, if MBE is Low, the data is good. If MBE is High the data is corrupted (reference Table 2).

Write Cycle

A combination of $\overline{W}$ and $\overline{E1}$ less than V_{IL}(max), and E2 greater than V_{IH}(min) defines a write cycle. The state of $\overline{G}$ is a "don't care" for a write cycle. The outputs are placed in the high- impedance state when either $\overline{G}$ is greater than V_{IH}(min), or when $\overline{W}$ is less than V_{IL}(max).

Write Cycle 1, the Write Enable-controlled Access in Figure 4a, is defined by a write terminated by $\overline{W}$ going high, with $\overline{E1}$ and E2 still active. The write pulse width is defined by t_{WLWH} when the write is initiated by $\overline{W}$, and by t_{ETWH} when the write is initiated by $\overline{E1}$ and E2. To avoid bus contention t_{WLQZ} must be satisfied before data is applied to the 32 bidirectional pins DQ(31:0) unless the outputs have been previously placed in high impedance state by deasserting $\overline{G}$.

Write Cycle 2, the Chip Enable-controlled Access in Figure 4b, is defined by a write terminated by the latter of $\overline{E1}$ or E2 going inactive. The write pulse width is defined by t_{WLEF} when the write is initiated by $\overline{W}$, and by t_{ETEF} when the write is initiated by either $\overline{E1}$ or E2 going active. For the $\overline{W}$ initiated write, unless the outputs have been previously placed in the high-impedance state by $\overline{G}$, the user must wait t_{WLQZ} before applying data to the thirty-two bidirectional pins DQ(31:0) to avoid bus contention.

Control Register Write/Read Cycles

Configuration options can be selected by writing to the control register. The configuration table (Table 4) details the programming options. The control register is accessed by applying a series of values to the address bus as shown in Figure 6a. The contents of the control register are written following the fifth address. The contents of the address bus are written to the control register if bit 9 is zero. The contents of the control register are output to the data bus if bit 9 is one. **Note:** MBE must be driven high by the user for both a write or a read of the control register.

Memory Scrubbing/Cycle Stealing

The UT8ER512K32 SRAM uses architectural improvements and embedded error detection and correction to maintain unsurpassed levels of error protection. This is accomplished by what Frontgrade refers to as Cycle Stealing. To minimize the system design impact on the speed of operation, the edge relationship between $\overline{BUSY}$ and $\overline{SCRUB}$ is programmable via the sequence described in figure 6a.

The effective error rate is a function of the intrinsic rate and the environment. As a result, some users may desire an increased scrub rate to lower the error rate at the sacrifice of reduced total throughput, while others may desire a lower scrub rate to increase the total throughput and accept a higher error rate. This rate at which the SRAM controller will correct errors from the memory is user programmable. The required sequence is described in figure 6a.

A master mode scrub cycle will occur at the user defined Scrub Rate Period. A scrub cycle is defined as the verification and correction (if necessary) of data for a single word address location. Address locations are scrubbed sequentially every Scrub Rate Period (t_{SCRT}). Scrub cycles will occur at every Scrub Rate Period regardless of the status of control pins. Control pin function will be returned upon deassertion of $\overline{BUSY}$ pin. The Slave mode scrub cycle occurs anytime the $\overline{SCRUB}$ pin is asserted. The scrub cycle is defined the same as the master mode, and will occur regardless of control pin status. Control pin function will be returned upon $\overline{SCRUB}$ deassertion.

Data is not only corrected during the internal scrub, but again during a user requested read cycle. If the data presented contains two or more errors after t_{AVAV} is satisfied, the MBE signal will be asserted. (Note: Reading un-initialized memory locations may result in un-intended MBE assertions.)

Operational Environment

The UT8ER512K32 SRAM incorporates special design, layout, and process features which allows operation in a limited environment.

Table 3. Operational Environment Design Specifications [1]

Total Dose	100K	rad(Si)
Heavy Ion Error Rate [2]	8.1×10^{-16}	Errors/Bit-Day

Notes:

1) The SRAM is immune to latchup to particles ≤111MeV-cm^2/mg.
2) 90% worst case particle environment, Geosynchronous orbit, 100 mils of Aluminum and default EDAC scrub rate.

Supply Sequencing

No supply voltage sequencing is required between V_{DD1} and V_{DD2}.

Power-Up Requirements

During power-up of the UT8ER512K32 device, the power supply voltages will transverse through voltage ranges where the device is not guaranteed to operate before reaching final levels. Since some circuits on the device will start to operate at lower voltage levels than others, the device may power-up in an unknown state. To eliminate this with most power-up situations, the device employs an on-chip power-on-reset (POR) circuit. The POR, however, requires time to complete the operation. Therefore, it is recommended that all device activity be delayed by a minimum of 100ms, after both V_{DD1} and V_{DD2} supplies have reached their respective minimum operating voltage.

UT8ER512K32

Absolute Maximum Ratings [1]

(Referenced to V_{SS})

Symbol	Parameter	Limits
V_{DD1}	DC supply voltage (Core)	-0.3 to 2.4V
V_{DD2}	DC supply voltage (I/O)	-0.3 to 4.5V
$V_{I/O}$	Voltage on any pin	-0.3 to 4.5V
T_{STG}	Storage temperature	-65 to +150°C
P_D [2]	Maximum package power dissipation permitted @ Tc = +125°C	5W
T_J	Maximum junction temperature	+150°C
Θ_{JC}	Thermal resistance, junction-to-case [2]	5°C/W
I_I	DC input current	±10mA

Notes:

1) Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2) Per MIL-STD-883, Method 1012, Section 3.4.1, $P_D = \frac{(T_{JC}(max) - T_C(max))}{\Theta_{JC}}$

Recommended Operating Conditions

Symbol	Parameter	Limit
V_{DD1}	DC supply voltage (Core)	1.7 to 1.9V [1]
V_{DD2}	DC supply voltage (I/O)	3.0 to 3.6V
T_C	Case temperature range	(C) Screening: -55 to +125°C (W) Screening: -40 to +125°C
V_{IN}	DC input voltage	0V to V_{DD2}

Note:

1) For increased noise immunity, supply voltage V_{DD1} can be increased to 2.0V. All characteristics contained herein are guaranteed by characterization at V_{DD1} = 2.0Vdc unless otherwise specified.

DC Electrical Characteristics (Pre and Post-Radiation)*

(Tc = -55°C to +125°C For (C) Screening And -40°C to +125°C for (W) Screening) (V_{DD1} = 1.7V to 1.9V; V_{DD2} = 3.0V to 3.6V)

Symbol	Parameter	Condition			MIN	MAX	Unit
V_{IH}	High-level input voltage				0.7*V_{DD2}		V
V_{IL}	Low-level input voltage					0.3*V_{DD2}	V
V_{OL} [1]	Low-level output voltage	I_{OL} = 8mA,V_{DD2} =V_{DD2} (min)				0.2*V_{DD2}	V
V_{OH}	High-level output voltage	I_{OH} = -4mA,V_{DD2} =V_{DD2} (min)			0.8*V_{DD2}		V
C_{IN} [2]	Input capacitance	f= 1MHz @ 0V				12	pF
C_{IO} [2]	Bidirectional I/O capacitance	f= 1MHz @ 0V				12	pF
I_{IN}	Input leakage current	V_{IN} = V_{DD2} and V_{SS}			-2	2	µA
I_{OZ} [3]	Three-state output leakage current	V_O = V_{DD2} and V_{SS} V_{DD2} = V_{DD2} (max), $\overline{G}$ = V_{DD2} (max)			-2	2	µA
I_{OS} [4, 5]	Short-circuit output current	V_{DD2} = V_{DD2} (max), V_O = V_{DD2} V_{DD2} = V_{DD2} (max), V_O = V_{SS}			-100	+100	mA
I_{DD1}(OP$_1$ [6, 7, 8])	V_{DD1} Supply current operating @ 1MHz, EDAC enabled @ default Scrub Rate Period (see table 4).	Inputs: V_{IL} = V_{SS} + 0.2V, V_{IH} = V_{DD2} -0.2V, I_{OUT} = 0 V_{DD1} = V_{DD1} (max), V_{DD2} = V_{DD2} (max)	-55°C and 25°C			25	mA
			V_{DD1}= 2.0V	125°C		70	mA
			V_{DD1}= 1.9V	125°C		65	mA
I_{DD1}(OP$_2$ [6, 7, 8])	V_{DD1} Supply current operating @ 50MHz, EDAC enabled @ default Scrub Rate Period (see table 4).	Inputs: V_{IL} = V_{SS} + 0.2V, V_{IH} = V_{DD2} -0.2V, I_{OUT} = 0 V_{DD1} = V_{DD1} (max), V_{DD2} = V_{DD2} (max)	-55°C and 25°C			250	mA
			V_{DD1} = 2.0V	125°C		300	mA
			V_{DD1}= 1.9V	125°C		270	mA
I_{DD2}(OP$_1$ [6,8])	V_{DD2} Supply current operating @ 1MHz, EDAC enabled @ default Scrub Rate Period (see table 4).	Inputs: V_{IL} = V_{SS} + 0.2V, V_{IH} = V_{DD2} -0.2V, I_{OUT} = 0 V_{DD1} = V_{DD1} (max), V_{DD2} = V_{DD2} (max)				2	mA
I_{DD2}(OP$_2$ [6, 8])	V_{DD2} Supply current operating @ 50MHz, EDAC enabled @ default Scrub Rate Period (see table 4).	Inputs: V_{IL} = V_{SS} + 0.2V, V_{IH} = V_{DD2} -0.2V, I_{OUT} = 0 V_{DD1} = V_{DD1} (max), V_{DD2} = V_{DD2} (max)				5	mA
I_{DD1}(SB) [7, 9]	Supply current standby @ 0Hz, EDAC bypassed	CMOS inputs, I_{OUT} = 0 $\overline{E1}$ = V_{DD2}-0.2, E2 = GND V_{DD1} = V_{DD1} (max), V_{DD2} = V_{DD2} (max)	-55°C and 25°C			25	mA
			125°C			70	mA
I_{DD2}(SB) [9]	Supply current standby @ 0Hz, EDAC bypassed	CMOS inputs, I_{OUT} = 0 $\overline{E1}$ = V_{DD2}-0.2, E2 = GND V_{DD1} = V_{DD1} (max), V_{DD2} = V_{DD2} (max)				2	mA

Symbol	Parameter	Condition		MIN	MAX	Unit
I_{DD1}(SB) [7, 9]	Supply current standby A(18:0) @ 50MHz, EDAC bypassed	CMOS inputs, I_{OUT} = 0 $\overline{E1}$ = V_{DD2}-0.2, E2 = GND V_{DD1} = V_{DD1} (max), V_{DD2} = V_{DD2} (max)	-55°C and 25°C		25	mA
			125°C		70	mA
I_{DD2}(SB) [9]	Supply current standby A(18:0) @ 50MHz, EDAC bypassed	CMOS inputs, I_{OUT} = 0 $\overline{E1}$ = V_{DD2}-0.2, E2 = GND V_{DD1} = V_{DD1} (max), V_{DD2} = V_{DD2} (max)			2	mA

Notes:
*For devices procured with a total ionizing dose tolerance, the post-irradiation performance is guaranteed.

1) The $\overline{SCRUB}$ and $\overline{BUSY}$ pins for UT8ER512K32M (master) are tested functionally for VOL specification.
2) Measured only for initial qualification and after process or design changes that could affect input/output capacitance.
3) The $\overline{SCRUB}$ and $\overline{BUSY}$ pins for UT8ER512K32M (master) are guaranteed by design, but neither tested nor characterized.
4) Supplied as a design limit but not guaranteed or tested.
5) Not more than one output may be shorted at a time for maximum duration of one second.
6) EDAC enabled. Default Scrub Rate Period applicable to master device only.
7) Post radiation limits are the 125°C temperature limit when specified.
8) Operating current limit includes standby current.
9) V_{IH} = V_{DD2} (max), V_{IL} = 0V.

AC Characteristics Read Cycle (Pre- and Post-Radiation) *

(Tc = -55°C to +125°C for (C) screening and -40°C to +125°C for (W) screening, V_{DD1} = 1.7V to 1.9V, V_{DD2} = 3.0V to 3.6V)

Symbol	Parameter	MIN	MAX	Unit	Figure
t_{AVAV1} [1,6]	Read cycle time	20		ns	3a
t_{AVSK} [5]	Address valid to address valid skew time		4	ns	3a
t_{AVQV1}	Address to data valid from address change		20	ns	3c
t_{AXQX} [2]	Output hold time	3		ns	3a
t_{GLQX} [1, 2]	$\overline{G}$-controlled output enable time	2		ns	3c
t_{GLQV}	$\overline{G}$-controlled output data valid		8	ns	3c
t_{GHQZ1} [2]	$\overline{G}$-controlled output three-state time	2	6	ns	3c
t_{ETQX} [2, 3]	$\overline{E}$-controlled output enable time	5		ns	3b
t_{AVET2} [5]	Address setup time for read ($\overline{E}$-controlled)	-4		ns	3b
t_{ETQV} [3]	$\overline{E}$-controlled access time		20	ns	3b
t_{EFQZ} [2, 4]	$\overline{E}$-controlled output three-state time [2]	2	7	ns	3b
t_{AVMV}	Address to error flag valid		20	ns	3a
t_{AXMX} [2]	Address to error flag hold time from address change	3		ns	3a
t_{GLMX} [2]	$\overline{G}$-controlled error flag enable time	2		ns	3c
t_{GLMV}	$\overline{G}$-controlled error flag valid		7	ns	3c
t_{ETMX} [2]	$\overline{E}$-controlled error flag enable time	5		ns	3b
t_{ETMV} [3]	$\overline{E}$-controlled error flag time		20	ns	3b
t_{GHMZ} [2]	G-controlled error flag three-state time	2	6	ns	3b

Notes:

*For devices procured with a total ionizing dose tolerance, the post-irradiation performance is guaranteed.

1) Guaranteed by characterization, but not tested.
2) Three-state is defined as a 300mV change from steady-state output voltage.
3) The ET (enable true) notation refers to the latter falling edge of $\overline{E1}$ or rising edge of E2.
4) The EF (enable false) notation refers to the latter rising edge of $\overline{E1}$ or falling edge of E2.
5) Guaranteed by design
6) Address changes prior to satisfying t_{AVAV} minimum is an invalid operation

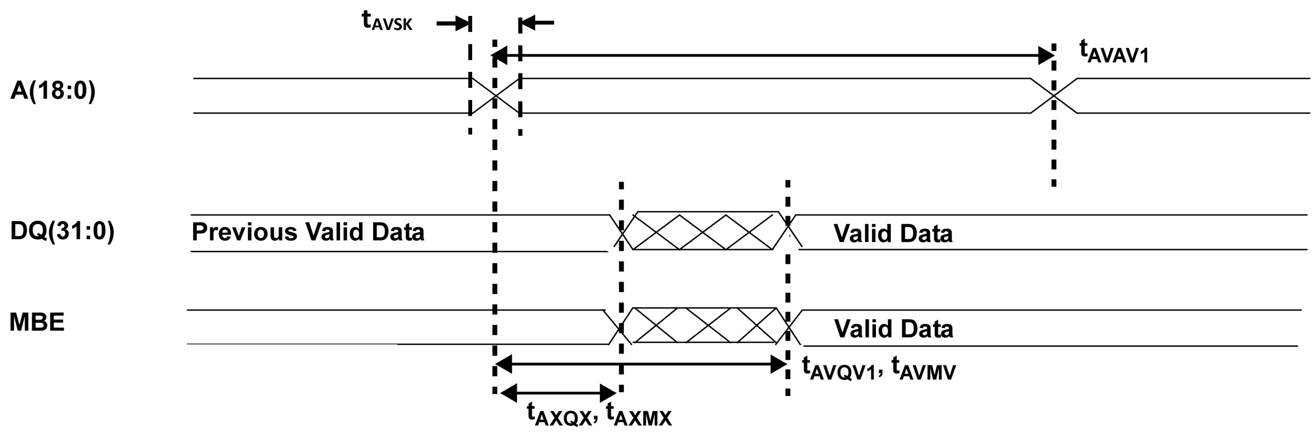


Figure 3a. SRAM Read Cycle 1: Address Access

Assumptions:

1) $\overline{E1}$ and $\overline{G}$ ≤ V_{IL} (max) and E2 and $\overline{W}$ ≥ V_{IH} (min)
2) $\overline{SCRUB}$ ≥ V_{OH} (min)
3) Reading uninitialized addresses will cause MBE to be asserted.

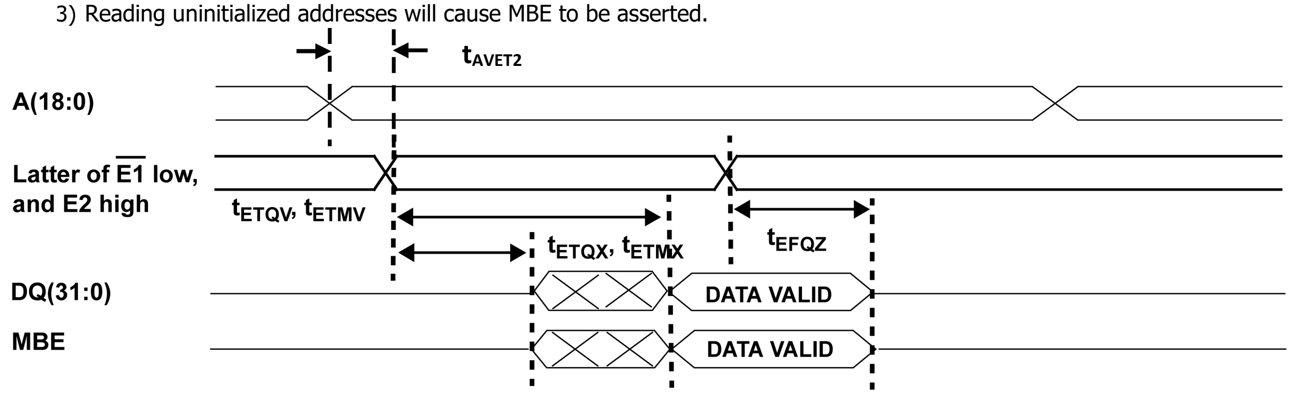


Figure 3b. SRAM Read Cycle 2: Chip Enable Access

Assumptions:

1) $\overline{G}$ ≤ V_{IL} (max) and $\overline{W}$ ≥ V_{IH} (min)
2) $\overline{SCRUB}$ ≥ V_{OH} (min)
3) Reading uninitialized addresses will cause MBE to be asserted.

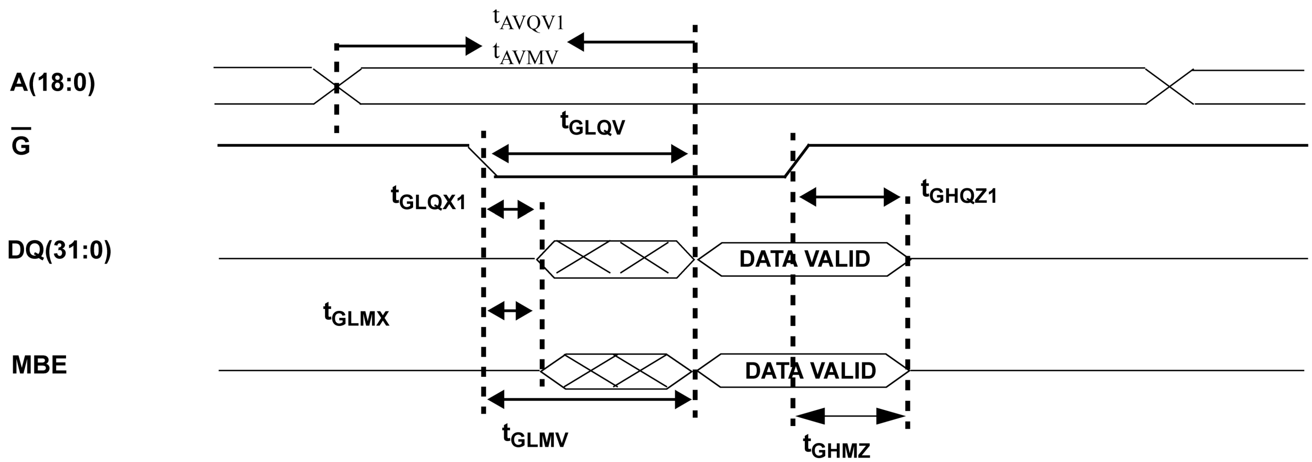


Figure 3c. SRAM Read Cycle 3: Output Enable Access

Assumptions:

1) $\overline{E1} \leq V_{IL}$ (max), E2 and $\overline{W} \geq V_{IH}$ (min)
2) $\overline{SCRUB} \geq V_{OH}$ (min)
3) Reading uninitialized addresses will cause MBE to be asserted.

AC Characteristics Write Cycle (Pre- and Post-Radiation) *

(Tc = -55°C to +125°C for (C) screening and -40°C to +125°C for (W) screening, V_{DD1} = 1.7V to 1.9V, V_{DD2} = 3.0V to 3.6V)

Symbol	Parameter	MIN	MAX	Unit	Figure
t_{AVAV2} [1]	Write cycle time	10		ns	4a/4b
t_{ETWH}	Device Enable to end of write	10		ns	4a
t_{AVET}	Address setup time for write ($\overline{E1}$/E2- controlled)	0		ns	4b
t_{AVWL}	Address setup time for write ($\overline{W}$ - controlled)	0		ns	4a
t_{WLWH} [1]	Write pulse width	8		ns	4a
t_{WHAX}	Address hold time for write ($\overline{W}$ - controlled)	0		ns	4a
t_{EFAX}	Address hold time for Device Enable ($\overline{E1}$/E2- controlled)	0		ns	4b
t_{WLQZ} [2]	$\overline{W}$ - controlled three-state time		7	ns	4a/4b
t_{WHQX} [2]	$\overline{W}$ - controlled Output Enable time	3		ns	4a
t_{ETEF}	Device Enable pulse width ($\overline{E1}$/E2 - controlled)	10		ns	4b
t_{DVWH}	Data setup time	5		ns	4a
t_{WHDX}	Data hold time	2		ns	4a
t_{WLEF} [1]	Device Enable controlled write pulse width	8		ns	4b
t_{DVEF}	Data setup time	5		ns	4a/4b
t_{EFDX}	Data hold time	2		ns	4b
t_{AVWH}	Address valid to end of write	10		ns	4a
t_{WHWL} [1]	Write disable time	2		ns	4a

Notes:

*For devices procured with a total ionizing dose tolerance, the post-irradiation performance is guaranteed.

1) Tested with $\overline{G}$ high.
2) Three-state is defined as 300mV change from steady-state output voltage.

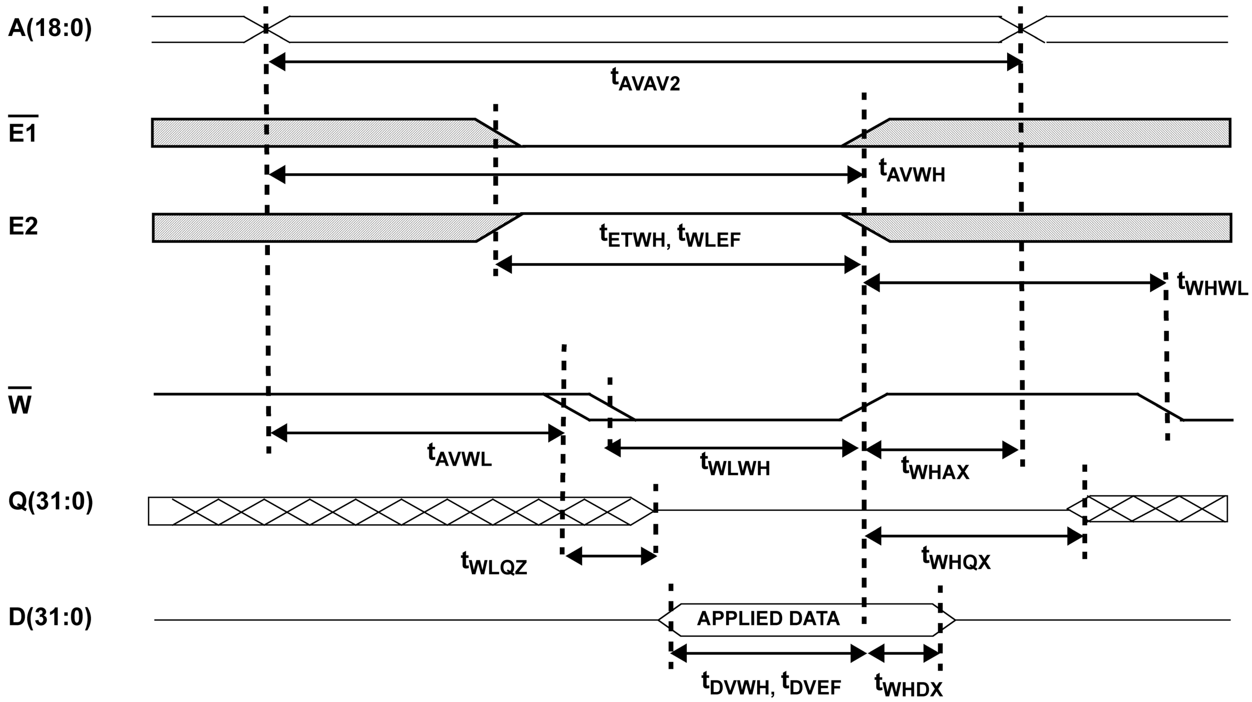


Figure 4a. SRAM Write Cycle 1: $\overline{W}$ - Controlled Access

Assumptions:

1) $\overline{G} \leq V_{IL}$ (max). (If $\overline{G} \geq V_{IH}$ (min) then Q(31:0) and MBE will be in three-state for the entire cycle.)
2) $\overline{SCRUB} \geq V_{OH}$ (min)

3)

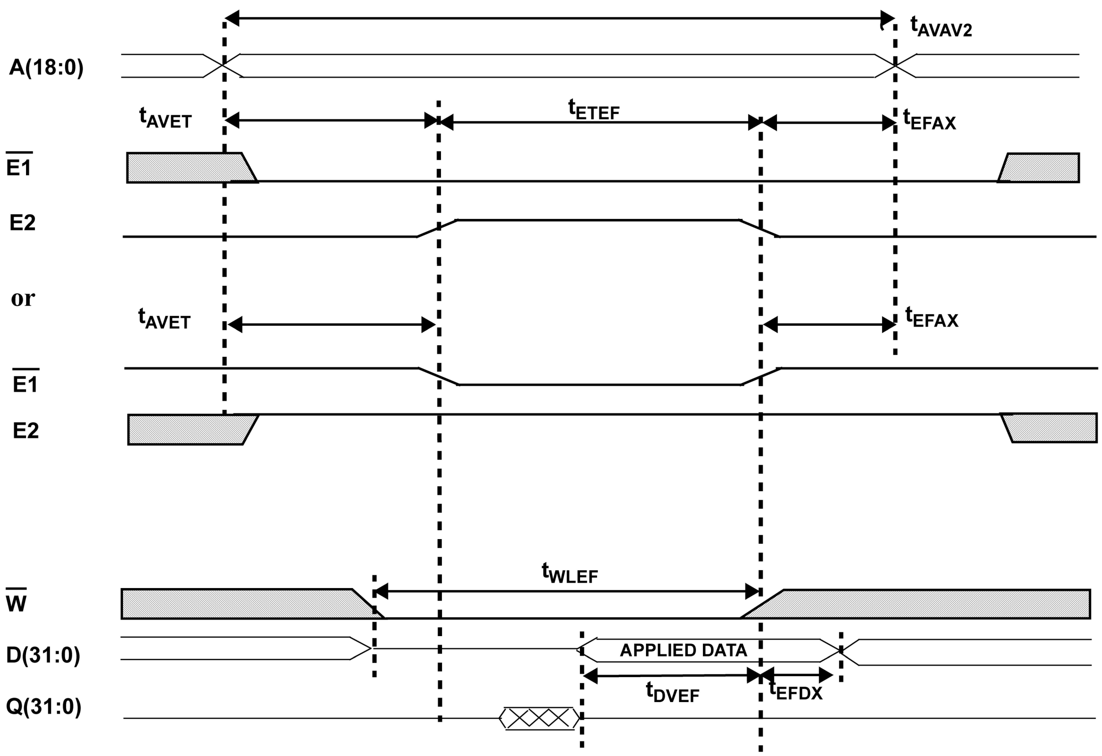


Figure 4b. SRAM Write Cycle 2: Enable - Controlled Access

Assumptions & Notes:

1) $\overline{G} \leq V_{IL}$ (max). (If $\overline{G} \geq V_{IH}$ (min) then Q(31:0) and MBE will be in three-state for the entire cycle.)
2) Either $\overline{E1}$ / E2 scenario can occur
3) $\overline{SCRUB} \geq V_{OH}$ (min)

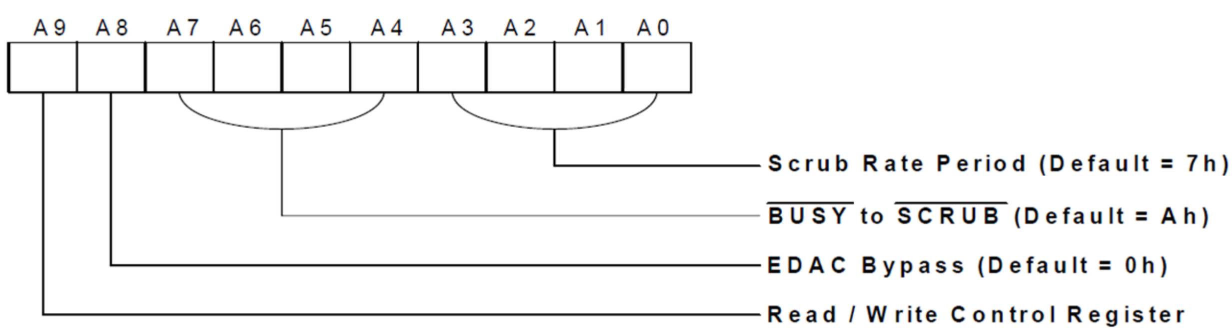


Figure 5. EDAC Control Register

Note:

1) See Table 4 for Control Register Definitions

UT8ER512K32

Table 4: EDAC Programming Configuration Table

ADDR BIT	Parameter	Value	Function
A (0 - 3)	Scrub Rate Period [1, 2, 3]	3-15 Note: 0-2 reserved	As Scrub Rate Period changes from 0 - 15, then the interval between Scrub cycles will change as follows: 3 = 600 ns 8 = 13.0 us 12 = 205 us 4 = 1000 ns 9 = 25.8 us 13 = 409.8 us[4] 5 = 1800 ns 10 = 51.4 us 14 = 819.4 us[4] 6 = 3400 ns 11 = 102.6 us 15 = 1.64 ms[4] 7 = 6600 ns
A (4 - 7)	$\overline{\text{BUSY}}$ to $\overline{\text{SCRUB}}$ [1, 3, 5]	0-15	If $\overline{\text{BUSY}}$ changes from 0 - 15, then the interval t_{BLSL} between $\overline{\text{SCRUB}}$ and $\overline{\text{BUSY}}$ will change as follows: 0 = 0 ns 6 = 300 ns 11 = 550 ns 1 = 50 ns 7 = 350 ns 12 = 600 ns 2 = 100 ns 8 = 400 ns 13 = 650 ns 3 = 150 ns 9 = 450 ns 14 = 700 ns 4 = 200 ns 10 = 500 ns 15 = 750 ns 5 = 250ns
A (8)	Bypass EDAC Bit [6]	0, 1	If 0, then normal EDAC operation will occur. If 1, then EDAC will be bypassed.
A (9)	Read / Write Control Register	0, 1	0 = A0 to A8 will be written to the control register 1 = Control register will be asserted to the data bus

Notes:

1) Values based on minimum specifications. For guaranteed ranges of Scrub Rate Period (t_{SCRT}) and $\overline{\text{BUSY}}$ to $\overline{\text{SCRUB}}$ (t_{BLSL}), reference the Master Mode AC Characteristic table.
2) Default Scrub Rate Period is 6600 ns.
3) Scrub Rate Period and $\overline{\text{BUSY}}$ to $\overline{\text{SCRUB}}$ applicable to the UT8ER512K32M device only.
4) Period below test capability.
5) The default for t_{BLSL} is 500 ns.
6) The default state for A8 is 0.

EDAC Control Register AC Characteristics (Pre- and Post-Radiation) *

(-55°C to +125°C for (C) screening and -40°C to +125°C for (W) screening, V_{DD1} = 1.7V to 1.9V, V_{DD2} = 3.0V to 3.6V

Symbol	Parameter	MIN	MAX	Unit	Figure
t_{AVAV3}	Address valid to address valid for control register cycle	200		ns	6a
t_{AVCL}	Address valid to control low	400		ns	6a
t_{AVEX}	Address valid to enable valid	200		ns	6a
t_{AVQV3}	Address to data valid control register read		400	ns	6a
t_{CHAV}	MBE high to address valid	0		ns	6a
t_{CLAX}	MBE low to address hold time	0		ns	6a
t_{MLQX} [1]	MBE control EDAC disable time	3		ns	6a
t_{GHQZ3} [1]	Output tri-state time	2	9	ns	6a
t_{MLGL} [2]	MBE low to output enable	85		ns	6a

Notes:
*For devices procured with a total ionizing dose tolerance, the post-irradiation performance is guaranteed.
1) Three-state is defined as 300mV change from steady-state output.
2) Guaranteed by design neither tested or characterized.

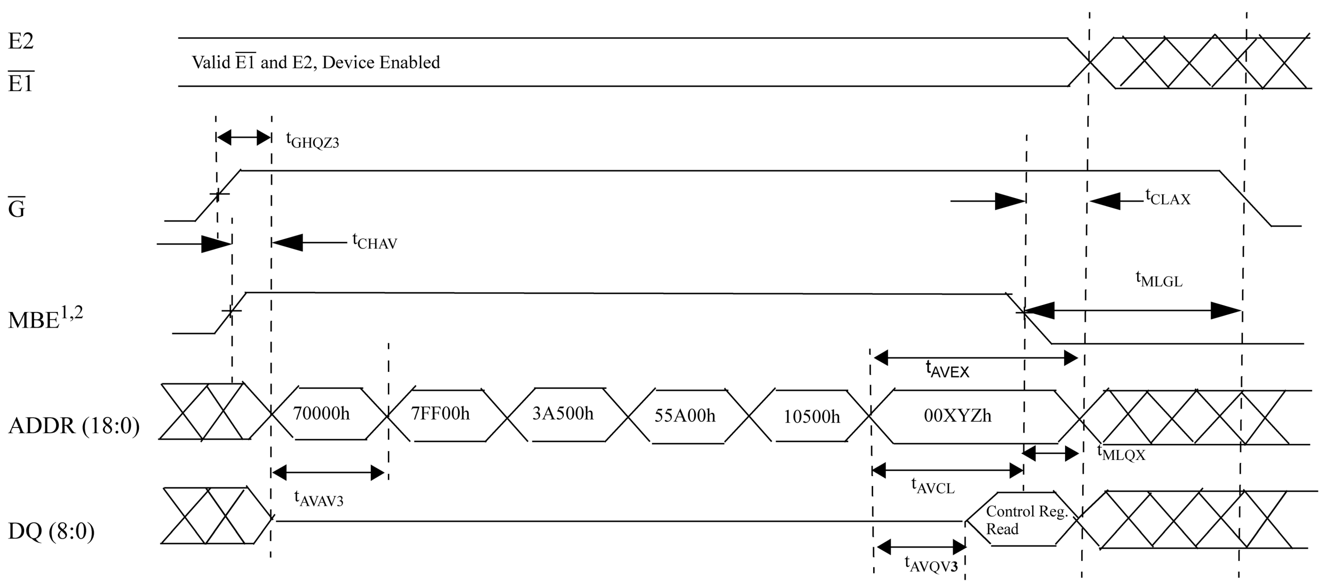


Figure 6a. EDAC Control Register Cycle

Notes:
1) MBE is driven high by the user.
2) Device must see a transition to address 70000h coincident with or subsequent to MBE assertion.
3) Lower 10 bits of the last address are used to read or configure the control register (ref Control Register Write/Read Cycles page 3 and Table 4).

Assumptions:
1) $\overline{SCRUB}$ ≥ V_{OH} before the start of the configuration cycle. Ignore $\overline{SCRUB}$ during configuration cycle.

Master Mode AC Characteristics (Pre- and Post-Radiation) *

(-55°C to +125°C for (C) screening and -40°C to +125°C for (W) screening, V_{DD1} = 1.7V to 1.9V, V_{DD2} = 3.0V to 3.6V

Symbol	Parameter	MIN	MAX	Unit	Figure
t_{BLSL} [1]	User Programmable - $\overline{\text{BUSY}}$ low to $\overline{\text{SCRUB}}$	(50)(n)	(90)(n)+1	ns	6b
t_{SLSH1}	$\overline{\text{SCRUB}}$ low to $\overline{\text{SCRUB}}$ high	200	350	ns	6b
t_{SHBH}	$\overline{\text{SCRUB}}$ high to $\overline{\text{BUSY}}$ high	50	85	ns	6b
t_{SCRT} [2]	Scrub Rate Period	$(2^n)(50)+200$	$(2^n)(90)+350$	ns	

Notes:

*For devices procured with a total ionizing dose tolerance, the post-irradiation performance is guaranteed.

1) See Table 4 for User Programmable information. The value "n" is decimal equivalent of hexidecimal value 0x0 through 0xF programmed into control register address bits A_4-A_7 by user. Default value "n" = 10.
2) See Table 4 for User Programmable information. The value "n" is decimal equivalent of hexidecimal value 0x3 through 0xF programmed into control register address bits A_0-A_3. Default value is “n” = 7.

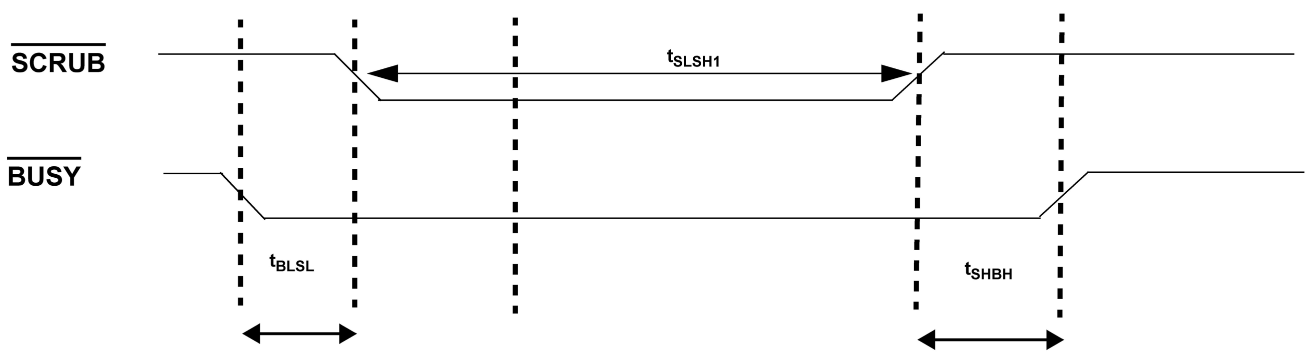


Figure 6b. Master Mode Scrub Cycle

Assumptions:

The conditions pertain to both a Read or Write.

UT8ER512K32

Slave Mode AC Characteristics (Pre and Post-Radiation) *

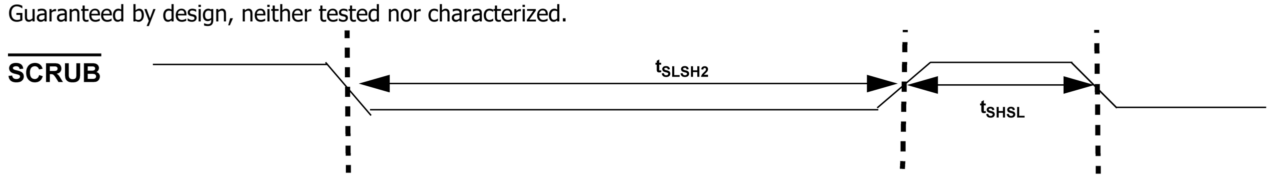
(-55°C to +125°C for (C) screening and -40°C to +125°C for (W) screening, V_{DD1} = V_{DD1}(min), V_{DD2} = V_{DD2}(min))

Symbol	Parameter	MIN	MAX	Unit	Figure
t_{SLSH2}	$\overline{SCRUB}$ low to $\overline{SCRUB}$ high (slave)	200		ns	6c
t_{SHSL} [1]	$\overline{SCRUB}$ high to $\overline{SCRUB}$ low (slave)	400		ns	6c

Note:

*For devices procured with a total ionizing dose tolerance, the post-irradiation performance is guaranteed.

1) Guaranteed by design, neither tested nor characterized.



1) ..

Figure 6c. Slave Mode Scrub Cycle

Assumption:

1) The conditions pertain to both a Read or Write.

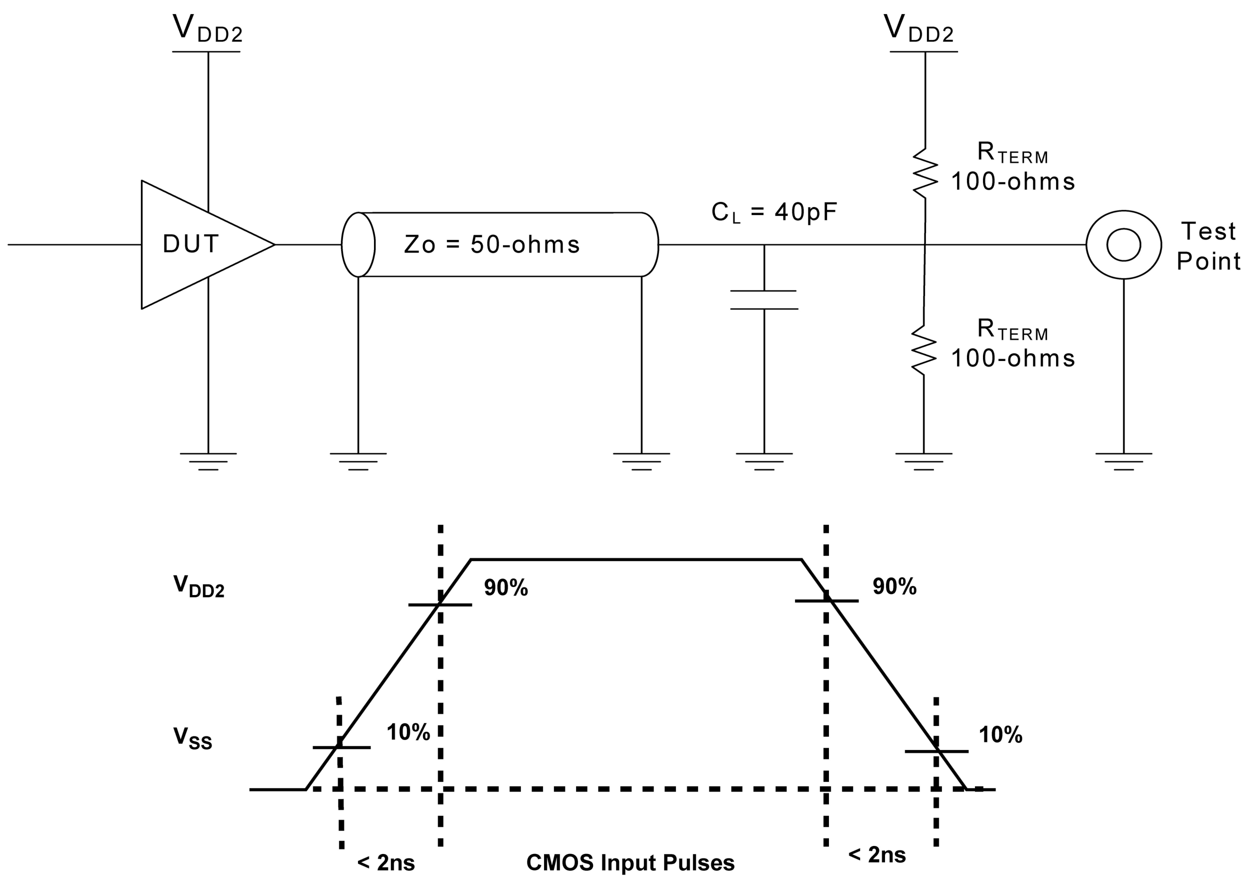


Figure 7. AC Test Loads and Input Waveforms

Note:

1) Measurement of data output occurs at the low to high or high to low transition mid-point (i.e., CMOS input = V_{DD2}/2

Packaging

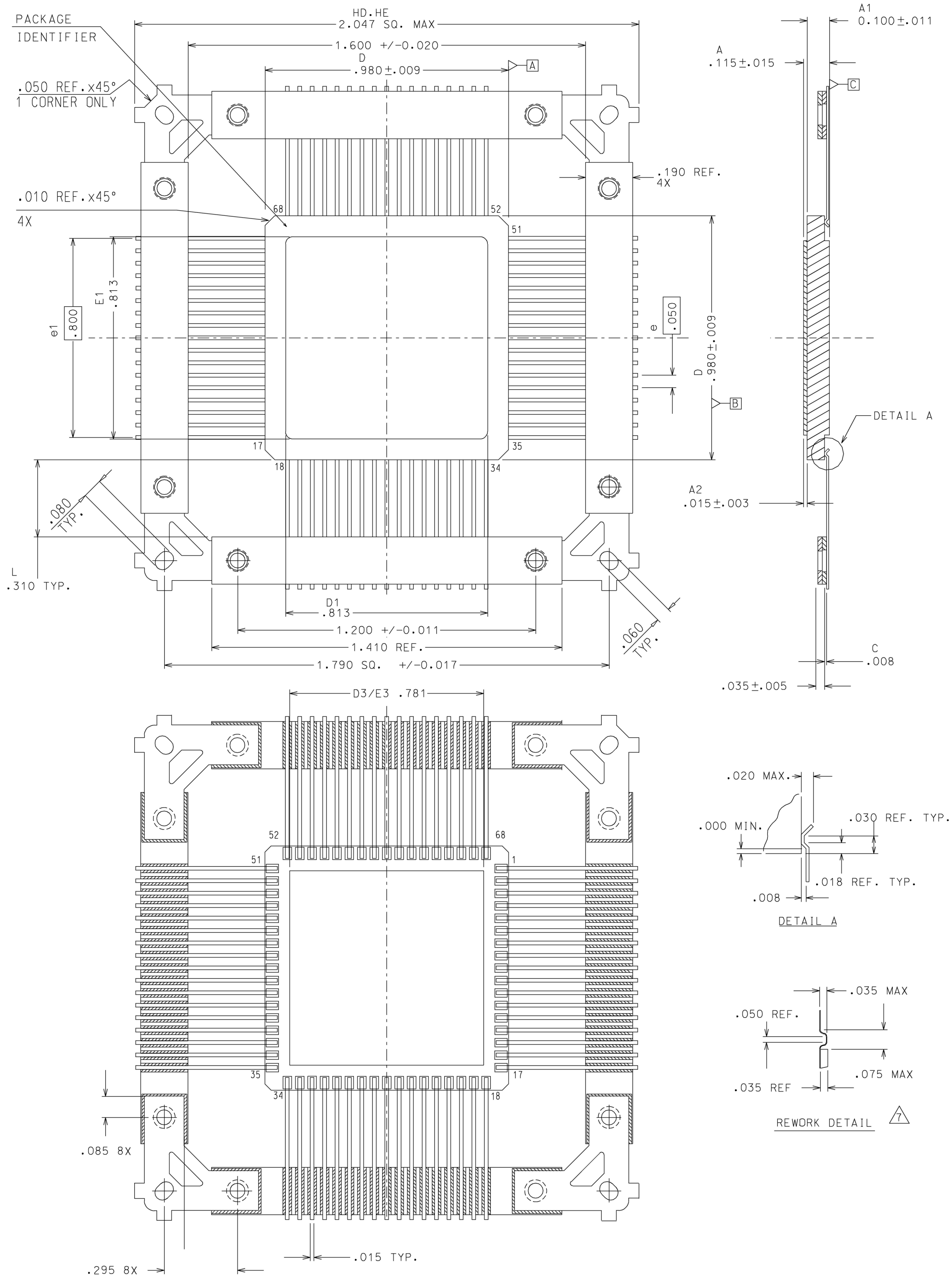


Figure 8. 68-Lead Ceramic Quad Flatpack

Notes:

1) All exposed metalized areas are gold plated over electroplated nickel per MIL-PRF-38535.
2) The lid is electrically connected to V_{SS}.
3) Lead finishes are in accordance to MIL-PRF-38535.

Monolithic 16M SRAM

UT8ER512K32

Ordering Information

512K x 32 SRAM

UT **** - ** * * *

Lead Finish: (Notes: 1, 2)
(A) = Hot Solder Dipped
(C) = Gold
(X) = Factory Option (gold or solder)

Screening Level: (Notes: 3, 4)
(P) = Prototype Flow
(C) = HiRel Temperature Range Flow (-55°C to 125°C)

Package Type:
(W) = 68-lead ceramic quad flatpack

Access Time:
(21) = 20ns read / 10ns write access times

Device Type:
(8ER512K32M) = 512K x 32 SRAM Master Device
(8ER512K32S) = 512K x 32 SRAM Slave Device

Notes:

1) Lead finish (A,C, or X) must be specified.
2) If an "X" is specified when ordering, then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3) Prototype flow per Frontgrade Colorado Springs Manufacturing Flows Document. Tested at 25°C only. Lead finish is GOLD ONLY. Radiation neither tested nor guaranteed.
4) HiRel Temperature Range flow per Frontgrade Colorado Springs Manufacturing Flows Document. Devices are tested at -55°C, room temp, and 125°C. Radiation neither tested nor guaranteed.

FRONTGRADE

DATASHEET

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Monolithic 16M SRAM

UT8ER512K32

512K x 32 SRAM: SMD

5962 * ***** ** * * *

Lead Finish: (Notes: 1, 2)
(A) = Hot Solder Dipped
(C) = Gold
(X) = Factory Option (gold or solder)

Case Outline:
(X) = 68-lead ceramic quad flatpack

QML/JAN Class:
(Q) = QML Class Q
(V) = QML Class V

Device Type:
(05) = 20ns read / 10ns write Master Device (-55°C to 125°C)
(06) = 20ns read / 10ns write Slave Device (-55°C to 125°C)

SMD Project Number: 06261

Radiation Hardness Assurance: (Note: 3)
(R) = 100 krad(Si)

Federal Stock Class Designator: No Options

Notes:

1) Lead finish (A,C, or X) must be specified.
2) If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3) TID tolerance guarantee is tested in accordance with MIL-STD-883 Test Method 1019 Condition A and section 3.11.2 resulting in an effective dose rate of 1 rad(Si)/sec.

Monolithic 16M SRAM

UT8ER512K32

Data Sheet Revision History

Revision Date	Description of Change	Page(s)	Author
3/23	added wording addressing read app note AN-MEM-002 and added timing parameters to AC Characteristics Read Cycle table, figure 3a, and 3b; revised ABS max section; New template	All	Nelson

FRONTGRADE

DATASHEET

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Monolithic 16M SRAM

UT8ER512K32

Datasheet Definitions

	DEFINITION
Advanced Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet **is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final**.
Preliminary Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

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