

4Tb TLC NAND Flash

UT81NDQ512G8T

Features

- Open NAND Flash Interface (ONFI) 4.0-compliant¹
- JEDEC NAND Flash Interoperability (JESD230C) compliant²
- Triple-level cell (TLC)
- B17A Industrial die source
- Organization
 - Page size x8: 18,592 bytes (16,384 + 2208 bytes)
 - Block size: 2304 pages, (36,864K + 4968K bytes)
 - Plane size: 4 planes x 504 blocks
 - Device size: 16128 blocks
- NV-DDR3 I/O performance³
 - Up to NV-DDR3 timing mode 9
 - Clock rate: 3ns (NV-DDR3)
 - Read/write throughput per pin: 667 MT/s
 - Tested over temperature in mode 9
- NV-DDR2 I/O performance⁴
 - Up to NV-DDR2 timing mode 8
 - Clock rate: 3.75ns (NV-DDR2)
 - Read/write throughput per pin: 533 MT/s
 - Tested over temperature in mode 6
- Asynchronous I/O performance⁴
 - Up to asynchronous timing mode 5
 - tRC/tWC: 20ns (MIN)
 - Read/write throughput per pin: 50 MT/s
 - Tested over temperature in mode 5
- TLC Array performance
 - SNAP READ operation time without VPP: 51μs(TYP)
 - Single-Plane READ PAGE operation time without/with VPP : 74/73μs (TYP)
 - Multi-Plane READ PAGE operation time without VPP: 88μs(TYP)
 - Effective Program page time without VPP : 1900μs(TYP)
 - Erase block time: 15ms (TYP)
- Operating Voltage Range
 - VCC: 2.7–3.6V
 - VCCQ: 1.14–1.26V, 1.7–1.95V
- Command set: ONFI NAND Flash Protocol
- Data is required to be randomized by the external host prior to being inputted to the NAND device, see External Data Randomization in the User Manual
- First block (block address 00h) is valid when shipped from factory. For minimum required ECC, see Error Management in the User Manual⁵
- RESET (FFh) required as first command after power-on
- Operation status byte provides software method for detecting
 - Operation completion
 - Pass/fail condition

4Tb TLC NAND Flash

UT81NDQ512G8T

- Write-protect status
- Data strobe (DQS) signals provide a hardware method for synchronizing data DQ in the NV-DDR2/NVDDR3 interface
- Copyback operations supported within the plane from which data is read
- On-die Termination (ODT)⁶
- Quality and reliability⁷
 - Testing methodology: JESD47
 - Data retention: JESD47 compliant
 - TLC Endurance: 3,000 PROGRAM/ERASE cycles
 - SLC Endurance: 40,000 PROGRAM/ERASE cycles
- Package
 - 132-ball BGA
 - Θ_{JC} : 2.68 °C/W
 - 2000V HBM ESD
 - 0.534 grams

Notes:

- 1) The ONFI 4.0 specification is available at www.onfi.org
- 2) The JEDEC specification is available at www.jedec.org/standards-documents
- 3) NV-DDR3 functionality is only available with 1.2V VCCQ
- 4) NV-DDR2 and Asynchronous functionality is only available with 1.8V VCCQ
- 5) ODT functionality is supported only in NVDDR2 and NV-DDR3 mode
- 6) READ RETRY and AUTO READ CALIBRATION operations are required to achieve specified endurance and for general array data integrity
- 7) For minimum required ECC, see External Data Randomization in the User Manual
- 8) Radiation testing is performed without VPP. VPP operations should not be used in a radiation environment. Devices using V_{pp} operations in a radiation environment will not be warranted

Operational Environment

- Temperature Range: -40°C to +85°C
- Total Dose: 30 to 50 krad(Si)
- SEL Immune: $\leq 60 \text{ MeV-cm}^2/\text{mg}$

Notes:

1. Radiation testing is performed without VPP. VPP operations should not be used in a radiation environment. Devices using V_{pp} operations in a radiation environment will not be warranted
2. Contact supplier for bit error performance and availability of material at a specific SLC and TLC TID levels

1 General Description

NAND Flash devices include an asynchronous data interface for I/O operations. These devices use a highly multiplexed 8-bit bus (DQx) to transfer commands, address, and data. There are five control signals used to implement the asynchronous data interface: CE#, CLE, ALE, WE#, and RE#. Additional signals control hardware write protection (WP#) and monitor device status (R/B#).

This NAND Flash device additionally includes a NV-DDR2, and/or a NV-DDR3 data interface for high-performance I/O operations. Data transfers include a bidirectional data strobe (DQS).

This hardware interface creates a low pin-count device with a standard pinout that remains the same from one density to another, enabling future upgrades to higher densities with no board redesign.

UT81NDQ512G8T

A target is the unit of memory accessed by a chip enable signal. A target contains one or more NAND Flash die. A NAND Flash die is the minimum unit that can independently execute commands and report status. A NAND Flash die, in the ONFI specification, is referred to as a logical unit (LUN). For further details, see Device and Array Organization.

2 Asynchronous, NV-DDR2, NV-DDR3 Signal Descriptions

Table 1: Asynchronous, NV-DDR2, and NV-DDR3 Signal Definitions

Asynchronous Signal ¹	NV-DDR2/NV-DDR3 Signal ¹	Type	Description ²
ALE	ALE	Input	Address latch enable: Loads an address from DQx into the address register.
CE#	CE#	Input	Chip enable: Enables or disables one or more die (LUNs) in a target.
CLE	CLE	Input	Command latch enable: Loads a command from DQx into the command register.
DQx	DQx	I/O	Data inputs/outputs: The bidirectional I/Os transfer address, data, and command information.
-	DQS, DQS_t	I/O	Data strobe: Provides a synchronous reference for data input and output.
-	DQS_c	I/O	Data strobe complement: Provides a complementary signal to the data strobe signal optionally used in the NV-DDR2 or NV-DDR3 interface for synchronous reference for data input and output
ENi	ENi	Input	Enumerate input: Input to a NAND device (if first NAND device on the daisy chain have as NC) from ENo of a previous NAND device to support CE# pin reduction functionality.
ENo	ENo	Output	Enumerate output: Output from a NAND device to the ENi of the next NAND device in the daisy chain to support CE# pin reduction functionality.
RE#	RE#, RE_t	Input	Read enable and write/read: RE# transfers serial data from the NAND Flash to the host system when the asynchronous interface is active.
-	RE_c	Input	Read enable complement: Provides a complementary signal to the read enable signal optionally used in the NV-DDR2 or NV-DDR3 interface for synchronous reference for data output.
WE#	WE#	Input	Write enable and clock: WE# transfers commands, addresses when the asynchronous, NV-DDR2, and NV-DDR3 interfaces are active, and serial data from the host system to the NAND Flash when the asynchronous interface is active.
WP#	WP#	Input	Write protect: Enables or disables array PROGRAM and ERASE operations.
R/B#	R/B#	Output	Ready/busy: An open-drain, active-low output that requires an external pull-up resistor. This signal indicates target array activity.

4Tb TLC NAND Flash

UT81NDQ512G8T

Asynchronous Signal ¹	NV-DDR2/NV-DDR3 Signal ¹	Type	Description ²
V _{CC}	V _{CC}	Supply	V_{CC} : Core power supply
V _{CCQ}	V _{CCQ}	Supply	V_{CCQ} : I/O power supply
V _{PP}	V _{PP}	Supply	V_{PP} : The V _{PP} signal is an optional external high voltage power supply to the device. This high voltage power supply may be used to enhance operations (e.g., improved power efficiency). If V _{PP} will not be utilized by a host system, that V _{PP} signal location is then defined as a DNU signal location.
V _{SS}	V _{SS}	Supply	V_{SS} : Core ground connection
V _{SSQ}	V _{SSQ}	Supply	V_{SSQ} : I/O ground connection
-	V _{REFQ}	Supply	V_{REFQ} : Reference voltage used with NV-DDR2 and NV-DDR3 interfaces
ZQ	ZQ	-	Reference pin for ZQ calibration : This is used on ZQ calibration. The ZQ signal shall be connected to V _{SS} through R _{ZQ} resistor
NC	NC	-	No connect : NCs are not internally connected. They can be driven or left unconnected
DNU	DNU	-	Do not use : DNUs must be left unconnected.
RFU	RFU	-	Reserved for future use : RFUs must be left unconnected

Notes:

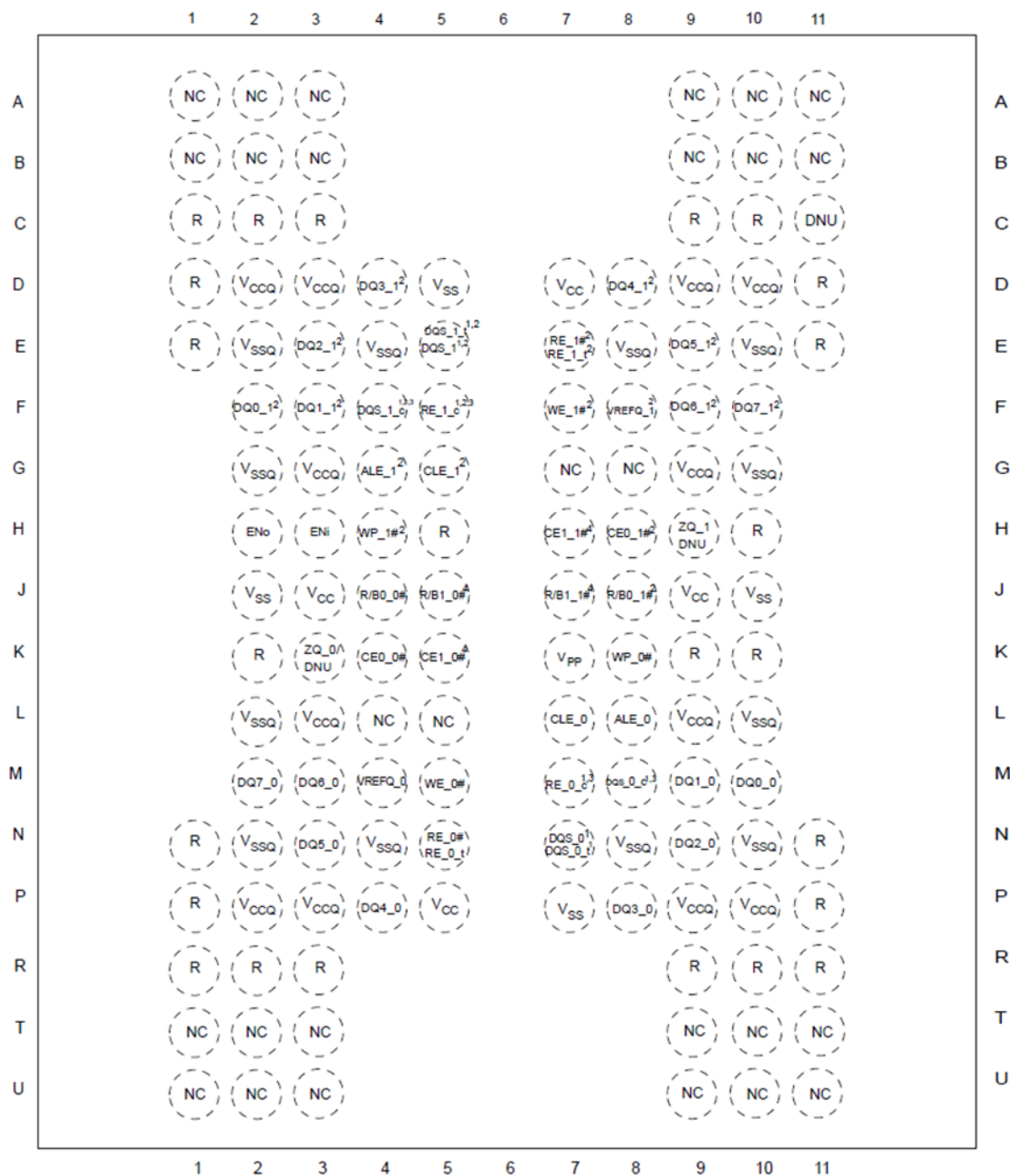
- 1) See Device and Array Organization and Signal Assignment sections for detailed signal connections.
- 2) See User Manual: Bus Operation - Asynchronous Interface, Bus Operations – NV-DDR2 Interface, and Bus Operation – NV-DDR3 Interface for detailed Asynchronous, NV-DDR2, and NV-DDR3 interface signal descriptions

4Tb TLC NAND Flash

UT81NDQ512G8T

3 Signal Assignments

Figure 1: 132-Ball BGA (Ball-Down, Top View)



Notes:

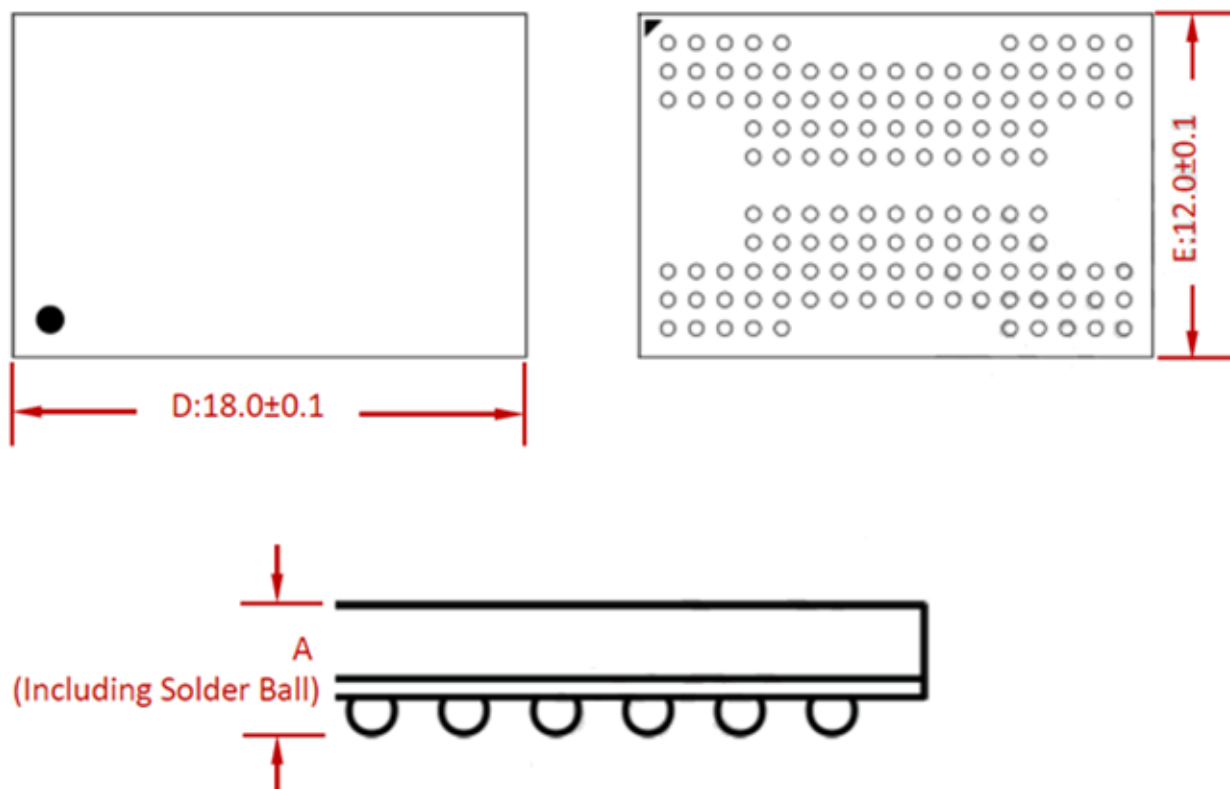
- 1) N/A: This signal is tri-stated when the asynchronous interface is active.
- 2) These signals are available on dual, quad, and octal die stacked die packages. They are NC for other configurations.
- 3) These signals are available when differential signaling is enabled.
- 4) These signals are available on quad die four CE# or octal die packages. They are NC for other configurations.

4Tb TLC NAND Flash

UT81NDQ512G8T

4 Package Dimensions

Figure 2: 132-Ball LBGA - 12mm x 18mm



Symbol (Dimension)	Min	Norm	Max
A (Total Thickness)	1.25	1.35	1.45
D (Lenth)	17.90	18.00	18.10
E (Width)	11.90	12.00	12.10
Ball Pitch	1.0 mm Typical		
Ball Diameter	0.45 mm Typical		

Notes:

- 1) All Dimensions in mm
- 2) Solder ball material: Sn-Pb
- 3) Package Mass: 0.534 grams

UT81NDQ512G8T

5 Architecture

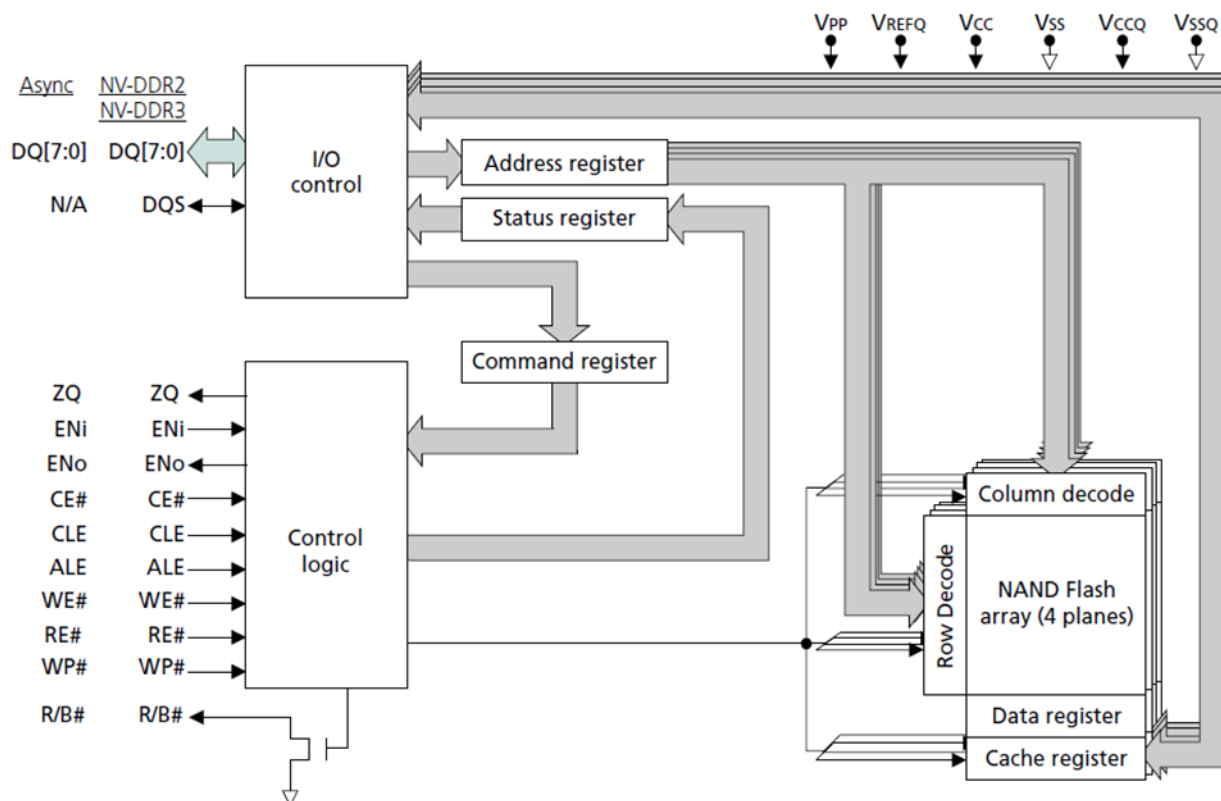
These devices use NAND Flash electrical and command interfaces. Data, commands, and addresses are multiplexed onto the same pins and received by I/O control circuits. The commands received at the I/O control circuits are latched by a command register and are transferred to control logic circuits for generating internal signals to control device operations. The addresses are latched by an address register and sent to a row decoder to select a row address, or to a column decoder to select a column address.

Data is transferred to or from the NAND Flash memory array, byte by byte, through a data register and a cache register.

The NAND Flash memory array is programmed and read using page-based operations and is erased using block-based operations. During normal page operations, the data and cache registers act as a single register. During cache operations, the data and cache registers operate independently to increase data throughput.

The status register reports the status of die (LUN) operations.

Figure 3: NAND Flash Die (LUN) Functional Block Diagram



Notes:

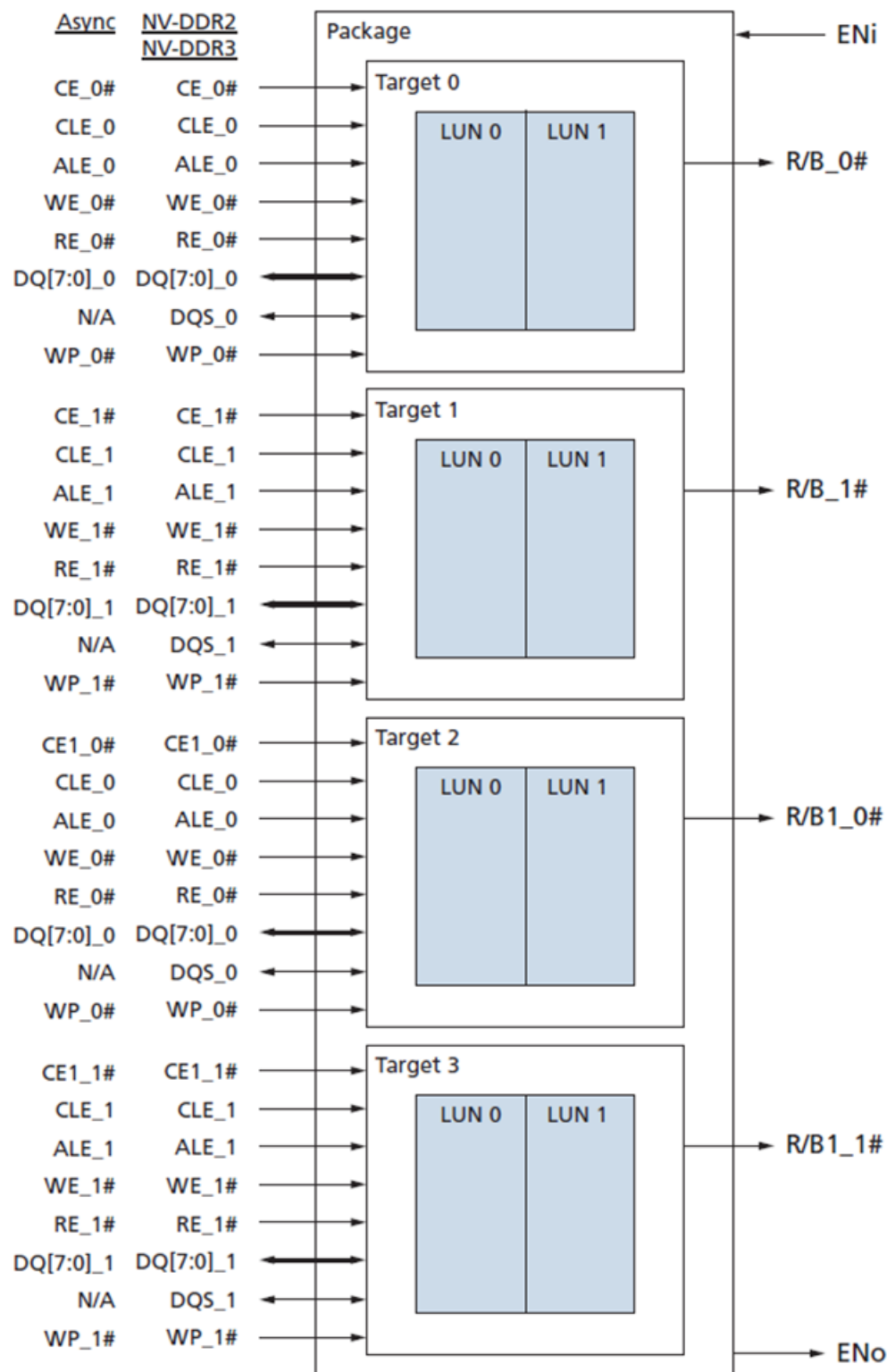
- 1) N/A: This signal is tri-stated when the asynchronous interface is active.

4Tb TLC NAND Flash

UT81NDQ512G8T

6 Device and Array Organization

Figure 4: Device Organization for Eight-Die Package with Four CE# (132-ball BGA)



UT81NDQ512G8T

Figure 5: Array Organization per Logical Unit (LUN) in TLC mode

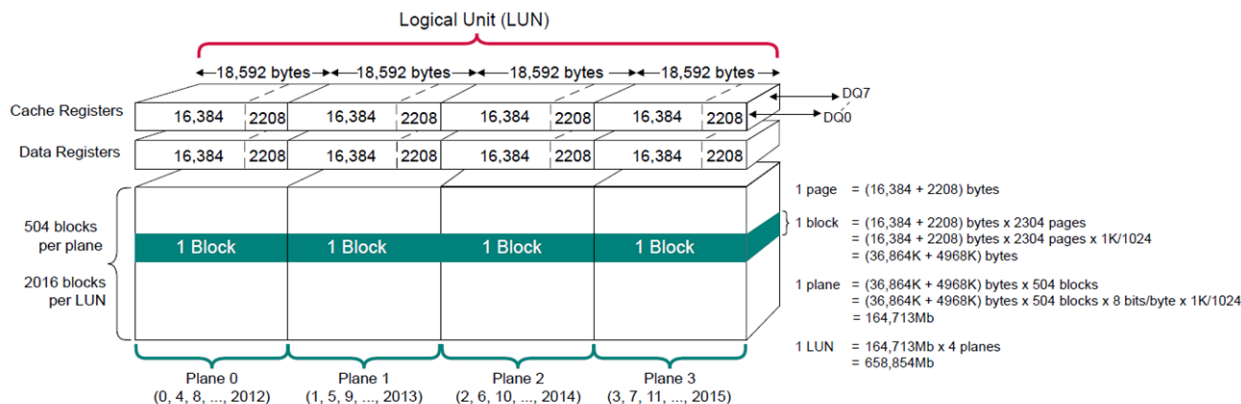


Table 2: Array Addressing for Logical Unit (LUN) in TLC mode

Cycle	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0 ²
Second	LOW	CA14 ³	CA13	CA12	CA11	CA10	CA9	CA8
Third	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA15	BA14	BA13 ⁵	BA12 ⁵	PA11 ⁴	PA10	PA9	PA8
Fifth	LA0 ^{6,7}	BA22	BA21	BA20	BA19	BA18	BA17	BA16

Notes:

- 1) CAx = column address, PAx = page address, BAx = block address, LAx = LUN address; the page address, block address, and LUN address are collectively called the row address. Consequently, the first and second cycles containing the column addresses are known as C1 and C2, and the third, fourth, fifth, and sixth cycles containing the row addresses cycles are known as R1, R2, R3, and R4 respectively.
- 2) When using the NV-DDR2/NV-DDR3 interface, CA0 is forced to 0 internally; one data cycle always returns one even byte and one odd byte.
- 3) CA [14:0] address column addresses 0 through 18,591 (16,384 + 2,208) (489Fh), therefore column addresses 18,592 (48A0h) through 32,767 (7FFFh) are invalid, out of bounds, do not exist in the device, and cannot be addressed.
- 4) PA [11:0] address page addresses 0 through 2303 (8FFh), therefore page addresses 2304 (900h) through 4095 (FFFh) are invalid, out of bounds, do not exist in the device, and cannot be addressed.
- 5) BA[13:12] are the plane-select bits:
Plane 0: BA[13:12] = 00b
Plane 1: BA[13:12] = 01b
Plane 2: BA[13:12] = 10b
Plane 3: BA[13:12] = 11b
- 6) LA0 is the LUN-select bit.
LUN 0: LA0 = 0
LUN 1: LA0 = 1
- 7) Block addresses 2016 through 2047 and 4063 through 4095 are invalid, out of bounds, do not exist in the device, and cannot be addressed.

UT81NDQ512G8T

Figure 6: Array Organization per Logical Unit (LUN) in SLC Mode

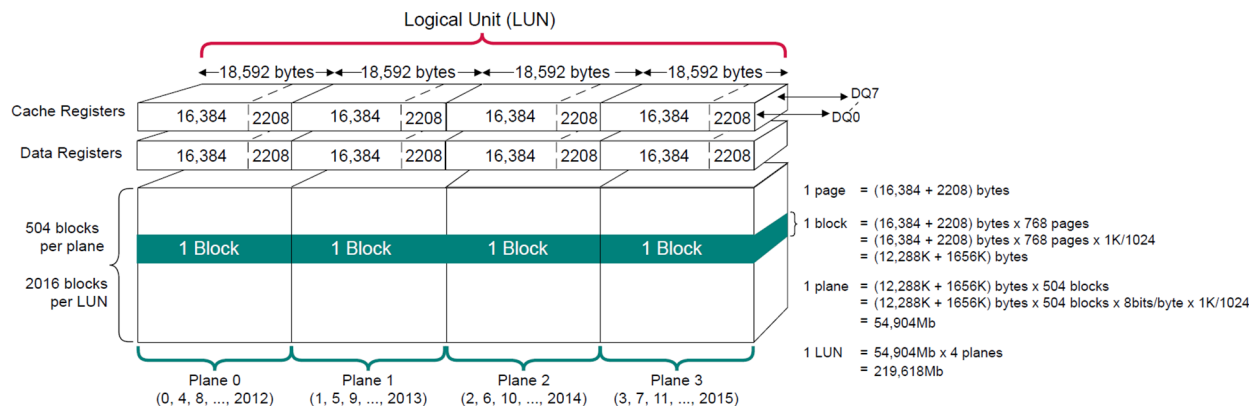


Table 3: Array Addressing for Logical Unit (LUN) in SLC mode

Cycle	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0 ²
Second	LOW	CA14 ³	CA13	CA12	CA11	CA10	CA9	CA8
Third	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA15	BA14	BA13 ⁵	BA12 ⁵	LOW	LOW	PA9 ⁴	PA8
Fifth	LA0 ^{6,7}	BA22	BA21	BA20	BA19	BA18	BA17	BA16

Notes:

- 1) CAx = column address, PAx = page address, BAx = block address, LAx = LUN address; the page address, block address, and LUN address are collectively called the row address. Consequently, the first and second cycles containing the column addresses are known as C1 and C2, and the third, fourth, fifth, and sixth cycles containing the row addresses cycles are known as R1, R2, R3, and R4 respectively.
- 2) When using the NV-DDR2/NV-DDR3 interface, CA0 is forced to 0 internally; one data cycle always returns one even byte and one odd byte.
- 3) CA [14:0] address column addresses 0 through 18,591 (16,384 + 2208) (489Fh), therefore column addresses 18,592 (48A0h) through 32,767 (7FFFh) are invalid, out of bounds, do not exist in the device, and cannot be addressed.
- 4) PA [9:0] address page addresses 0 through 767 (2FFh), therefore page addresses 768 (300h) through 1023 (3FFh) are invalid, out of bounds, do not exist in the device, and cannot be addressed.
- 5) BA[13:12] are the plane-select bits:
Plane 0: BA[13:12] = 00b
Plane 1: BA[13:12] = 01b
Plane 2: BA[13:12] = 10b
Plane 3: BA[13:12] = 11b
- 6) LA0 is the LUN-select bit.
LUN 0: LA0 = 0
LUN 1: LA0 = 1
- 7) Block addresses 2016 through 2047 and 4063 through 4095 are invalid, out of bounds, do not exist in the device, and cannot be addressed.

4Tb TLC NAND Flash

UT81NDQ512G8T

7 Command Definitions

Command	Command Cycle #1	Number of Valid Address Cycles ⁹ #1	Data Input Cycles	Command Cycle #2	Number of Valid Address Cycles ⁹ #2	Command Cycle #3	Valid While Selected LUN Is Busy ¹	Valid While Other LUNs are Busy ²	Notes
Reset Operations									
RESET	FFh	0	-	-	-	-	Yes	Yes	
HARD RESET	FDh	0	-	-	-	-		Yes	
SYNCHRONOUS RESET	FCh	0	-	-	-	-	Yes	Yes	
RESET LUN	FAh	3/4	-	-	-	-	Yes	Yes	
Identification Operations									
READ ID	90h	1	-	-	-	-			3
READ PARAMETER PAGE	ECh	1	-	-	-	-			
READ UNIQUE ID	EDh	1	-	-	-	-			
Configuration Operations									
VOLUME SELECT	E1h	1	-	-	-	-			
ODT CONFIGURE	E2h	1/2	4	-	-	-			
GET FEATURES	EEh	1	-	-	-	-			3
SET FEATURE	EFh	1	4	-	-	-			4
GET FEATURES BY LUN	D4h	2	-	-	-	-	-	Yes	3
SET FEATURES BY LUN	D5h	2	4	-	-	-	-	Yes	4
ZQ CALIBRATION LONG	F9h	1	-	-	-	-		Yes	
ZQ CALIBRATION SHORT	D9h	1	-	-	-	-		Yes	
SLC MODE ENABLE	DAh	0	-	-	-	-		Yes	
SLC MODE DISABLE	DFh	0	-	-	-	-		Yes	
Status Operations									
READ STATUS	70h	0	-	-	-	-	Yes		
FIXED ADDRESS READ STATUS ENHANCED	71h	1	-	-	-	-	Yes	Yes	
READ STATUS ENHANCED	78h	3/4	-	-	-	-	Yes	Yes	
Column Address Operations									
CHANGE READ COLUMN	05h	2	-	E0h	-	-		Yes	
CHANGE READ COLUMN ENHANCED (ONFI)	06h	5/6	-	E0h	-	-		Yes	
CHANGE READ COLUMN ENHANCED (JEDEC)	00h	5/6	-	05h	2	E0h		Yes	
CHANGE WRITE COLUMN	85h	2	Optional	-	-	-		Yes	

4Tb TLC NAND Flash

UT81NDQ512G8T

Command	Command Cycle #1	Number of Valid Address Cycles ⁹ #1	Data Input Cycles	Command Cycle #2	Number of Valid Address Cycles ⁹ #2	Command Cycle #3	Valid While Selected LUN Is Busy ¹	Valid While Other LUNs are Busy ²	Notes
CHANGE ROW ADDRESS	85h	5/6	Optional	11h (Optional)	-	-		Yes	5
Read Operations									
READ MODE	00h	0	-	-	-	-		Yes	
READ PAGE	00h	5/6	-	30h	-	-		Yes	6
SNAP READ	00h	5/6	-	20h	-	-		Yes	
READ PAGE MULTI-PLANE	00h	5/6	-	32h	-	-		Yes	
READ PAGE CACHE SEQUENTIAL	31h	0	-	-	-	-		Yes	7
READ PAGE CACHE RANDOM	00h	5/6	-	31h	-	-		Yes	6, 7
READ PAGE CACHE LAST	3Fh	0	-	-	-	-		Yes	7
READ PAGE WITH SOFT INFORMATION	33h	5/6	-	30h	-	-		Yes	
SOFT INFORMATION READOUT	36h	0	-		-	-		Yes	10
SINGLE BIT SOFT BIT READ PAGE	00h	5/6	-	34h	-	-		Yes	
SINGLE BIT SOFT BIT READ PAGE CACHE RANDOM	00h	5/6	-	38h	-	-		Yes	
Program Operations									
PROGRAM PAGE	80h	5/6	Yes	10h	-	-		Yes	
PROGRAM PAGE MULTI-PLANE	80h or 81h	5/6	Yes	11h	-	-		Yes	
PROGRAM PAGE CACHE	80h	5/6	Yes	15h	-	-		Yes	8
PROGRAM SUSPEND	84h	5/6	-	-	-	-	Yes	Yes	
PROGRAM RESUME	13h	5/6	-	-	-	-		Yes	
Erase Operations									
ERASE BLOCK	60h	3/4	-	D0h	-	-		Yes	
ERASE BLOCK MULTI-PLANE (ONFI)	60h	3/4	-	D1h	-	-		Yes	
ERASE BLOCK MULTI-PLANE (JEDEC)	60h	3/4	-	60h	3	D0h		Yes	

4Tb TLC NAND Flash

UT81NDQ512G8T

Command	Command Cycle #1	Number of Valid Address Cycles ⁹ #1	Data Input Cycles	Command Cycle #2	Number of Valid Address Cycles ⁹ #2	Command Cycle #3	Valid While Selected LUN Is Busy ¹	Valid While Other LUNs are Busy ²	Notes
ERASE SUSPEND	61h	3/4	-	-	-	-	Yes	Yes	
ERASE RESUME	D2h	-	-	-	-	-		Yes	
Copyback Operations									
COPYBACK READ	00h	5/6	-	35h	-	-		Yes	6
COPYBACK PROGRAM	85h	5/6	Optional	10h	-	-		Yes	
COPYBACK PROGRAM MULTI-PLANE	85h	5/6	Optional	11h	-	-		Yes	

Notes:

- 1) Busy means RDY = 0.
- 2) These commands can be used for interleaved die (multi-LUN) operations.
- 3) The READ ID (90h), GET FEATURES (EEh), and GET FEATURES by LUN (D4h) commands output identical data on rising and falling DQS edges.
- 4) The SET FEATURES (EFh) and SET FEATURES by LUN (D5h) commands requires data transition prior to the rising edge of DQS, with identical data for the rising and falling edges.
- 5) Command cycle #2 of 11h is conditional. See the User Manual, CHANGE ROW ADDRESS (85h) for more details.
- 6) This command can be preceded by READ PAGE MULTI-PLANE (00h-32h) command to accommodate a maximum simultaneous multi-plane array operation.
- 7) Issuing a READ PAGE CACHE-series (31h, 00h-31h, 00h-32h, 3Fh) command when the array is busy (RDY = 1, ARDY = 0) is supported if the previous command was a READ PAGE (00h-30h) or READ PAGE CACHE-series command; otherwise, it is prohibited.
- 8) Issuing a PROGRAM PAGE CACHE (80h-15h) command when the array is busy (RDY = 1, ARDY = 0) is supported if the previous command was a PROGRAM PAGE CACHE (80h-15h) command; otherwise, it is prohibited.
- 9) Refer to Device and Array Organization section for details of when the additional address cycles is required.
- 10) Refer to the User Manual, Soft Data Read Operations section for details of how this command is used.

UT81NDQ512G8T

8 Output Drive Impedance

Because NAND Flash is designed for use in systems that are typically point-to-point connections, an option to control the drive strength of the output buffers is provided. Drive strength should be selected based on the expected loading of the memory bus. The three supported settings for the output drivers for the Asynchronous, and NVDDR2 interfaces are: 25 ohms, 35 ohms, and 50 ohms. The two supported settings for the output drivers for the NV-DDR3 interface are: 35 ohms and 50 ohms.

The 35 ohms output drive strength setting is the power-on default value in the Asynchronous, and NV-DDR2 interfaces. The 35 ohms output drive strength setting is the power-on default value in the NV-DDR3 interface. The host can select a different drive strength setting using the SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command.

The output impedance range from minimum to maximum covers process, voltage, and temperature variations. Devices are not guaranteed to be at the nominal line.

Table 4: Output Drive Strength Conditions ($V_{CCQ}=1.7-1.95V$)

Range	Process	Voltage	Temperature
Minimum	Fast-Fast	1.95V	T_A (MIN)
Nominal	Typical-Typical	1.8V	+25°C
Maximum	Slow-Slow	1.7V	T_A (MAX)

Table 5: Output Drive Strength Impedance Values Without ZQ Calibration ($V_{CCQ} = 1.7-1.95V$)

Output Strength	Rpd/Rpu	V_{OUT} to V_{SSQ}	Minimum	Nominal	Maximum	Unit
25 ohms	Rpd	$V_{CCQ} \times 0.2$	11.4	25.0	44.0	ohms
		$V_{CCQ} \times 0.5$	15.0	25.0	44.0	ohms
		$V_{CCQ} \times 0.8$	15.0	25.0	61.0	ohms
	Rpu	$V_{CCQ} \times 0.2$	15.0	25.0	61.0	ohms
		$V_{CCQ} \times 0.5$	15.0	25.0	44.0	ohms
		$V_{CCQ} \times 0.8$	11.4	25.0	44.0	ohms
35 ohms	Rpd	$V_{CCQ} \times 0.2$	16.0	35.0	61.0	ohms
		$V_{CCQ} \times 0.5$	21.0	35.0	61.0	ohms
		$V_{CCQ} \times 0.8$	21.0	35.0	85.3	ohms
	Rpu	$V_{CCQ} \times 0.2$	21.0	35.0	85.3	ohms
		$V_{CCQ} \times 0.5$	21.0	35.0	61.0	ohms
		$V_{CCQ} \times 0.8$	16.0	35.0	61.0	ohms
50 ohms	Rpd	$V_{CCQ} \times 0.2$	24.0	50.0	87.0	ohms
		$V_{CCQ} \times 0.5$	30.0	50.0	87.0	ohms
		$V_{CCQ} \times 0.8$	30.0	50.0	122.0	ohms
	Rpu	$V_{CCQ} \times 0.2$	30.0	50.0	122.0	ohms
		$V_{CCQ} \times 0.5$	30.0	50.0	87.0	ohms
		$V_{CCQ} \times 0.8$	24.0	50.0	87.0	ohms

UT81NDQ512G8T

Table 6: Output Drive Strength Impedance Values With ZQ Calibration ($V_{CCQ} = 1.7-1.95V$)

Output Strength	Rpd/Rpu	V_{OUT} to V_{SSQ}	Minimum	Nominal	Maximum	Unit	Note
25 ohms	Rpd	$V_{CCQ} \times 0.2$	11.4	20.0	32.0	ohms	1
		$V_{CCQ} \times 0.5$	16.3	25.0	33.7	ohms	
		$V_{CCQ} \times 0.8$	20.0	31.0	49.0	ohms	
	Rpu	$V_{CCQ} \times 0.2$	20.0	31.0	49.0	ohms	
		$V_{CCQ} \times 0.5$	16.3	25.0	33.7	ohms	
		$V_{CCQ} \times 0.8$	11.4	20.0	32.0	ohms	
35 ohms	Rpd	$V_{CCQ} \times 0.2$	0.57	1	1.15	$R_{ZQ}/8.5$	
		$V_{CCQ} \times 0.5$	0.85	1	1.15	$R_{ZQ}/8.5$	
		$V_{CCQ} \times 0.8$	0.85	1	1.47	$R_{ZQ}/8.5$	
	Rpu	$V_{CCQ} \times 0.2$	0.85	1	1.47	$R_{ZQ}/8.5$	
		$V_{CCQ} \times 0.5$	0.85	1	1.15	$R_{ZQ}/8.5$	
		$V_{CCQ} \times 0.8$	0.57	1	1.15	$R_{ZQ}/8.5$	
50 ohms	Rpd	$V_{CCQ} \times 0.2$	0.57	1	1.15	$R_{ZQ}/6$	
		$V_{CCQ} \times 0.5$	0.85	1	1.15	$R_{ZQ}/6$	
		$V_{CCQ} \times 0.8$	0.85	1	1.47	$R_{ZQ}/6$	
	Rpu	$V_{CCQ} \times 0.2$	0.85	1	1.47	$R_{ZQ}/6$	
		$V_{CCQ} \times 0.5$	0.85	1	1.15	$R_{ZQ}/6$	
		$V_{CCQ} \times 0.8$	0.57	1	1.15	$R_{ZQ}/6$	

Notes:

- 1) The 25 ohms drive strength does not support ZQ CALIBRATION operations. If ZQ CALIBRATION operations are used when the 25 ohms drive strength is selected, the default NAND drive strength settings are still used.
- 2) Tolerance limits assume RZQ of 300 ohms $\pm 1\%$ and are applicable after proper ZQ calibration has been performed at a stable temperature and voltage.
- 3) Refer to Output Driver Sensitivity if either the temperature or the voltage changes after calibration.
- 4) The minimum values are derated by 6% when the device operates between $-40^{\circ}C$ and $0^{\circ}C$.

Table 7: Output Drive Strength Conditions ($V_{CCQ}=1.14-1.26V$)

Range	Process	Voltage	Temperature
Minimum	Fast-Fast	1.26V	T_A (MIN)
Nominal	Typical-Typical	1.2V	$+25^{\circ}C$
Maximum	Slow-Slow	1.14V	T_A (MAX)

UT81NDQ512G8T

Table 8: Output Drive Strength Impedance Values Without ZQ Calibration ($V_{CCQ} = 1.14\text{--}1.26\text{V}$)

Output Strength	Rpd/Rpu	V_{OUT} to V_{SSQ}	Minimum	Nominal	Maximum	Unit
35 ohms	Rpd	$V_{CCQ} \times 0.2$	16.0	35.0	61.0	ohms
		$V_{CCQ} \times 0.5$	21.0	35.0	61.0	ohms
		$V_{CCQ} \times 0.8$	21.0	35.0	85.3	ohms
	Rpu	$V_{CCQ} \times 0.2$	21.0	35.0	85.3	ohms
		$V_{CCQ} \times 0.5$	21.0	35.0	61.0	ohms
		$V_{CCQ} \times 0.8$	16.0	35.0	61.0	ohms
50 ohms	Rpd	$V_{CCQ} \times 0.2$	24.0	50.0	87.0	ohms
		$V_{CCQ} \times 0.5$	30.0	50.0	87.0	ohms
		$V_{CCQ} \times 0.8$	30.0	50.0	122.0	ohms
	Rpu	$V_{CCQ} \times 0.2$	30.0	50.0	122.0	ohms
		$V_{CCQ} \times 0.5$	30.0	50.0	87.0	ohms
		$V_{CCQ} \times 0.8$	24.0	50.0	87.0	ohms

Table 9: Output Drive Strength Impedance Values With ZQ Calibration ($V_{CCQ} = 1.14\text{--}1.26\text{V}$)

Output Strength	Rpd/Rpu	V_{OUT} to V_{SSQ}	Minimum	Nominal	Maximum	Unit
35 ohms	Rpd	$V_{CCQ} \times 0.2$	0.57	1	1.15	$R_{ZQ}/8.5$
		$V_{CCQ} \times 0.5$	0.85	1	1.15	$R_{ZQ}/8.5$
		$V_{CCQ} \times 0.8$	0.85	1	1.47	$R_{ZQ}/8.5$
	Rpu	$V_{CCQ} \times 0.2$	0.85	1	1.47	$R_{ZQ}/8.5$
		$V_{CCQ} \times 0.5$	0.85	1	1.15	$R_{ZQ}/8.5$
		$V_{CCQ} \times 0.8$	0.57	1	1.15	$R_{ZQ}/8.5$
50 ohms	Rpd	$V_{CCQ} \times 0.2$	0.57	1	1.15	$R_{ZQ}/6$
		$V_{CCQ} \times 0.5$	0.85	1	1.15	$R_{ZQ}/6$
		$V_{CCQ} \times 0.8$	0.85	1	1.47	$R_{ZQ}/6$
	Rpu	$V_{CCQ} \times 0.2$	0.85	1	1.47	$R_{ZQ}/6$
		$V_{CCQ} \times 0.5$	0.85	1	1.15	$R_{ZQ}/6$
		$V_{CCQ} \times 0.8$	0.57	1	1.15	$R_{ZQ}/6$

Notes:

- 1) Tolerance limits assume R_{ZQ} of 300 ohms $\pm 1\%$ and are applicable after proper ZQ calibration has been performed at a stable temperature and voltage.
- 2) Refer to Output Driver Sensitivity if either the temperature or the voltage changes after calibration.
- 3) The minimum values are derated by 6% when the device operates between -40°C and 0°C .

If either the temperature or the voltage changes after the ZQ CALIBRATION operation, then output drive strength impedance tolerance limits can be expected to widen according to Table 10 and Table 11.

UT81NDQ512G8T

Table 10: Output Drive Sensitivity With ZQ Calibration

Output Strength	Rpd/Rpu	V _{OUT} to V _{SSQ}	Minimum	Maximum	Unit
35 ohms	Rpd	V _{CCQ} × 0.2	0.57 – dR _{OND} T × ΔT – dR _{OND} V × ΔV	1.15 + dR _{OND} T × ΔT + dR _{OND} V × ΔV	R _{ZQ} /8.5
		V _{CCQ} × 0.5	0.85 – dR _{OND} T × ΔT – dR _{OND} V × ΔV	1.15 + dR _{OND} T × ΔT + dR _{OND} V × ΔV	R _{ZQ} /8.5
		V _{CCQ} × 0.8	0.85 – dR _{OND} T × ΔT – dR _{OND} V × ΔV	1.47 + dR _{OND} T × ΔT + dR _{OND} V × ΔV	R _{ZQ} /8.5
	Rpu	V _{CCQ} × 0.2	0.85 – dR _{OND} T × ΔT – dR _{OND} V × ΔV	1.47 + dR _{OND} T × ΔT + dR _{OND} V × ΔV	R _{ZQ} /8.5
		V _{CCQ} × 0.5	0.85 – dR _{OND} T × ΔT – dR _{OND} V × ΔV	1.15 + dR _{OND} T × ΔT + dR _{OND} V × ΔV	R _{ZQ} /8.5
		V _{CCQ} × 0.8	0.57 – dR _{OND} T × ΔT – dR _{OND} V × ΔV	1.15 + dR _{OND} T × ΔT + dR _{OND} V × ΔV	R _{ZQ} /8.5
50 ohms	Rpd	V _{CCQ} × 0.2	0.57 – dR _{OND} T × ΔT – dR _{OND} V × ΔV	1.15 + dR _{OND} T × ΔT + dR _{OND} V × ΔV	R _{ZQ} /6
		V _{CCQ} × 0.5	0.85 – dR _{OND} T × ΔT – dR _{OND} V × ΔV	1.15 + dR _{OND} T × ΔT + dR _{OND} V × ΔV	R _{ZQ} /6
		V _{CCQ} × 0.8	0.85 – dR _{OND} T × ΔT – dR _{OND} V × ΔV	1.47 + dR _{OND} T × ΔT + dR _{OND} V × ΔV	R _{ZQ} /6
	Rpu	V _{CCQ} × 0.2	0.85 – dR _{OND} T × ΔT – dR _{OND} V × ΔV	1.47 + dR _{OND} T × ΔT + dR _{OND} V × ΔV	R _{ZQ} /6
		V _{CCQ} × 0.5	0.85 – dR _{OND} T × ΔT – dR _{OND} V × ΔV	1.15 + dR _{OND} T × ΔT + dR _{OND} V × ΔV	R _{ZQ} /6
		V _{CCQ} × 0.8	0.57 – dR _{OND} T × ΔT – dR _{OND} V × ΔV	1.15 + dR _{OND} T × ΔT + dR _{OND} V × ΔV	R _{ZQ} /6

Table 11: Output Driver Voltage and Temperature Sensitivity With ZQ Calibration

Change	Minimum	Maximum	Unit
dR _{OND} T	0	0.5	%/°C
dR _{OND} V	0	0.2	%/mV

Table 12: Output Driver Voltage and Temperature Sensitivity With ZQ Calibration

Drive Strength	Minimum	Maximum	Unit	Notes
25 ohms	0	4.4	ohms	1, 2
35 ohms	0	6.2	ohms	1, 2
50 ohms	0	8.8	ohms	1, 2

Notes:

- 1) Mismatch is the absolute value between pull-up and pull-down impedances. Both are measured at the same temperature and voltage.
- 2) Test conditions: V_{CCQ} = V_{CCQ} (MIN), V_{OUT} = V_{CCQ} × 0.5, T_{OPER}.

UT81NDQ512G8T

Table 13: Pull-Up and Pull-Down Output Impedance Mismatch With ZQ Calibration for NV-DDR2

Drive Strength	Minimum	Maximum	Unit	Notes
25 ohms	0	3.75	ohms	1, 2, 3
35 ohms	0	5.25	ohms	2, 3
50 ohms	0	7.5	ohms	2, 3

Notes:

- 1) The 25 ohms drive strength does not support ZQ CALIBRATION operations. If ZQ CALIBRATION operations are used when the 25 ohms drive strength is selected, the default NAND drive strength settings are still used.
- 2) Mismatch is the absolute value between pull-up and pull-down impedances. Both are measured at the same temperature and voltage.
- 3) Test conditions: $V_{CCQ} = V_{CCQ} (MIN)$, $V_{OUT} = V_{CCQ} \times 0.5$, T_{OPER} .

Table 14: Pull-Up and Pull-Down Output Impedance Mismatch Without ZQ calibration for NV-DDR3

Drive Strength	Minimum	Maximum	Unit	Notes
35 ohms	0	6.2	ohms	1, 2
50 ohms	0	8.8	ohms	1, 2

Notes:

- 1) Mismatch is the absolute value between pull-up and pull-down impedances. Both are measured at the same temperature and voltage.
- 2) Test conditions: $V_{CCQ} = V_{CCQ} (MIN)$, $V_{OUT} = V_{CCQ} \times 0.5$, T_{OPER} .

Table 15: Pull-Up and Pull-Down Output Impedance Mismatch With ZQ calibration for NV-DDR3

Drive Strength	Minimum	Maximum	Unit	Notes
35 ohms	0	5.25	ohms	1, 2
50 ohms	0	7.5	ohms	1, 2

Notes:

- 1) Mismatch is the absolute value between pull-up and pull-down impedances. Both are measured at the same temperature and voltage.
- 2) Test conditions: $V_{CCQ} = V_{CCQ} (MIN)$, $V_{OUT} = V_{CCQ} \times 0.5$, T_{OPER} .

UT81NDQ512G8T

9 AC overshoot/undershoot specifications

The supported AC overshoot and undershoot area depends on the timing mode selected by the host. NAND devices may have different maximum amplitude requirements for overshoot and undershoot than the host controller. If the host controller has more stringent requirements, termination or other means of reducing overshoot or undershoot may be required beyond the NAND requirements.

Table 16: Asynchronous Overshoot/Undershoot Parameters

Parameter	Timing Mode						Unit
	0	1	2	3	4	5	
Maximum peak amplitude provided for overshoot area	1	1	1	1	1	1	V
Maximum peak amplitude provided for undershoot area	1	1	1	1	1	1	V
Maximum overshoot area above V_{CCQ}	3	3	3	3	3	3	V-ns
Maximum undershoot area below V_{SSQ}	3	3	3	3	3	3	V-ns

Table 17: NV-DDR2 Overshoot/Undershoot Parameters

Parameter	Signals	Timing Mode								Unit
		0	1	2	3	4	5	6	7	
Maximum peak amplitude provided for overshoot area	-	1	1	1	1	1	1	1	1	V
Maximum peak amplitude provided for undershoot area	-	1	1	1	1	1	1	1	1	V
Maximum overshoot area above V_{CCQ}	DQ[7:0], DQS, RE#	3	3	2.25	1.8	1.5	1.1	0.9	0.75	V-ns
	ALE, CLE, WE#	3	3	3	3	3	3	3	3	
Maximum undershoot area below V_{SSQ}	DQ[7:0], DQS, RE#	3	3	2.25	1.8	1.5	1.1	0.9	0.75	V-ns
	ALE, CLE, WE#	3	3	3	3	3	3	3	3	

Table 18: NV-DDR3 Overshoot/Undershoot Parameters

Parameter	Signals	Timing Mode											Unit
		0	1	2	3	4	5	6	7	8	9	10	
Maximum peak amplitude provided for overshoot area	-	0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	V
Maximum peak amplitude provided for undershoot area	-	0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	0.8	V
Maximum overshoot area above V_{CCQ}	DQ[7:0], DQS, RE#	3	3	2.25	1.8	1.5	1.1	0.9	0.75	0.56	0.45	0.38	V-ns
	ALE, CLE, WE#	3	3	3	3	3	3	3	3	3	3	3	
Maximum undershoot area below V_{SSQ}	DQ[7:0], DQS, RE#	3	3	2.25	1.8	1.5	1.1	0.9	0.75	0.56	0.45	0.38	V-ns
	ALE, CLE, WE#	3	3	3	3	3	3	3	3	3	3	3	

UT81NDQ512G8T

Figure 7: Overshoot

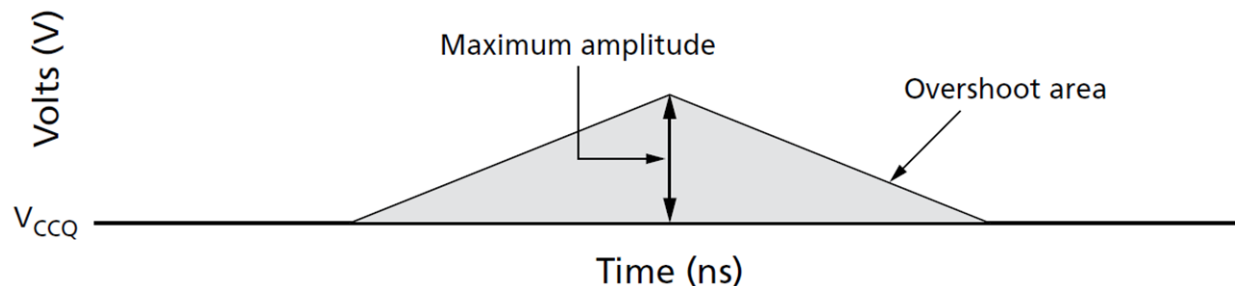
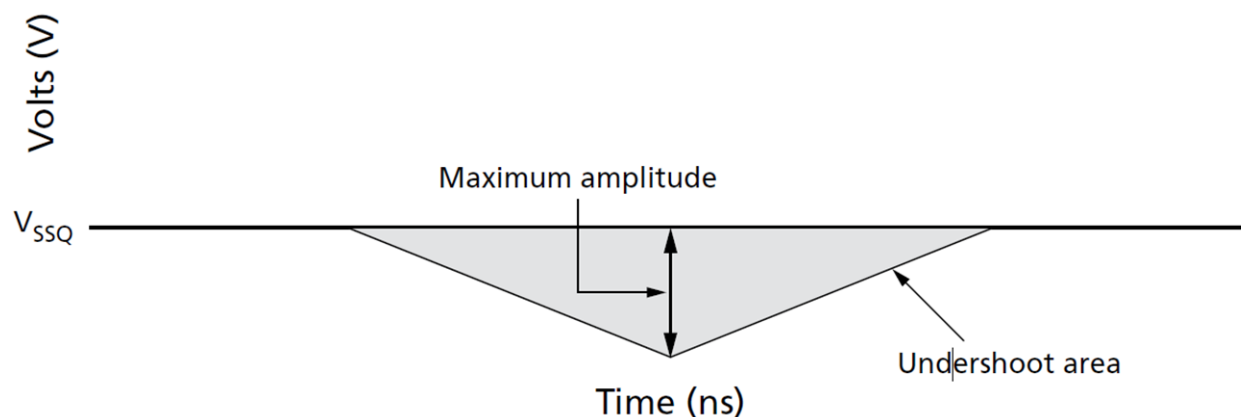


Figure 8: Undershoot



10 Input slew rate

Though all AC timing parameters are tested with a nominal input slew rate of 1 V/ns, it is possible to run the device at a slower slew rate. The input slew rates shown below are sampled, and not 100% tested. When using slew rates slower than the minimum values, timing must be derated by the host.

Table 19: Test Conditions for Input Slew Rate

Parameter	Value
Rising edge for setups	The last crossing of $V_{REFQ(DC)}$ and the first crossing of $V_{IH(AC)}$ min for NV-DDR2 and NV-DDR3
Falling edge for setups	The last crossing of $V_{REFQ(DC)}$ and the first crossing of $V_{IL(AC)}$ max for NV-DDR2 and NV-DDR3
Rising edge for holds	The first crossing of $V_{IL(AC)}$ max and the first crossing of $V_{REFQ(DC)}$ for NV-DDR2 and NV-DDR3
Falling edge for holds	The first crossing of $V_{IH(AC)}$ min and the first crossing of $V_{REFQ(DC)}$ for NV-DDR2 and NV-DDR3
Temperature range	T_A

The minimum and maximum input slew rate requirements that the device shall comply with below for NV-DDR2 and NV-DDR3 operations. If the input slew rate falls below the minimum value, then derating shall be applied.

UT81NDQ512G8T

Table 20: NV-DDR2/NV-DDR3 Maximum and Minimum Input Slew Rate

Description	Single Ended	Differential	Unit
Input slew rate (min)	1.0	2.0	V/ns
Input slew rate (max)	4.5	9.0	V/ns

For DQ signals when used for input, the total data setup time (t_{DS}) and data hold time (t_{DH}) required is calculated by adding a derating value to the t_{DS} and t_{DH} values indicated for the timing mode. To calculate the total data setup time, t_{DS} is incremented by the appropriate Δ_{set} derating value. To calculate the total data hold time, t_{DH} is incremented by the appropriate Δ_{hold} derating value. Table 21 and Table 23 provides the derating values when single-ended DQS is used. Table 22 and Table 24 provides the derating values when differential DQS (DQS_t/DQS_c) is used.

The setup nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REFQ(DC)}$ and the first crossing of $V_{IH(AC)}$ min. The setup nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REFQ(DC)}$ and the first crossing of $V_{IL(AC)}$ max. If the actual signal is always earlier than the nominal slew rate line between the shaded ' $V_{REFQ(DC)}$ to AC region', then the derating value uses the nominal slew rate shown in Figure 9. If the actual signal is later than the nominal slew rate line anywhere between shaded ' $V_{REFQ(DC)}$ to AC region', then the derating value uses the slew rate of a tangent line to the actual signal from the AC level to the DC level shown in Figure 10.

The hold nominal slew rate for a rising signal is defined as the slew rate between the first crossing of $V_{IL(DC)}$ max and the first crossing of $V_{REFQ(DC)}$. The hold nominal slew rate for a falling signal is defined as the slew rate between the first crossing of $V_{IH(DC)}$ min and the first crossing of $V_{REFQ(DC)}$. If the actual signal is always later than the nominal slew rate line between shaded 'DC to $V_{REFQ(DC)}$ region', then the derating value uses the nominal slew rate shown in Figure 11. If the actual signal is earlier than the nominal slew rate line anywhere between the shaded 'DC to $V_{REFQ(DC)}$ region', then the derating value uses the slew rate of a tangent line to the actual signal from the DC level to the $V_{REFQ(DC)}$ level shown in Figure 12.

If the tangent line is used for derating, the setup and hold values shall be derated from where the tangent line crosses $V_{REFQ(DC)}$, not the actual signal (refer to Figure 10 and Figure 12).

For slew rates not explicitly listed in Table 21 and Table 22, the derating values should be obtained by linear interpolation. These values are typically not subject to production test; the values are verified by design and characterization.

Table 21: Input Slew Rate derating for NV-DDR2 single-ended ($V_{CCQ} = 1.7-1.95V$)

DQ slew rate V/ns	Δ^tDS, Δ^tDH Derating (ps) $V_{IH(AC)} / V_{IL(AC)} = V_{REF} + / - 250mV, V_{IH(DC)} / V_{IL(DC)} = V_{REF} + / - 125mV$																				Unit
	DQS Slew Rate																				
	2 V/ns		1.5V/ns		1 V/ns		0.9V/ns		0.8V/ns		0.7V/ns		0.6V/ns		0.5V/ns		0.4V/ns		0.3V/ns		
	t^tDH	t^tDH	t^tDH	t^tDH	t^tDH	t^tDH	t^tDH	t^tDH	t^tDH	t^tDH	t^tDH	t^tDH	t^tDH	t^tDH	t^tDH	t^tDH	t^tDH	t^tDH	t^tDH	t^tDH	
2	0	0	0	0	0	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	ps
1.5	0	0	0	0	0	0	14	0	-	-	-	-	-	-	-	-	-	-	-	-	ps
1	0	0	0	0	0	0	14	0	31	0	-	-	-	-	-	-	-	-	-	-	ps
0.9	-	-	14	0	14	0	28	0	45	0	67	0	-	-	-	-	-	-	-	-	ps
0.8	-	-	-	-	31	0	45	0	63	0	85	0	115	0	-	-	-	-	-	-	ps
0.7	-	-	-	-	-	-	67	0	85	0	107	0	137	0	179	0	-	-	-	-	ps
0.6	-	-	-	-	-	-	-	-	115	0	137	0	167	0	208	0	271	0	-	-	ps
0.5	-	-	-	-	-	-	-	-	-	-	179	0	208	0	250	0	313	0	418	0	ps
0.4	-	-	-	-	-	-	-	-	-	-	-	-	271	0	313	0	375	0	480	0	ps
0.3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	418	0	480	0	594	0	ps

Note: Shaded area indicates the slew rate combinations not supported.

4Tb TLC NAND Flash

UT81NDQ512G8T

Table 22: Input Slew Rate derating for NV-DDR2 differential ($V_{CCQ} = 1.7-1.95V$)

DQ slew rate V/ns	Δ^tDS, Δ^tDH Derating (ps) $V_{IH(AC)} / V_{IL(AC)} = V_{REF} + / - 250mV, V_{IH(DC)} / V_{IL(DC)} = V_{REF} + / - 125mV$																Unit
	DQS_t/DQS_c Slew Rate																
	2 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1 V/ns		0.8 V/ns		0.6 V/ns		
	t'DH	t'DH	t'DH	t'DH	t'DH	t'DH	t'DH	t'DH	t'DH	t'DH	t'DH	t'DH	t'DH	t'DH	t'DH	t'DH	
2	0	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	ps
1.5	0	0	7	7	-	-	-	-	-	-	-	-	-	-	-	-	ps
1	0	0	7	7	16	16	-	-	-	-	-	-	-	-	-	-	ps
0.9	14	14	21	21	30	30	41	41	-	-	-	-	-	-	-	-	ps
0.8	31	31	38	38	47	47	58	58	73	73	-	-	-	-	-	-	ps
0.7	-	-	61	61	69	69	80	80	90	90	116	116	-	-	-	-	ps
0.6	-	-	-	-	99	99	100	100	100	100	100	100	100	100	-	-	ps
0.5	-	-	-	-	-	-	150	150	150	150	150	150	150	150	150	150	ps
0.4	-	-	-	-	-	-	-	-	200	200	200	200	200	200	200	200	ps
0.3	-	-	-	-	-	-	-	-	-	-	225	225	225	225	225	225	ps

Note: Shaded area indicates the slew rate combinations not supported.Table 23: Input Slew Rate derating for NV-DDR3 single-ended ($V_{CCQ} = 1.14-1.26V$)

DQ slew rate V/ns	Δ^tDS, Δ^tDH Derating (ps) $V_{IH(AC)} / V_{IL(AC)} = V_{REF} + / - 150mV, V_{IH(DC)} / V_{IL(DC)} = V_{REF} + / - 100mV$																				Unit
	DQS Slew Rate																				
	2 V/ns		1.5V/ns		1 V/ns		0.9V/ns		0.8V/ns		0.7V/ns		0.6V/ns		0.5V/ns		0.4V/ns		0.3V/ns		
	t^tDH	t^tDH	t^tDH	t^tDH	t^tDH	t^tDH	t^tDH	t^tDH	t^tDH	t^tDH	t^tDH	t^tDH	t^tDH	t^tDH	t^tDH	t^tDH	t^tDH	t^tDH	t^tDH	t^tDH	
2	0	0	0	0	0	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	ps
1.5	0	0	0	0	0	0	11	0	-	-	-	-	-	-	-	-	-	-	-	-	ps
1	0	0	0	0	0	0	11	0	25	0	-	-	-	-	-	-	-	-	-	-	ps
0.9	-	-	0	0	11	0	22	0	36	0	54	0	-	-	-	-	-	-	-	-	ps
0.8	-	-	-	-	25	0	39	0	50	0	68	0	92	0	-	-	-	-	-	-	ps
0.7	-	-	-	-	-	-	54	0	68	0	86	0	110	0	143	0	-	-	-	-	ps
0.6	-	-	-	-	-	-	-	-	92	0	110	0	133	0	167	0	217	0	-	-	ps
0.5	-	-	-	-	-	-	-	-	-	-	143	0	167	0	200	0	250	0	333	0	ps
0.4	-	-	-	-	-	-	-	-	-	-	-	-	217	0	250	0	300	0	383	0	ps
0.3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	333	0	383	0	467	0	ps

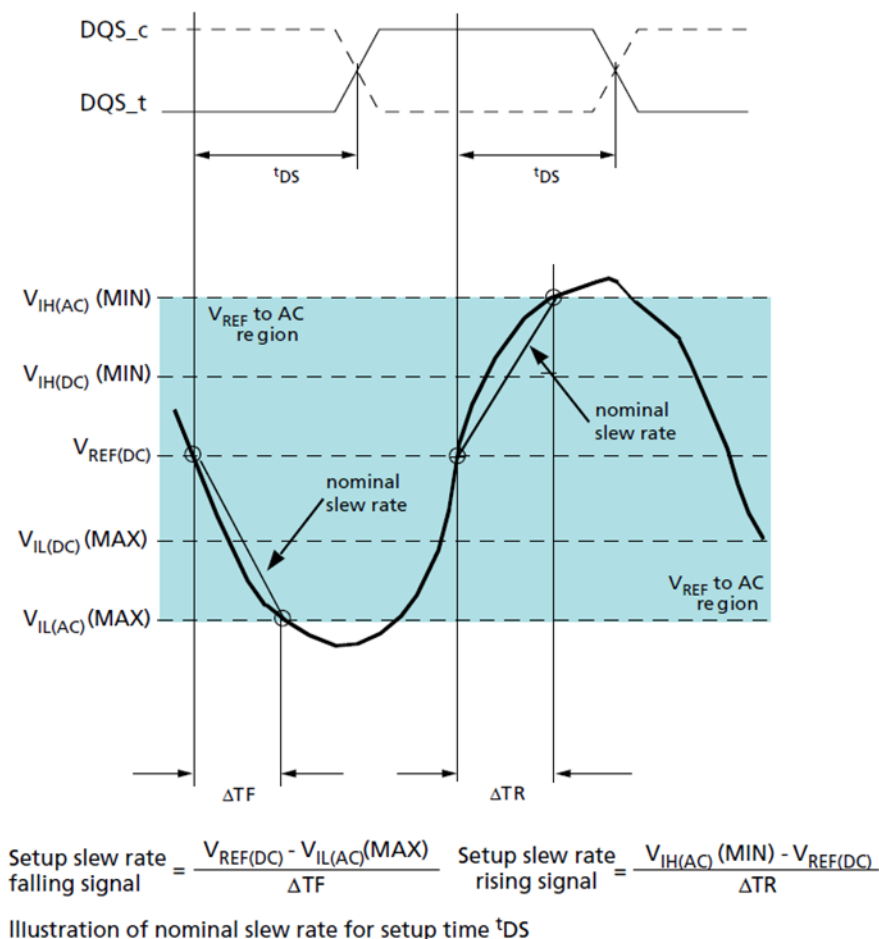
Note: Shaded area indicates the slew rate combinations not supported.

UT81NDQ512G8T

Table 24: Input Slew Rate derating for NV-DDR3 differential ($V_{CCQ} = 1.14-1.26V$)

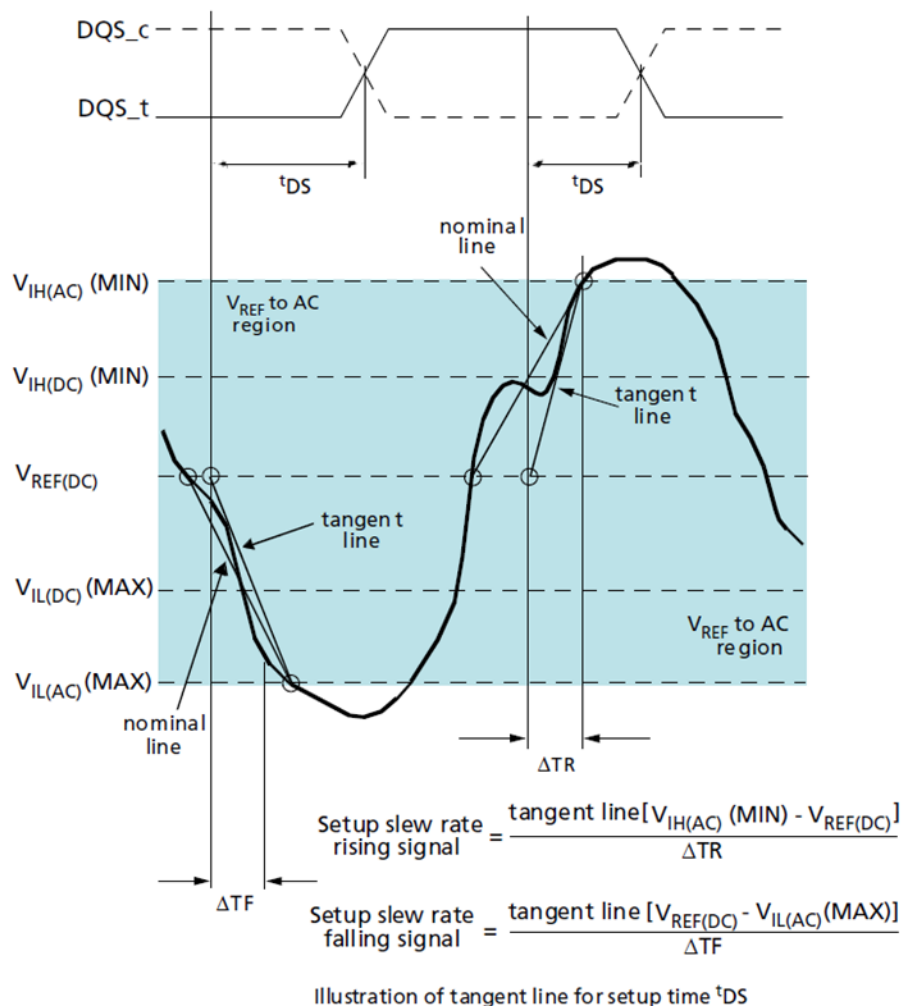
DQ slew rate V/ns	Δ^tDS, Δ^tDH Derating (ps) $V_{IH(AC)} / V_{IL(AC)} = V_{REF} + / - 250mV, V_{IH(DC)} / V_{IL(DC)} = V_{REF} + / - 125mV$																Unit
	DQS_t/DQS_c Slew Rate																
	2 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1 V/ns		0.8 V/ns		0.6 V/ns		
	t^tDH	t^tDH	t^tDH	t^tDH	t^tDH	t^tDH	t^tDH	t^tDH	t^tDH	t^tDH	t^tDH	t^tDH	t^tDH	t^tDH	t^tDH	t^tDH	
2	0	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	ps
1.5	0	0	6	6	-	-	-	-	-	-	-	-	-	-	-	-	ps
1	0	0	6	6	13	13	-	-	-	-	-	-	-	-	-	-	ps
0.9	11	11	17	17	24	24	33	33	-	-	-	-	-	-	-	-	ps
0.8	25	25	31	31	38	38	46	46	58	58	-	-	-	-	-	-	ps
0.7	-	-	48	48	55	55	64	64	75	75	75	75	-	-	-	-	ps
0.6	-	-	-	-	79	79	88	88	100	100	100	100	100	100	-	-	ps
0.5	-	-	-	-	-	-	121	121	125	125	125	125	125	125	125	125	ps
0.4	-	-	-	-	-	-	-	-	150	150	150	150	150	150	150	150	ps
0.3	-	-	-	-	-	-	-	-	-	-	175	175	175	175	175	175	ps

Note: Shaded area indicates the slew rate combinations not supported.

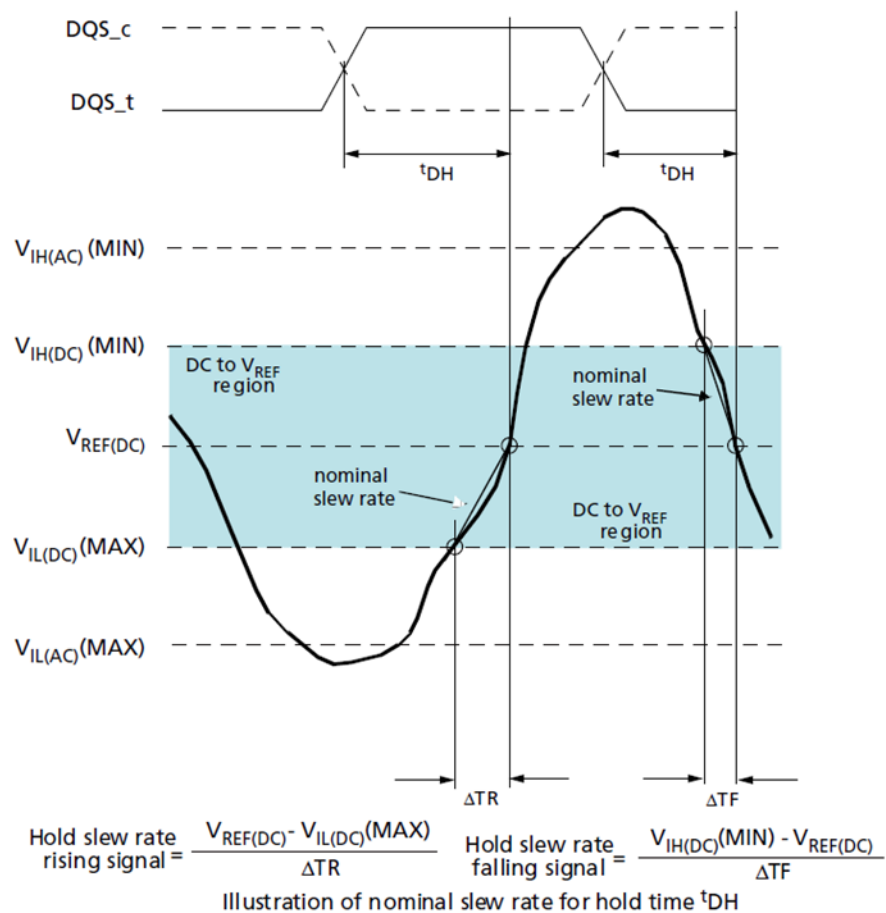
Figure 9: Nominal Slew Rate for Data Setup Time (t_{DS}), NV-DDR2/NV-DDR3 only

4Tb TLC NAND Flash

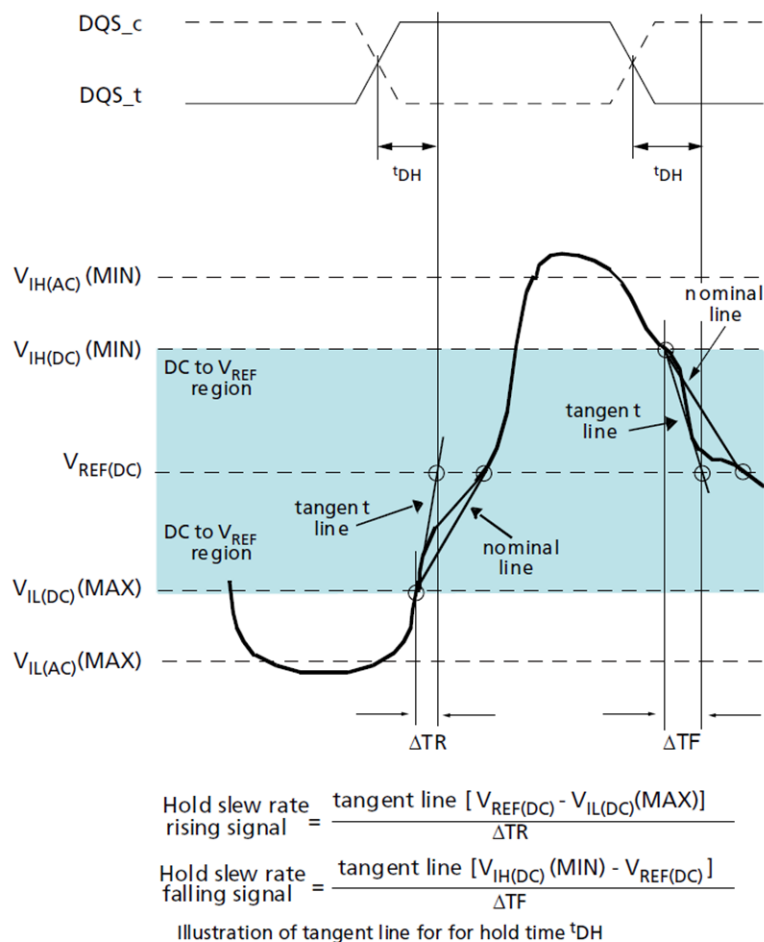
UT81NDQ512G8T

Figure 10: Tangent Line for Data Setup Time (t_{DS}), NV-DDR2/NV-DDR3 only

UT81NDQ512G8T

Figure 11: Nominal Slew Rate for Data Hold Time (t_{DH}), NV-DDR2/NV-DDR3 only

UT81NDQ512G8T

Figure 12: Tangent Line for Data Hold Time (t_{DH}), NV-DDR2/NV-DDR3 only

11 Output slew rate

The output slew rate is tested using the following setup with only one die per DQ channel.

Parameter	Asynchronous Interface ¹	NV-DDR2/NV-DDR3 Single-Ended ^{1, 2}	NV-DDR2/NV-DDR3 Differential ^{1, 2}
VOL(DC)	$0.4 \times V_{CCQ}$	—	—
VOH(DC)	$0.6 \times V_{CCQ}$	—	—
VOL(AC) ³	$0.3 \times V_{CCQ}$	$V_{TT} - (V_{CCQ} \times 0.10)$	—
VOH(AC) ³	$0.7 \times V_{CCQ}$	$V_{TT} + (V_{CCQ} \times 0.10)$	—
VOLdiff(AC)	—	—	$-0.2 \times V_{CCQ}$
VOHdiff(AC)	—	—	$0.2 \times V_{CCQ}$
Rising edge (t_{RISE})	VOL(DC) to VOH(AC)	VOL(AC) to VOH(AC)	—
Falling edge (t_{FALL})	VOH(DC) to VOL(AC)	VOH(AC) to VOL(AC)	—
Differential rising edge ($t_{RISEdiff}$)	—	—	VOLdiff(AC) to VOHdiff(AC)
Differential falling edge ($t_{FALLdiff}$)	—	—	VOHdiff(AC) to VOLdiff(AC)

4Tb TLC NAND Flash

UT81NDQ512G8T

Parameter	Asynchronous Interface ¹	NV-DDR2/NV-DDR3 Single-Ended ^{1, 2}	NV-DDR2/NV-DDR3 Differential ^{1, 2}
Output slew rate rising edge	$[V_{OH(AC)} - V_{OL(DC)}]/t_{RISE}$	$[V_{OH(AC)} - V_{OL(AC)}]/t_{RISE}$	$[V_{OHdiff(AC)} - V_{OLdiff(AC)}]/t_{RISEdiff}$
Output slew rate falling edge	$[V_{OH(DC)} - V_{OL(AC)}]/t_{FALL}$	$[V_{OH(AC)} - V_{OL(AC)}]/t_{FALL}$	$[V_{OHdiff(AC)} - V_{OLdiff(AC)}]/t_{FALLdiff}$
Output reference load ³	5pf to Vss		
Temperature range	T _A		

Notes:

- 1) 1.8V V_{CCQ} is required for Asynchronous and NV-DDR2 operations.
- 2) 1.2V V_{CCQ} is required for NV-DDR3 operations.
- 3) V_{TT} is 0.5 x V_{CCQ}.

Table 25: Output Slew Rate for Single-Ended Asynchronous, or NV-DDR2 (V_{CCQ} = 1.7–1.95V) Without ZQ Calibration

Output Drive Strength	Min	Max	Unit
25 ohms	0.85	5	V/ns
35 ohms	0.75	4	V/ns
50 ohms	0.6	4	V/ns

Table 26: Output Slew Rate for Differential NV-DDR2 (V_{CCQ} = 1.7–1.95V) Without ZQ Calibration

Output Drive Strength	Min	Max	Unit
25 ohms	1.7	10.0	V/ns
35 ohms	1.5	8.0	V/ns
50 ohms	1.2	8.0	V/ns

Table 27: Output Slew Rate for Differential NV-DDR2 (V_{CCQ} = 1.7–1.95V) With ZQ Calibration

Output Drive Strength	Min	Max	Unit
25 ohms	2.4	10.0	V/ns
35 ohms	2.16	8.0	V/ns
50 ohms	1.8	7.0	V/ns

Table 28: Output Slew Rate Matching Ratio for NV-DDR2/NV-DDR3 Without ZQ Calibration

Drive Strength	Min	Max
Output slew rate matching ratio (pull-up to pull-down)	0.7	1.4

Notes:

- 1) The output slew rate mismatch is determined by the ratio of fast slew rate and slow slew rate. If the rising edge is faster than the falling edge, then divide the rising slew rate by the falling slew rate. If the falling edge is faster than the rising edge, then divide the falling slew rate by the rising slew rate.
- 2) The output slew rate mismatch is verified by design and characterization; it may not be subject to production testing.

UT81NDQ512G8T

Table 29: Output Slew Rate for Single-Ended NV-DDR3 ($V_{CCQ} = 1.14\text{--}1.26\text{V}$) With ZQ Calibration

Output Drive Strength	Min	Max	Unit
35 ohms	0.72	4	V/ns
50 ohms	0.6	3.5	V/ns

Table 30: Output Slew Rate for Differential NV-DDR3 ($V_{CCQ} = 1.14\text{--}1.26\text{V}$) With ZQ Calibration

Output Drive Strength	Min	Max	Unit
35 ohms	1.44	8.0	V/ns
50 ohms	1.2	7.0	V/ns

Table 31: Output Slew Rate Matching Ratio for NV-DDR2/NV-DDR3 Without ZQ Calibration

Drive Strength	Min	Max
Output slew rate matching ratio (pull-up to pull-down)	0.7	1.3

Notes:

- 1) The output slew rate mismatch is determined by the ratio of fast slew rate and slow slew rate. If the rising edge is faster than the falling edge, then divide the rising slew rate by the falling slew rate. If the falling edge is faster than the rising edge, then divide the falling slew rate by the rising slew rate.
- 2) The output slew rate mismatch is verified by design and characterization; It may not be subject to production testing.

Slew rates are measured under normal SSO conditions with a half of the DQ signals per data byte driving HIGH and a half of the DQ signals per data byte driving LOW. The output slew rate is measured per individual DQ signal.

UT81NDQ512G8T

12 Electrical specifications

Stresses greater than those listed can cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not guaranteed. Exposure to absolute maximum rating conditions for extended periods can affect reliability.

12.1 Absolute Maximum DC Ratings^(1,2)

Parameter		Symbol	Min ¹	Max ¹	Unit
V _{CC} =3.3V and V _{CCQ} =1.8V nominal	V _{CC} supply voltage	V _{CC}	-0.6	4.6	V
	Voltage Input	V _{IN}	-0.2	2.4	V
	V _{CCQ} supply voltage	V _{CCQ}	-0.2	2.4	V
V _{CC} =3.3V and V _{CCQ} =1.2V nominal	V _{CC} supply voltage	V _{CC}	-0.6	4.6	V
	Voltage Input	V _{IN}	-0.2	1.5	V
	V _{CCQ} supply voltage	V _{CCQ}	-0.2	1.5	V
V _{PP} supply voltage		V _{PP}	-0.6	16.0	V
V _{REFQ} supply voltage		V _{REFQ}	-0.2	2.4	V
Storage temperature		T _{STG}	-65	+150	°C
Maximum Junction temperature		T _{J max}		125	°C
Thermal impedance – Junction to Case ³		Θ _{JC}		2.68	°C/W
Maximum Power Dissipation Allowed ⁴		P _d		14.9	W

Notes:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification are not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2. Voltage on any pin relative to V_{SS}.
3. Thermal impedance junction-to-case is taken from the worst case die in the module to the center/top of the package.
4. Per MIL-STD-883, method 1012.1, section 3.4.1, PD=[T_J(max)-T_C(max)]/Θ_{JC}. Using T_C = 85°C.

UT81NDQ512G8T

12.2 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating temperature ¹	T _{OPER}	-40	-	+85	°C
V _{CC} supply voltage ²	V _{CC}	2.7	3.3	3.6	V
V _{CCQ} supply voltage (1.8V) ²	V _{CCQ}	1.7	1.8	1.95	V
V _{CCQ} supply voltage (1.2V) ²		1.14	1.2	1.26	V
V _{PP} 12V (10.8V Min) configuration	V _{PP}	10.8	12.0	13.2	V
V _{REFQ} supply voltage	V _{REFQ}	0.49 x V _{CCQ}	0.5 x V _{CCQ}	0.51 x V _{CCQ}	V
V _{SS} ground voltage	V _{SS}	0	0	0	V

Notes:

- 1) Operating temperature (T_{OPER}) is the case surface temperature on the center/top of the NAND.
- 2) AC Noise on the supply voltages shall not exceed +/- 3% (10kHz to 800MHz). AC and DC noise together shall stay within the Min-Max range specified in this table.

12.3 Operational Environment⁴

Symbol	Parameter	Limit	Units
TID ^{1,5}	Total Ionizing Dose	30 to 50	krad(Si)
SEL ²	Single Event Latchup Immunity	≤60	MeV-cm ² /mg
SEU ³	Single Event Upset Immunity	Contact Factory	MeV-cm ² /mg
SER ³	Soft Error Rate	Contact Factory	Errors/bit-day
SEFI	Single Event Functional Interrupt	Contact Factory	MeV-cm ² /mg

Notes:

- 1) For devices procured with a total ionizing dose tolerance guarantee, post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A at an effective dose rate of 0.1 rad(Si)/sec up to maximum TID level procured.
- 2) Performed at V_{CC} = 3.6 V, V_{CCQ} = 1.95V and 85°C.
- 3) Performed at V_{CC} = 2.7 V, V_{CCQ} = 1.7V/1.14V and 25°C.
- 4) Radiation testing is performed without V_{PP}. V_{PP} operations should not be used in a radiation environment. Devices using V_{PP} operations in a radiation environment will not be warranted.
- 5) TID performance may vary from wafer lot to wafer lot. Contact factory for bit error performance and availability at specific TID levels from 30 to 50 krad(Si).

12.4 Valid Block per LUN

Parameter	Symbol	Min	Max	Unit	Notes
Valid block number	NVB	1912	2016	Blocks	1

Notes:

- 1) Invalid blocks are blocks that contain one or more bad bits beyond ECC. The device may contain bad blocks upon shipment. Additional bad blocks may develop over time; however, the total number of available blocks will not drop below NVB during the endurance life of the device. Do not erase or program blocks marked invalid from the factory.

UT81NDQ512G8T

12.5 Package Electrical Specification and Pad Capacitance

The capacitance delta values in Table 32 measure the pin-to-pin capacitance for all LUNs within a package, including across data buses if the package has the same number of LUNs per x8 data bus (i.e. package channel). The capacitance delta values are not measured across data buses if the package has a different number of LUNs per x8 data bus.

For Table 33, Z_{IO} applies to DQ[7:0], DQS_t, DQS_c, RE_t and RE_c. TdIO RE applies to RE_t and RE_c. TdIO and TdIO_Mismatch applies to DQ[7:0], DQS_t and DQS_c. Mismatch and Delta values are required to be met across same data bus on given package (that is package channel), but not required across all channels on a given package. All other pins only need meet requirements described in Table 32. The DQ[7:0], DQS_t, DQS_c, RE_t and RE_c pins only need to meet the requirements in Table 33.

For each signal group defined below for Table 32, a typical capacitance value is defined and reported for each NAND Target within a package. The signal groups include all signal group pins in a single package even if the pins belong to separate I/O channels unless the package has a different number of LUNs per x8 data bus. If the package has a different number of LUNs per x8 data bus than the signal group pins are separated per each x8 data bus.

Table 32: Input Capacitance: 132-Ball BGA Package

Description	Symbol	Min	Typ	Max	Unit	Notes
Input capacitance (ALE, CLE, WE#)	C_{IN}	8.0	10.0	12.0	pF	3
Input capacitance (CE#, WP#)	C_{OTHER}	-	-	12.0	pF	
Delta input capacitance	DC_{IN}	-	-	2	pF	

Notes:

- 1) Verified in device characterization; not 100% tested.
- 2) Test conditions: $T_A = 25^{\circ}\text{C}$, $f = 100\text{ MHz}$, $V_{IN} = 0\text{V}$.
- 3) Values for C_{IN} (TYP) are estimates.

4Tb TLC NAND Flash

UT81NDQ512G8T

Table 33: Package Electrical Specifications

Description	Symbol	<=400 MT/s			533 MT/s			667 MT/s			Unit	Notes
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Input/Output Z_{PKG}	Z_{IO}	35	-	90	35	-	90	35	-	90	Ohms	1
Delta Z_{PKG} for DQS_t and DQS_c	$DZ_{IO\ DQS}$	-	-	10	-	-	10	-	-	10	Ohms	8
Input/Output Package delay	T_{dIO}	-	-	160	-	-	160	-	-	145	ps	1
Input/Output Package delay	$T_{dIO\ RE}$	-	-	160	-	-	160	-	-	145	ps	1
Input/Output Package delay mismatch	$T_{dIO\ Mismatch}$	-	-	50	-	-	40	-	-	40	ps	6
Delta package delay for DQS_t and DQS_c	$DZd_{IO\ DQS}$	-	-	10	-	-	10	-	-	10	ps	
Delta Z_{PKG} for RE_t and RE_c	$DZ_{IO\ DE}$	-	-	10	-	-	10	-	-	10	Ohms	
Delta package delay for RE_t and RE_c	DC_{IO}	-	-	10	-	-	10	-	-	10	ps	

Notes:

- 1) Z_{IO} and T_{dIO} apply to DQ[7:0], DQS_t, DQS_c, RE_t and RE_c. All other pins only need to meet Table 32 requirements.
- 2) T_{dIO} apply to DQ[7:0], DQS_t, and DQS_c. All other pins only need to meet Table 32 requirements.
- 3) Test conditions: $T_A = 25^\circ\text{C}$, $f = 100\text{ MHz}$, $V_{IN} = 0\text{V}$.
- 4) Verified in device characterization; not 100% tested. The package parasitic (L & C) are validated using package only samples. The capacitance is measured with V_{CC} , V_{CCQ} , V_{SS} , V_{SSQ} shorted with all other signal pins floating. The inductance is measured with V_{CC} , V_{CCQ} , V_{SS} , and V_{SSQ} shorted and all other signal pins shorted at the die side (not pin).
- 5) Package only impedance (Z_{PKG}) is calculated based on the L_{PKG} and C_{PKG} total for a given pin where: Z_{PKG} (total per pin) = $\text{SQRT}(L_{PKG}/C_{PKG})$.
- 6) Mismatch for T_{dIO} ($T_{dIO\ Mismatch}$) is calculated based on L_{PKG} and C_{PKG} total for a given pin where: T_{dPKG} (total per pin) = $\text{SQRT}(L_{PKG} * C_{PKG})$.
- 7) Package only delay (T_{PKG}) is calculated based on L_{PKG} and C_{PKG} total for a given pin where: T_{dPKG} (total per pin) = $\text{SQRT}(L_{PKG} * C_{PKG})$.
- 8) Delta for DQS is Absolute value of $Z_{IO}(\text{DQS}_t - Z_{IO}(\text{DQS}_c))$ for impedance (Z) or absolute value of $T_{dIO}(\text{DQS}_t) - T_{dIO}(\text{DQS}_c)$ for delay (Td).
- 9) Delta for RE is Absolute value of $Z_{IO}(\text{RE}_t - Z_{IO}(\text{RE}_c))$ for impedance (Z) or absolute value of $T_{dIO}(\text{RE}_t) - T_{dIO}(\text{RE}_c)$ for delay (Td).

4Tb TLC NAND Flash

UT81NDQ512G8T

Table 34: LUN Pad Specifications

Description	Symbol	<=400 MT/s			533 MT/s			667 MT/s			Unit	Notes
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Input/Output Pad capacitance	C_Pad _{IO}	-	-	1.6	-	-	1.6	-	-	1.6	pF	1
ZQ Pad capacitance	C_Pad _{ZQ}	-	-	1.84	-	-	1.84	-	-	1.84	pF	1
Delta Input/Output Pad capacitance for DQS_t and DQS_c	D_C_Pad _{IO DQS}	0	-	0.2	0	-	0.2	0	-	0.2	pF	4
Delta Input/Output Pad capacitance for RE_t and RE_c	D_C_Pad _{IO RE}	0	-	0.2	0	-	0.2	0	-	0.2	pF	5

Notes:

- 1) LUN Pad capacitances apply to DQ[7:0], DQS_t, DQS_c, RE_t, and RE_c. All other LUN pads only need to meet ONFI legacy capacitance requirements.
- 2) Verified in device characterization; not 100% tested. These parameters are not subject to a production test. They are verified by design and characterization. The capacitance is measured according to JEP147("PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER(VNA)") with V_{CC}, V_{CCQ}, V_{SS}, and V_{SSQ} applied and all other pins floating (except the pin under test). V_{CCQ} = 1.2V, VBIAS = V_{CCQ}/2 and on-die termination off.
- 3) These parameters apply to monolithic LUN, obtained by de-embedding the package L & C parasitics.
- 4) Delta for DQS is Absolute value of C_PAD_{IO}(DQS_t) - C_PAD_{IO}(DQS_c).
- 5) Delta for RE is Absolute value of C_PAD_{IO}(RE_t) - C_PAD_{IO}(RE_c).

12.6 DC Characteristics and Operating Conditions (Asynchronous Interface) 1.8 V_{CCQ}

Parameter	Conditions	Symbol	Single plane Typ ¹	Two plane Typ ¹	Four plane Typ ¹	Max average ¹	Max single operation ¹	Unit
Array read current (active)	SLC Mode Snap Read operation –without V _{PP}	I _{CC1_A} ⁵	33	-	-	38	38	mA
	SLC Mode operation - Without V _{PP}	I _{CC1_A}	35	51	66	80	80	
	TLC Mode Snap Read operation – without V _{PP}	I _{CC1_A} ⁵	26	-	-	33	37	
	TLC Mode operation - without V _{PP}	I _{CC1_A}	29	42	56	62	68	
	-	I _{CCQ1_A}	1.5			5		
Array program current (active)	SLC Mode operation - without V _{PP}	I _{CC2_A}	31	40	50	60	61	mA
	TLC Mode operation - without V _{PP}	I _{CC2_A}	30	42	53	58	65	
	-	I _{CCQ2_A}	2			8		
Erase current (active)	without V _{PP}	I _{CC3_A}	25	30	36	55 (90 post TID)		mA
	-	I _{CCQ3_A}	1.5			5		
I/O burst read current	^t RC= ^t RC (MIN); I _{OUT} =0mA	I _{CC4R_A}	8			10		mA
		I _{CCQ4R_A}	6			10		

4Tb TLC NAND Flash

UT81NDQ512G8T

Parameter	Conditions	Symbol	Single plane Typ ¹	Two plane Typ ¹	Four plane Typ ¹	Max ave- rage ¹	Max single operation ¹	Unit
I/O burst write current	^t WC= ^t WC (MIN)	I _{CC4w_A}	10			13		mA
		I _{CCQ4w_A}	6			10		
Bus idle current	-	I _{CC5_A}	5			7		mA
		I _{CCQ5_A}	1			7		mA
Current during first RESET command after power-on	-	I _{CC6}	38			68		mA
Power-up peak current (V _{CC})	-	I _{CC_Peak_Up} ⁴	-			20		mA
Power-down peak current (V _{CC})	-	I _{CC_Peak_Down} ⁴	-			20		mA
Power-up peak current (V _{CCQ})	-	I _{CCQ_Peak_Up} ⁴	-			10		mA
Power-down peak current (V _{CCQ})	-	I _{CCQ_Peak_Down} ⁴	-			15		mA
Standby current V _{CC}	CE# = V _{CCQ} - 0.2V; WP# = 0V/V _{CCQ}	I _{SB}	15			75 (162.5 post TID)		μA
Standby current V _{CCQ}	CE# = V _{CCQ} - 0.2V; WP# = 0V/V _{CCQ}	I _{SBQ}	10			50		μA
Staggered power-up current	^t RISE = 1ms; C _{LINE} = 0.1uF	I _{ST}	-			10		mA

Notes:

- 1) All values are per die (LUN) unless otherwise specified.
- 2) During I_{SBQ} testing, DQS_t/DQS_c , RE_t/RE_c , and $DQ[7:0]$ are floating.
- 3) During I_{CC} testing, on-die termination (ODT) is not enabled.
- 4) For the I_{CC_Peak} and I_{CCQ_Peak} currents the entire duration of the operation should be considered when calculating the maximum average current of the worst case $1\mu s$ subset of the operation.
- 5) These Snap Read operations are measured based on $SR[5]$ busy time.

4Tb TLC NAND Flash

UT81NDQ512G8T

12.7 DC Characteristics (NV-DDR2, NV-DDR3)

Table 35: DC Characteristics and Operating Conditions (NV-DDR2 Interface) 1.8V V_{CCQ}

Parameter	Conditions	Symbol	Single plane Typ ¹	Two plane Typ ¹	Four plane Typ ¹	Max ave- rage ¹	Max single operation ¹	Unit
Array read current (active)	SLC Mode Snap Read operation -without V _{PP}	I _{CC1_S}	33	-	-	38	38	mA
	SLC Mode operation - without V _{PP}	I _{CC1_S}	35	51	66	80	80	
	TLC Mode Snap Read operation - without V _{PP}	I _{CC1_S}	26	-	-	33	37	
	TLC Mode operation - without V _{PP}	I _{CC1_S}	29	42	56	62	68	
	-	I _{CCQ1_S}	1.5			5		
Array program current (active) ¹⁰	SLC Mode operation - without V _{PP}	I _{CC2_S}	31	40	50	60	61	mA
	TLC Mode operation - without V _{PP}	I _{CC2_S}	30	42	53	58	65	
	-	I _{CCQ2_S}	2			8		
Erase current (active)	without V _{PP}	I _{CC3_S}	25	30	36	55 (90 post TID)		mA
	-	I _{CCQ3_S}	1.5			5		
I/O burst read current	^t RC= ^t RC (MIN); I _{OUT} =0mA	I _{CC4R_S}	13 ³			17 ³		mA
			20 ⁴			26 ⁴		
			28 ⁵			37 ⁵		
		I _{CCQ4R_S}	18 ^{3,9}			24 ^{3,9}		
			34 ^{4,9}			40 ^{4,9}		
			45 ^{5,9}			55 ^{5,9}		
I/O burst write current	^t DSC= ^t DSC (MIN)	I _{CC4W_S}	15 ³			20 ³		mA
			20 ⁴			26 ⁴		
			25 ⁵			33 ⁵		
		I _{CCQ4W_S}	13 ³			17 ³		
			19 ⁴			25 ⁴		
			25 ⁵			33 ⁵		
Bus idle current	CE# = V _{IL}	I _{CC5_S}	5			7		mA
		I _{CCQ5_S}	5			7		mA
Power-up peak current (V _{CC})	-	I _{CC_Peak_Up} ⁷	-			20		mA
Power-down peak current (V _{CC})	-	I _{CC_Peak_Down} ⁷	-			20		mA
Power-up peak current (V _{CCQ})	-	I _{CCQ_Peak_Up} ⁷	-			10		mA

4Tb TLC NAND Flash

UT81NDQ512G8T

Parameter	Conditions	Symbol	Single plane Typ ¹	Two plane Typ ¹	Four plane Typ ¹	Max average ¹	Max single operation ¹	Unit
Power-down peak current (V _{CCQ})	-	I _{CCQ_Peak_Down} ⁷	-			15		mA
Standby current V _{CC}	CE# = V _{CCQ} - 0.2V; WP# = 0V/V _{CCQ}	I _{SB}	15			75 (162.5 post TID)		μA
Standby current V _{CCQ}	CE# = V _{CCQ} - 0.2V; WP# = 0V/V _{CCQ}	I _{SBQ}	10			50		μA

Notes:

- 1) All values are per die (LUN) unless otherwise specified.
- 2) During I_{SBQ} testing, DQS_t/DQS_c, RE_t/RE_c, and DQ[7:0] are floating.
- 3) For speeds up to 200 MT/s.
- 4) For speeds greater than 200 MT/s up to 400 MT/s.
- 5) For speeds greater than 400 MT/s.
- 6) During I_{CC} testing, on-die termination (ODT) is not enabled.
- 7) For the I_{CC_Peak} and I_{CCQ_Peak} currents the entire duration of the operation should be considered when calculating the maximum average current of the worst case 1μs subset of the operation.
- 8) N/A
- 9) For speeds up to 200 MT/s, speeds greater than 200 MT/s up to 400 MT/s and speeds greater than 400 MT/s, two-LUN-per-channel's I_{CCQ4R} MAX may increase by 10% when comparing with one LUN-per-channel's.

4Tb TLC NAND Flash

UT81NDQ512G8T

Table 36: DC Characteristics and Operating Conditions (NV-DDR3 Interface) 1.2V V_{CCQ}

Parameter	Conditions	Symbol	Single plane Typ ¹	Two plane Typ ¹	Four plane Typ ¹	Max average ¹	Max single operation ¹	Unit
Array read current (active)	SLC Mode Snap Read operation -without V _{PP}	I _{CC1_S}	33	-	-	38	38	mA
	SLC Mode operation - without V _{PP}	I _{CC1_S}	35	51	66	80	80	
	TLC Mode Snap Read operation - without V _{PP}	I _{CC1_S}	26	-	-	33	37	
	TLC Mode operation - without V _{PP}	I _{CC1_S}	29	42	56	62	68	
	-	I _{CCQ1_S}	1.5			5		
Array program current (active)	SLC Mode operation - without V _{PP}	I _{CC2_S}	31	40	50	60	61	mA
	TLC Mode operation - without V _{PP}	I _{CC2_S}	30	42	53	58	65	
	-	I _{CCQ2_S}	2			8		
Erase current (active)	without V _{PP}	I _{CC3_S}	25	30	36	55 (90 post TID)		mA
	-	I _{CCQ3_S}	1.5			5		
I/O burst read current	^t RC= ^t RC (MIN); I _{OUT} =0mA	I _{CC4R_S}	13 ³			17 ³		mA
			20 ⁴			26 ⁴		
			28 ⁵			37 ⁵		
		I _{CCQ4R_S}	18 ^{3,9}			24 ^{3,9}		
			34 ^{4,9}			34 ^{4,9}		
			45 ^{5,9}			55 ^{5,9}		
I/O burst write current	^t DSC= ^t DSC (MIN)	I _{CC4W_S}	15 ³			20 ³		mA
			20 ⁴			26 ⁴		
			25 ⁵			33 ⁵		
		I _{CCQ4W_S}	13 ³			17 ³		
			19 ⁴			25 ⁴		
			25 ⁵			33 ⁵		
Bus idle current	CE# = V _{IL}	I _{CC5_S}	5			7		mA
		I _{CCQ5_S}	5			7		mA
Power-up peak current (V _{CC})	-	I _{CC_Peak_Up} ⁷	-			20		mA
Power-down peak current (V _{CC})	-	I _{CC_Peak_Down} ⁷	-			20		mA
Power-up peak current (V _{CCQ})	-	I _{CCQ_Peak_Up} ⁷	-			10		mA

4Tb TLC NAND Flash

UT81NDQ512G8T

Parameter	Conditions	Symbol	Single plane Typ ¹	Two plane Typ ¹	Four plane Typ ¹	Max ave- rage ¹	Max single operation ¹	Unit
Power-down peak current (V _{CCQ})	-	I _{CCQ_Peak_Down} ⁷	-			15		mA
Standby current V _{CC}	CE# = V _{CCQ} - 0.2V; WP# = 0V/V _{CCQ}	I _{SB}	15			75 (162.5 post TID)		μA
Standby current V _{CCQ}	CE# = V _{CCQ} - 0.2V; WP# = 0V/V _{CCQ}	I _{SBQ}	10			50		μA

Notes:

- 1) All values are per die (LUN) unless otherwise specified.
- 2) During I_{SBQ} testing, DQS_t/DQS_c, RE_t/RE_c, and DQ[7:0] are floating.
- 3) For speeds up to 200MT/s.
- 4) For speeds greater than 200MT/s up to 400MT/s.
- 5) For speeds greater than 400MT/s up to 667MT/s.
- 6) During I_{CC} testing, on-die termination (ODT) is not enabled.
- 7) For the I_{CC_Peak} and I_{CCQ_Peak} currents the entire duration of the operation should be considered when calculating the maximum average current of the worst case 1μs subset of the operation.
- 8) N/A
- 9) For speeds up to 200MT/s, speeds greater than 200MT/s up to 400MT/s and speeds greater than 400MT/s, two-LUN-per-channel's I_{CCQ4R} MAX may increase by 10% when comparing with one-LUN-per-channel's.

4Tb TLC NAND Flash

UT81NDQ512G8T

12.8 DC Characteristics (V_{CCQ})

Table 37: Asynchronous DC Characteristics and Operating Conditions (1.8V V_{CCQ})

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
AC input high voltage	CE#, DQ[7:0], DQS, ALE, CLE, WE#, RE#, WP#	V _{IH(AC)}	0.8xV _{CCQ}	-	V _{CCQ} +0.3	V	
AC input low voltage		V _{IL(AC)}	-0.3	-	0.2xV _{CCQ}	V	
DC input high voltage	DQ[7:0], DQS, ALE, CLE, WE#, RE#	V _{IH(DC)}	0.7xV _{CCQ}	-	V _{CCQ} +0.3	V	
DC input low voltage		V _{IL(DC)}	-0.3	-	0.3xV _{CCQ}	V	
Input leakage current	Any input V _{IN} = 0V to V _{CCQ}	I _{LI}	-	-	±10	µA	1
Output leakage current	DQ are disabled; V _{OUT} = V _{CCQ}	I _{LO_PD}	-	0.3	1	µA	4
	DQ are disabled; V _{OUT} = 0V; ODT disabled	I _{LO_PU}	-	0.9	5	µA	4
Output low current (R/B#)	V _{OL} = 0.2V	I _{OL} (R/B#)	3	4	-	mA	2

Notes:

- 1) All leakage currents are per die (LUN). For example, four die (LUNs) have a maximum leakage current of ±40µA.
- 2) DC characteristics may need to be relaxed if R/B# pull-down strength is not set to full strength. See the User Manual, Feature Address 81h: Programmable R/B# Pull-Down Strength table, in the Configuration Operations section, for additional details.
- 3) See the Overshoot/Undershoot Parameters table in the AC Overshoot / Undershoot Specifications section.
- 4) Absolute leakage value per I/O per NAND LUN (DQ[7:0], DQS_t, DQS_c, RE_t, RE_c).

Table 38: NV-DDR2 DC Characteristics and Operating Conditions for Single-Ended Signals (1.8V V_{CCQ})

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
AC input high voltage	DQ[7:0], DQS, ALE, CLE, WE#, RE#	V _{IH(AC)}	V _{REFQ} +0.250	-	-	V	4
AC input low voltage		V _{IL(AC)}	-	-	V _{REFQ} +0.250	V	4
AC input high voltage	CE#, WP#	V _{IH(AC)}	0.8xV _{CCQ}	-	V _{CCQ} +0.3	V	4
AC input low voltage		V _{IL(AC)}	-0.3	-	0.2xV _{CCQ}	V	4
DC input high voltage	DQ[7:0], DQS, ALE, CLE, WE#, RE#	V _{IH(DC)}	V _{REFQ} +0.125	-	V _{CCQ} +0.3	V	2
DC input low voltage		V _{IL(DC)}	-0.3	-	V _{REFQ} -0.125	V	2
DC input high voltage	CE#, WP#	V _{IH(DC)}	0.7xV _{CCQ}	-	V _{CCQ} +0.3	V	
DC input low voltage		V _{IL(DC)}	-0.3	-	0.3xV _{CCQ}	V	
Input leakage current	Any input V _{IN} = 0V to V _{CCQ}	I _{LI}	-	-	±10	µA	1
Output leakage current	DQ are disabled; V _{OUT} = V _{CCQ}	I _{LO_PD}	-	0.3	1	µA	5
	DQ are disabled; V _{OUT} = 0V; ODT disabled	I _{LO_PU}	-	0.9	5	µA	5
Output low current (R/B#)	V _{OL} = 0.2V	I _{OL} (R/B#)	3	4	-	mA	3
V _{REFQ} leakage current	V _{REFQ} =V _{CCQ} /2 (all other pins not under test=0V)	I _{VREFQ}	-	-	±5	µA	

Notes:

- 1) All leakage currents are per die (LUN). For example, four die (LUNs) have a maximum leakage current of ±40µA.
- 2) These values are not defined. However, the single-ended signals (RE_t, RE_c, DQS_t, and DQS_c) need to be within the respective limits [V_{IH(DC)} Max, V_{IL(DC)} Min] for single-ended signals as well as the limitations for overshoot and

4Tb TLC NAND Flash

UT81NDQ512G8T

- undershoot.
- 3) DC characteristics may need to be relaxed if R/B# pull-down strength is not set to full strength. See the User Manual, Feature Address 81h: Programmable R/B# Pull-Down Strength table, in the Configuration Operations section, for additional details.
 - 4) See the Overshoot/Undershoot Parameters table in the AC Overshoot / Undershoot Specifications section.
 - 5) Absolute leakage value per I/O per NAND LUN (DQ[7:0], DQS_t, DQS_c, RE_t, RE_c).

Table 39: NV-DDR2 DC Characteristics and Operating Conditions for Differential Signals (1.8V V_{CCQ})

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Differential AC input high voltage	DQS_t, DSQ_c, RE_t, RE_c	V _{IHdiff(AC)}	2x[V _{IH(AC)} -V _{REF}]	-	See Note	V	2
Differential AC input low voltage		V _{ILdiff(AC)}	See Note	-	2x[V _{REF} -V _{IL(AC)}]	V	2
Differential DC input high voltage	DQS_t, DSQ_c, RE_t, RE_c	V _{IHdiff(DC)}	2x[V _{IH(AC)} -V _{REF}]	-	See Note	V	2
Differential DC input low voltage		V _{ILdiff(DC)}	See Note	-	2x[V _{REF} -V _{IL(AC)}]	V	2
Input leakage current	Any input V _{IN} = 0V to V _{CCQ}	I _{LI}	-	-	±10	μA	1
Output leakage current	DQ are disabled; V _{OUT} = V _{CCQ}	I _{LO_PD}	-	0.3	1	μA	5
	DQ are disabled; V _{OUT} = 0V; ODT disabled	I _{LO_PU}	-	0.9	5	μA	5
Output low current (R/B#)	V _{OL} = 0.2V	I _{OL} (R/B#)	3	4	-	mA	3
V _{REFQ} leakage current	V _{REFQ} =V _{CCQ} /2 (all other pins not under test=0V)	I _{VREFQ}	-	-	±5	μA	

Notes:

- 1) All leakage currents are per die (LUN). For example, four die (LUNs) have a maximum leakage current of ±40μA.
- 2) These values are not defined. However, the single-ended signals (RE_t, RE_c, DQS_t, and DQS_c) need to be within the respective limits [V_{IH(DC)} Max, V_{IL(DC)} Min] for single-ended signals as well as the limitations for overshoot and undershoot.
- 3) DC characteristics may need to be relaxed if R/B# pull-down strength is not set to full strength. See the User Manual, Feature Address 81h: Programmable R/B# Pull-Down Strength table, in the Configuration Operations section, for additional details.
- 4) See the Overshoot/Undershoot Parameters table in the AC Overshoot / Undershoot Specifications section.
- 5) Absolute leakage value per I/O per NAND LUN (DQ[7:0], DQS_t, DQS_c, RE_t, RE_c).

4Tb TLC NAND Flash

UT81NDQ512G8T

Table 40: NV-DDR3 DC Characteristics and Operating Conditions for Single-Ended Signals (1.2V V_{CCQ})

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
AC input high voltage	DQ[7:0], DQS, ALE, CLE, WE#, RE#	V _{IH(AC)}	V _{REFQ} +0.150	-	-	V	4
AC input low voltage		V _{IL(AC)}	-	-	V _{REFQ} +0.150	V	4
AC input high voltage	CE#, WP#	V _{IH(AC)}	0.8xV _{CCQ}	-	V _{CCQ} +0.3	V	4
AC input low voltage		V _{IL(AC)}	-0.3		0.2xV _{CCQ}	V	4
DC input high voltage	DQ[7:0], DQS, ALE, CLE, WE#, RE#	V _{IH(DC)}	V _{REFQ} +0.100	-	V _{CCQ}	V	2
DC input low voltage		V _{IL(DC)}	V _{SSQ}	-	V _{REFQ} -0.100	V	2
DC input high voltage	CE#, WP#	V _{IH(DC)}	0.7xV _{CCQ}	-	V _{CCQ} +0.3	V	
DC input low voltage		V _{IL(DC)}	-0.3		0.3xV _{CCQ}	V	
Input leakage current	Any input V _{IN} = 0V to V _{CCQ}	I _{LI}	-	-	±10	μA	1
Output leakage current	DQ are disabled; V _{OUT} = V _{CCQ}	I _{LO_PD}	-	0.3	1	μA	5
	DQ are disabled; V _{OUT} = 0V; ODT disabled	I _{LO_PU}	-	0.9	5	μA	5
Output low current (R/B#)	V _{OL} = 0.2V	I _{OL} (R/B#)	3	4	-	mA	3
V _{REFQ} leakage current	V _{REFQ} =V _{CCQ} /2 (all other pins not under test=0V)	I _{VREFQ}	-	-	±5	μA	

Notes:

- 1) All leakage currents are per die (LUN). For example, four die (LUNs) have a maximum leakage current of ±40μA.
- 2) These values are not defined. However, the single-ended signals (RE_t, RE_c, DQS_t, and DQS_c) need to be within the respective limits [V_{IH(DC)} Max, V_{IL(DC)} Min] for single-ended signals as well as the limitations for overshoot and undershoot.
- 3) DC characteristics may need to be relaxed if R/B# pull-down strength is not set to full strength. See the User Manual, Feature Address 81h: Programmable R/B# Pull-Down Strength table, in the Configuration Operations section, for additional details.
- 4) See the Overshoot/Undershoot Parameters table in the AC Overshoot / Undershoot Specifications section.
- 5) Absolute leakage value per I/O per NAND LUN (DQ[7:0], DQS_t, DQS_c, RE_t, RE_c).

UT81NDQ512G8T

Table 41: NV-DDR3 DC Characteristics and Operating Conditions for Differential Signals (1.2V V_{CCQ})

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Differential AC input high voltage	DQS_t, DSQ_c, RE_t, RE_c	V _{IHdiff(AC)}	2x[V _{IH(AC)} -V _{REF}]	-	See Note	V	2
Differential AC input low voltage		V _{ILdiff(AC)}	See Note	-	2x[V _{REF} -V _{IL(AC)}]	V	2
Differential DC input high voltage	DQS_t, DSQ_c, RE_t, RE_c	V _{IHdiff(DC)}	2x[V _{IH(AC)} -V _{REF}]	-	See Note	V	2
Differential DC input low voltage		V _{ILdiff(DC)}	See Note	-	2x[V _{REF} -V _{IL(DC)}]	V	2
Input leakage current	Any input V _{IN} = 0V to V _{CCQ}	I _{LI}	-	-	±10	µA	1
Output leakage current	DQ are disabled; V _{OUT} = V _{CCQ}	I _{LO_PD}	-	0.3	1	µA	5
	DQ are disabled; V _{OUT} = 0V; ODT disabled	I _{LO_PU}	-	0.9	5	µA	5
Output low current (R/B#)	V _{OL} = 0.2V	I _{OL} (R/B#)	3	4	-	mA	3
V _{REFQ} leakage current	V _{REFQ} =V _{CCQ} /2 (all other pins not under test=0V)	I _{VREFQ}	-	-	±5	µA	

Notes:

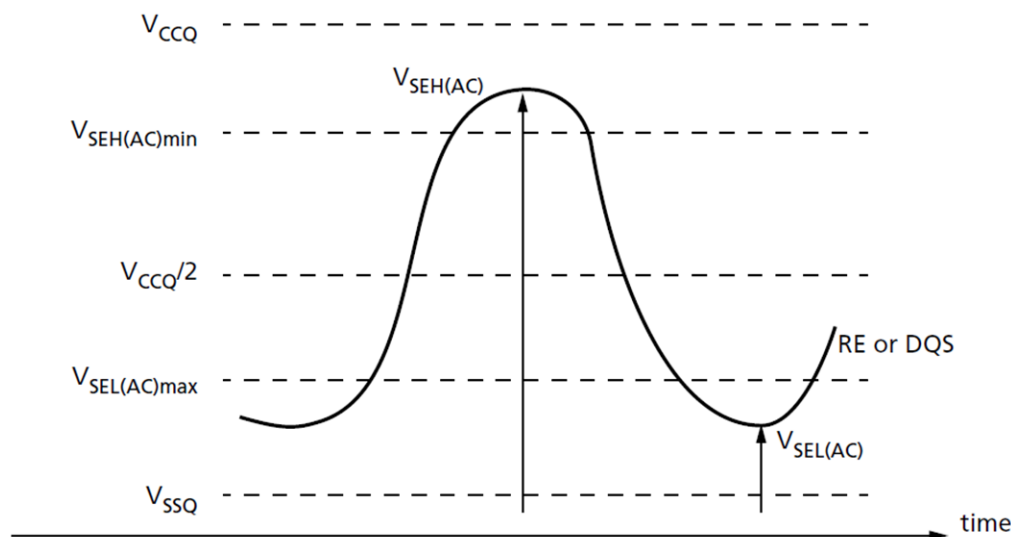
- 1) All leakage currents are per die (LUN). For example, four die (LUNs) have a maximum leakage current of ±40µA.
- 2) These values are not defined. However, the single-ended signals (RE_t, RE_c, DQS_t, and DQS_c) need to be within the respective limits [V_{IH(DC)} Max, V_{IL(DC)} Min] for single-ended signals as well as the limitations for overshoot and undershoot.
- 3) DC characteristics may need to be relaxed if R/B# pull-down strength is not set to full strength. See the User Manual, Feature Address 81h: Programmable R/B# Pull-Down Strength table, in the Configuration Operations section, for additional details.
- 4) See the Overshoot/Undershoot Parameters table in the AC Overshoot / Undershoot Specifications section.
- 5) Absolute leakage value per I/O per NAND LUN (DQ[7:0], DQS_t, DQS_c, RE_t, RE_c).

12.8.1 Single-Ended Requirements for Differential Signals

Each individual component of a differential signal (RE_t, RE_c, DQS_t, or DQS_c) shall comply with requirements for single-ended signals. RE_t and RE_c shall meet V_{SEH(AC)} Min / V_{SEL(AC)} Max in every half-cycle. DQS_t and DQS_c shall meet V_{SEH(AC)} Min/V_{SEL(AC)} Max in every half-cycle preceding and following a valid transition.

UT81NDQ512G8T

Figure 13: Single-Ended requirements for Differential Signals



While control (e.g., ALE, CLE) and DQ signal requirements are with respect to V_{REF} , the single-ended components of differential signals have a requirement with respect to $V_{CCQ}/2$; this is nominally the same. The transition of single-ended signals through the AC-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach $V_{SEL(AC)}$ Max, $V_{SEH(AC)}$ Min has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

Table 42: Single-Ended Levels for RE_t, RE_c, DQS_t, DQS_c for NV-DDR2 (1.8V V_{CCQ})

Parameter	Symbol	Min	Max	Unit	Notes
Single-Ended high level	$V_{SEH(AC)}$	$V_{CCQ}/2 + 0.250$	See Note	V	1
Single-Ended low level	$V_{SEL(AC)}$	See Note	$V_{CCQ}/2 - 0.250$	V	1

Note:

- These values are not defined. However, the single-ended signals (RE_t, RE_c, DQS_t, and DQS_c) need to be within the respective limits [$V_{IH(DC)}$ Max, $V_{IL(DC)}$ Min] for single-ended signals as well as the limitations for overshoot and undershoot.

Table 43: Single-Ended Levels for RE_t, RE_c, DQS_t, DQS_c for NV-DDR3 (1.2V V_{CCQ})

Parameter	Symbol	Min	Max	Unit	Notes
Single-Ended high level	$V_{SEH(AC)}$	$V_{CCQ}/2 + 0.150$	See Note	V	1
Single-Ended low level	$V_{SEL(AC)}$	See Note	$V_{CCQ}/2 - 0.150$	V	1

Note:

- These values are not defined. However, the single-ended signals (RE_t, RE_c, DQS_t, and DQS_c) need to be within the respective limits [$V_{IH(DC)}$ Max, $V_{IL(DC)}$ Min] for single-ended signals as well as the limitations for overshoot and undershoot.

Table 44: Differential AC Input/Output Parameters

Parameter	Symbol	Min	Max	Unit	Notes
AC differential input cross-point voltage relative to $V_{CCQ}/2$: NV-DDR2 interface	$V_{IX(AC)}$	$0.5 \times V_{CCQ} - 0.175$	$0.5 \times V_{CCQ} + 0.175$	V	1
AC differential input cross-point voltage relative to $V_{CCQ}/2$: NV-DDR3 interface	$V_{IX(AC)}$	$0.5 \times V_{CCQ} - 0.120$	$0.5 \times V_{CCQ} + 0.120$	V	1
AC differential output cross-point voltage without ZQ calibration	$V_{OX(AC)}$	$0.5 \times V_{CCQ} - 0.2$	$0.5 \times V_{CCQ} + 0.2$	V	2,3,4

4Tb TLC NAND Flash

UT81NDQ512G8T

Parameter	Symbol	Min	Max	Unit	Notes
AC differential output cross-point voltage with ZQ calibration	$V_{OX(AC)}$	$0.5 \times V_{CCQ} - 0.150$	$0.5 \times V_{CCQ} + 0.150$	V	2,3,4

Note:

- 1) The typical value of $V_{IX(AC)}$ is expected to be $0.5 \times V_{CCQ}$ of the transmitting device. $V_{IX(AC)}$ is expected to track variations in V_{CCQ} . $V_{IX(AC)}$ indicates the voltage at which differential input signals shall cross.
- 2) The typical value of $V_{OX(AC)}$ is expected to be $0.5 \times V_{CCQ}$ of the transmitting device. $V_{OX(AC)}$ is expected to track variations in V_{CCQ} . $V_{OX(AC)}$ indicates the voltage at which differential input signals shall cross.
- 3) $V_{OX(AC)}$ is measured with $\frac{1}{2}$ DQ signals per data byte driving logic HIGH and $\frac{1}{2}$ DQ signals per data byte driving logic LOW.
- 4) $V_{OX(AC)}$ is verified by design and characterization; it may not be subject to production testing.

12.8.2 Testing Conditions

The following table is to be used for the testing conditions of all the Electrical Specifications – AC Characteristics and Operating Conditions parameters.

Table 45: Test Conditions¹

Parameter	Asynchronous	NV-DDR2 and NV-DDR3 single-ended	NV-DDR2 and NV-DDR3 differential	Notes
Rising input transition	$V_{IL(DC)}$ to $V_{IH(AC)}$	$V_{IL(DC)}$ to $V_{IH(AC)}$	$V_{ILdiff(DC)}$ max to $V_{IHdiff(AC)}$ min	2
Falling input transition	$V_{IH(DC)}$ to $V_{IL(AC)}$	$V_{IH(DC)}$ to $V_{IL(AC)}$	$V_{IHdiff(DC)}$ max to $V_{ILdiff(AC)}$ min	2
Input rise and fall slew rates	1 V/ns	1 V/ns	2 V/ns	-
Input timing levels	$V_{CCQ}/2$	V_{REFQ}	cross-point	-
Output timing levels	$V_{CCQ}/2$	V_{TT}	cross-point	5
Drive strength	35 Ohms	35 Ohms	35 Ohms	
Output reference load	50 Ohms to V_{TT}	50 Ohms to V_{TT}	50 Ohms to V_{TT}	4, 5

Notes:

- 1) Test conditions that shall be used to verify compliance with a particular timing mode for devices
- 2) The receiver will effectively switch as a result of the signal crossing the AC input level; it will remain in that status as long as the signal does not ring back above (below) the DC input LOW (HIGH) level.
- 3) Transmission line delay is assumed to be very small.
- 4) This test setup applies to all package configurations.
- 5) V_{TT} is $0.5 \times V_{CCQ}$.

12.9 AC Characteristics (Asynchronous)

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Mode 5		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Clock period		100		50		35		30		25		20		ns	
Frequency		≈ 10		≈ 20		≈ 28		≈ 33		≈ 40		≈ 50		MHz	
ALE to data start	t_{ADL}	150	–	150	–	150	–	150	–	150	–	150	–	ns	1
ALE hold time	t_{ALH}	20	–	10	–	10	–	5	–	5	–	5	–	ns	
ALE setup time	t_{ALS}	50	–	25	–	15	–	10	–	10	–	10	–	ns	
ALE to RE# delay	t_{AR}	25	–	10	–	10	–	10	–	10	–	10	–	ns	
CE# access time	t_{CEA}	–	100	–	45	–	30	–	25	–	25	–	25	ns	

4Tb TLC NAND Flash

UT81NDQ512G8T

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Mode 5		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
CE# HIGH hold time prior to VOLUME SELECT (E1h)	t_{CEH}	20	–	20	–	20	–	20	–	20	–	20	–	ns	
CE# hold time	t_{CH}	20	–	10	–	10	–	5	–	5	–	5	–	ns	
Delay before CE# HIGH for any volume after a volume is selected	t_{CEVDLY}	50	–	50	–	50	–	50	–	50	–	50	–	ns	
CE# HIGH to output High-Z	t_{CHZ}	–	100	–	50	–	50	–	50	–	30	–	30	ns	2
CLE hold time	t_{CLH}	20	–	10	–	10	–	5	–	5	–	5	–	ns	
CLE to RE# delay	t_{CLR}	20	–	10	–	10	–	10	–	10	–	10	–	ns	
CLE setup time	t_{CLS}	50	–	25	–	15	–	10	–	10	–	10	–	ns	
CE# HIGH to output hold	t_{COH}	0	–	15	–	15	–	15	–	15	–	15	–	ns	
CE# setup time	t_{CS}	70	–	35	–	25	–	25	–	20	–	15	–	ns	
CE# to RE# LOW or RE_t/RE_c	t_{CR}	10	–	10	–	10	–	10	–	10	–	10	–	ns	
CE# to RE# LOW after CE# has been HIGH for >1 μ s	t_{CR2}	100	–	100	–	100	–	100	–	100	–	100	–	ns	
	t_{CR2} (Read ID)	150	–	150	–	150	–	150	–	150	–	150	–	ns	5
CE# setup time for data input after CE# has been HIGH for >1 μ s	t_{CR3}	100	–	100	–	100	–	100	–	100	–	100	–	ns	
Data hold time	t_{DH}	20	–	10	–	5	–	5	–	5	–	5	–	ns	
Data setup time	t_{DS}	40	–	20	–	15	–	10	–	10	–	7	–	ns	
ENi LOW until any issued command is ignored	t_{ENi}	–	15	–	15	–	15	–	15	–	15	–	15	ns	
CE# LOW until ENo LOW	t_{ENo}	–	50	–	50	–	50	–	50	–	50	–	50	ns	
Output High-Z to RE# LOW	t_{IR}	10	–	0	–	0	–	0	–	0	–	0	–	ns	
RE# cycle time	t_{RC}	100	–	50	–	35	–	30	–	25	–	20	–	ns	
RE# access time	t_{REA}	–	40	–	30	–	25	–	20	–	20	–	16	ns	3
RE# HIGH hold time	t_{REH}	30	–	15	–	15	–	10	–	10	–	7	–	ns	3

4Tb TLC NAND Flash

UT81NDQ512G8T

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Mode 5		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
RE# HIGH to output hold	t_{RHOH}	0	–	15	–	15	–	15	–	15	–	15	–	ns	3
RE# HIGH to WE# LOW	t_{RHW}	200	–	100	–	100	–	100	–	100	–	100	–	ns	
RE# HIGH to output High-Z	t_{RHZ}	–	200	–	100	–	100	–	100	–	100	–	100	ns	2, 3
RE# LOW to output Hold	t_{RLOH}	0	–	0	–	0	–	0	–	5	–	5	–	ns	3
RE# pulse width	t_{RP}	50	–	25	–	17	–	15	–	12	–	10	–	ns	
Ready to RE# LOW	t_{RR}	40	–	20	–	20	–	20	–	20	–	20	–	ns	
WE# HIGH to R/B# LOW	t_{WB}	–	200	–	100	–	100	–	100	–	100	–	100	ns	4
WE# cycle time	t_{WC}	100	–	45	–	35	–	30	–	25	–	20	–	ns	
WE# HIGH hold time	t_{WH}	30	–	15	–	15	–	10	–	10	–	7	–	ns	
WE# HIGH to RE# LOW	t_{WHR}	120	–	80	–	80	–	60	–	60	–	60	–	ns	
WE# pulse width	t_{WP}	50	–	25	–	17	–	15	–	12	–	10	–	ns	
WP# transition to WE# LOW	t_{WW}	100	–	100	–	100	–	100	–	100	–	100	–	ns	
Delay before next command after a volume is selected	t_{VDLY}	50	–	50	–	50	–	50	–	50	–	50	–	ns	

Notes:

- 1) Timing for t_{ADL} begins in the address cycle, on the final rising edge of WE# and ends with the first rising edge of WE# for data input. t_{ADL} SPEC for SET FEATURES operations is 70ns.
- 2) Data transition is measured ± 200 mV from steady-state voltage with load. This parameter is sampled and not 100 percent tested.
- 3) AC characteristics may need to be relaxed if output drive strength is not set to at least nominal.
- 4) Any command (including READ STATUS commands) cannot be issued during t_{WB} , even if R/B# or RDY is ready.
- 5) t_{CR2} (MIN) is 150ns for read ID sequence only. For all other command sequences t_{CR2} (MIN) requirement is 100ns.

12.10 AC Characteristics (NV-DDR2, NV-DDR3)**Table 46: AC Characteristics: NV-DDR2/NV-DDR3 Command, Address, and Data for Modes 0–4**

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Clock period		30		25		15		12		10		ns	
Frequency		≈33		≈40		≈66		≈83		≈100		MHz	
Command and Address													
Access window of DQ[7:0] from RE# LOW or RE_t/RE_c	tAC	3	25	3	25	3	25	3	25	3	25	ns	

4Tb TLC NAND Flash

UT81NDQ512G8T

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
ALE to data loading time	t_{ADL}	150	–	150	–	150	–	150	–	150	–	ns	13
ALE to RE# LOW or RE_t/RE_c	t_{AR}	10	–	10	–	10	–	10	–	10	–	ns	
DQ hold – command, address	t_{CAH}	5	–	5	–	5	–	5	–	5	–	ns	
ALE, CLE hold	t_{CALH}	5	–	5	–	5	–	5	–	5	–	ns	
ALE, CLE setup with ODT disabled	t_{CALS}	15	–	15	–	15	–	15	–	15	–	ns	
ALE, CLE setup with ODT enabled	t_{CALS2}	25	–	25	–	25	–	25	–	25	–	ns	
DQ setup – command, address	t_{CAS}	5	–	5	–	5	–	5	–	5	–	ns	
CE# HIGH hold time prior to VOLUME SELECT (E1h)	t_{CEH}	20	–	20	–	20	–	20	–	20	–	ns	
Delay before CE# HIGH for any volume after a volume is selected	t_{CEVDLY}	50	–	50	–	50	–	50	–	50	–	ns	
CE# hold	t_{CH}	5	–	5	–	5	–	5	–	5	–	ns	
CE# HIGH to output High-Z	t_{CHZ}	–	30	–	30	–	30	–	30	–	30	ns	1
CLE HIGH to output High-Z	t_{CLHZ}	–	30	–	30	–	30	–	30	–	30	ns	1
CLE to RE# LOW or RE_t/RE_c	t_{CLR}	10	–	10	–	10	–	10	–	10	–	ns	
CE# to RE# LOW or RE_t/RE_c	t_{CR}	10	–	10	–	10	–	10	–	10	–	ns	
CE# to RE# LOW or RE_t/RE_c if CE# has been HIGH for >1 μ s	t_{CR2}	100	–	100	–	100	–	100	–	100	–	ns	
	t_{CR2} (Read ID)	150	–	150	–	150	–	150	–	150	–	ns	14
CE# setup	t_{CS}	20	–	20	–	20	–	20	–	20	–	ns	
CE# setup for data output with ODT disabled	t_{CS1}	30	–	30	–	30	–	30	–	30	–	ns	
CE# setup for DQS/DQ[7:0] with ODT enabled	t_{CS2}	40	–	40	–	40	–	40	–	40	–	ns	17
CE# setup time to DQS (DQS_t) low after CE# has been HIGH for >1 μ s	t_{CD}	100	–	100	–	100	–	100	–	100	–	ns	

4Tb TLC NAND Flash

UT81NDQ512G8T

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
ALE, CLE, WE#, hold time from CE# HIGH	t ^{CSD}	10	–	10	–	10	–	10	–	10	–	ns	
ENi LOW until any issued command is ignored	t ^{ENi}	–	15	–	15	–	15	–	15	–	15	ns	
CE_# LOW until ENo LOW	t ^{ENo}	–	50	–	50	–	50	–	50	–	50	ns	
Ready to data output	t ^{RR}	20	–	20	–	20	–	20	–	20	–	ns	
WE# HIGH to R/B# LOW	t ^{WB}	–	100	–	100	–	100	–	100	–	100	ns	16
WE# cycle time	t ^{WC}	25	–	25	–	25	–	25	–	25	–	ns	
WE# pulse width	t ^{WH}	11	–	11	–	11	–	11	–	11	–	ns	
Command cycle to data output	t ^{WHR}	80	–	80	–	80	–	80	–	80	–	ns	
WE# pulse width	t ^{WP}	11	–	11	–	11	–	11	–	11	–	ns	
WP# transition to command cycle	t ^{WW}	100	–	100	–	100	–	100	–	100	–	ns	
Delay before next command after a volume is selected	t ^{VDLY}	50	–	50	–	50	–	50	–	50	–	ns	
Jitter													
The deviation of a given t ^{DQS(abs)} /t ^{DSC(abs)} from a t ^{DQS(avg)} / t ^{DSC(avg)}	t ^{JITper} (DQS)	-2.4	2.4	-2.0	2.0	-1.2	1.2	-1.0	1.0	-0.8	0.8	ns	3, 5, 7
The deviation of a given t ^{RC(abs)} /t ^{DSC(abs)} from a t ^{RC(avg)} / t ^{DSC(avg)}	t ^{JITper} (RE#)	-1.8	1.8	-1.5	1.5	-0.9	0.9	-0.75	0.75	-0.6	0.6	ns	3, 5, 7
Cycle to cycle jitter for DQS	t ^{JITcc} (DQS)	–	4.8	–	4.0	–	2.4	–	2.0	–	1.6	ns	3, 6
Cycle to cycle jitter for RE#	t ^{JITcc} (RE#)	–	3.6	–	3.0	–	1.8	–	1.5	–	1.2	ns	3, 6
Data Input													
DQS setup time for data input start	t ^{CDQSS}	30	–	30	–	30	–	30	–	30	–	ns	
DQS hold time for data input burst end	t ^{CDQSH}	100	–	100	–	100	–	100	–	100	–	ns	

4Tb TLC NAND Flash

UT81NDQ512G8T

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
DQS (DQS_t) HIGH and RE# (RE_t) HIGH setup to ALE, CLE and CE# LOW during data burst	t_{DBS}	5	–	5	–	5	–	5	–	5	–	ns	
Data In hold	t_{DH}	4.0	–	3.3	–	2.0	–	1.1	–	0.7	–	ns	10
Data In setup	t_{DS}	4.0	–	3.3	–	2.0	–	1.1	–	0.7	–	ns	10
DQ input pulse width	t_{DIPW}	0.31	–	0.31	–	0.31	–	0.31	–	0.31	–	$t_{DCS}(avg)$	12
DQS input high pulse width	t_{DQSH}	0.43	–	0.43	–	0.43	–	0.43	–	0.43	–	$t_{DCS}(avg)$	
DQS input low pulse width	t_{DQSL}	0.43	–	0.43	–	0.43	–	0.43	–	0.43	–	$t_{DCS}(avg)$	
Average DQS cycle time	$t_{DCS}(avg)$ or t_{DCS}	30	–	25	–	15	–	12	–	10	–	ns	2
Absolute DQS cycle time, from rising edge to rising edge	$t_{DCS}(abs)$	$t_{DSC}(abs) (MIN) = t_{DSC}(avg) + t_{JITper}(DQS) (MIN)$ $t_{DSC}(abs) (MAX) = t_{DSC}(avg) + t_{JITper}(DQS) (MAX)$										ns	
ENi LOW until any issued command is ignored	t_{ENi}	–	15	–	15	–	15	–	15	–	15	ns	
CE# LOW until ENo LOW	t_{ENo}	–	50	–	50	–	50	–	50	–	50	ns	
DQS write preamble with ODT disabled	t_{WPRE}	15	–	15	–	15	–	15	–	15	–	ns	
DQS write preamble with ODT enabled	t_{WPRE2}	25	–	25	–	25	–	25	–	25	–	ns	
DQS write postamble	t_{WPST}	6.5	–	6.5	–	6.5	–	6.5	–	6.5	–	ns	
DQS write postamble hold time	t_{WPSTH}	25	–	25	–	25	–	25	–	25	–	ns	
Data Output													
Access window of DQ[7:0] from CLK	t_{AC}	3	25	3	25	3	25	3	25	3	25	ns	
DQS (DQS_t) HIGH and RE# (RE_t) HIGH setup to ALE, CLE, and CE# LOW during data burst	t_{DBS}	5	–	5	–	5	–	5	–	5	–	ns	
DQS-DQ skew	t_{DQSQ}	–	2.5	–	2.0	–	1.4	–	1.0	–	0.8	ns	
Access window of DQS from RE# or RE_t/RE_c	t_{DQSRE}	3	25	3	25	3	25	3	25	3	25	ns	
RE# LOW to DQS or DQ[7:0] driven	t_{DQSD}	6	18	6	18	6	18	6	18	6	18	ns	

4Tb TLC NAND Flash

UT81NDQ512G8T

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
DQS hold time after RE# LOW or RE_t/RE_c crosspoint	t_{DQSRH}	5	–	5	–	5	–	5	–	5	–	ns	15
Data valid window	t_{DVW}	$t_{\text{DVW}} = t_{\text{QH}} - t_{\text{DQSQ}}$										ns	
DQ-DQS hold, DQS to first DQ to go nonvalid, per access	t_{QH}	0.37	–	0.37	–	0.37	–	0.37	–	0.37	–	$t_{\text{RC}}(\text{avg})$	9, 11
DQS (DQS_t/DQS_c) output HIGH time	t_{QSH}	0.37	–	0.37	–	0.37	–	0.37	–	0.37	–	$t_{\text{RC}}(\text{avg})$	9, 11
DQS (DQS_t/DQS_c) output LOW time	t_{QSL}	0.37	–	0.37	–	0.37	–	0.37	–	0.37	–	$t_{\text{RC}}(\text{avg})$	9, 11
Average RE# cycle time	$t_{\text{RC}}(\text{avg})$ or t_{RC}	30	–	25	–	15	–	12	–	10	–	ns	2
Absolute RE# cycle time	$t_{\text{RC}}(\text{abs})$	$t_{\text{RC}}(\text{abs})(\text{MIN}) = t_{\text{RC}}(\text{avg}) + t_{\text{JITper}}(\text{RE\#})(\text{MIN})$ $t_{\text{RC}}(\text{abs})(\text{MAX}) = t_{\text{RC}}(\text{avg}) + t_{\text{JITper}}(\text{RE\#})(\text{MAX})$										ns	
Average RE# HIGH hold time	$t_{\text{REH}}(\text{avg})$	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	$t_{\text{RC}}(\text{avg})$	4
Absolute RE# HIGH hold time	$t_{\text{REH}}(\text{abs})$	0.43	–	0.43	–	0.43	–	0.43	–	0.43	–	$t_{\text{RC}}(\text{avg})$	
Data output to command, address, or data input	t_{RHW}	100	–	100	–	100	–	100	–	100	–	ns	
Average RE# pulse width	$t_{\text{RP}}(\text{avg})$	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	$t_{\text{RC}}(\text{avg})$	4
Absolute RE# pulse width	$t_{\text{RP}}(\text{abs})$	0.43	–	0.43	–	0.43	–	0.43	–	0.43	–	$t_{\text{RC}}(\text{avg})$	
Read preamble with ODT disabled	t_{RPRE}	15	–	15	–	15	–	15	–	15	–	ns	
Read preamble with ODT enabled	t_{RPRE2}	25	–	25	–	25	–	25	–	25	–	ns	
Read postamble	t_{RPST}	$t_{\text{RPST}}(\text{MIN}) = t_{\text{DQSRE}} + 0.5 \times t_{\text{RC}}$ $t_{\text{RPST}}(\text{MAX}) = -$										ns	
Read postamble hold time	t_{RPSTH}	15	–	15	–	15	–	15	–	15	–	ns	

Notes:

- 1) t_{CHZ} and t_{CLHZ} are not referenced to a specific voltage level, but specify when the device output is no longer driving.
- 2) The parameters $t_{\text{RC}}(\text{avg})$ and $t_{\text{DSC}}(\text{avg})$ are the average over any 200 consecutive periods and $t_{\text{RC}}(\text{avg})/t_{\text{DSC}}(\text{avg})$ min are the smallest rates allowed, with the exception of a deviation due to $t_{\text{JIT}}(\text{per})$.
- 3) Input jitter is allowed provided it does not exceed values specified.
- 4) $t_{\text{REH}}(\text{avg})$ and $t_{\text{RP}}(\text{avg})$ are the average half clock period over any 200 consecutive clocks and is the smallest half period allowed, expect a deviation due to the allowed clock jitter. Input clock jitter is allowed provided it does not exceed values specified.
- 5) The period jitter $t_{\text{JIT}}(\text{per})$ is the maximum deviation in the t_{RC} or t_{DSC} period from the average or nominal t_{RC} or t_{DSC} period. It is allowed in either the positive or negative direction.

UT81NDQ512G8T

- 6) The cycle-to-cycle jitter t_{JITcc} is the amount the clock period can deviate from one cycle to the next.
- 7) The duty cycle jitter applies to either the high pulse or low pulse; however, the two cumulatively cannot exceed t_{JITper} . As long as the absolute minimum half period $t_{RP(abs)}$, $t_{REH(abs)}$, t_{DQSH} , or t_{DQSL} is not less than 43 percent of the average cycle.
- 8) All timing parameter values assume differential signaling for RE# and DQS is used.
- 9) When the device is operated with input clock jitter, t_{QSL} , t_{QSH} , and t_{QH} need to be derated by the actual t_{JITper} in the input clock. (output deratings are relative to the NAND input RE pulse that generated the DQS pulse).
- 10) The t_{DS} and t_{DH} times listed are based on an input slew rate greater than or equal to 1 V/ns for single-ended signal, and based on an input slew rate greater than or equal to 2 V/ns for differential signal. If the input slew rate is less than 1 V/ns for single-ended signal, or less than 2 V/ns for differential signal, then the derating methodology should be used.
- 11) When the device is operated with input RE (RE_t/RE_c) jitter, t_{QSL} , t_{QSH} , and t_{QH} need to be derated by the actual input duty cycle jitter beyond $0.45 \times t_{RC(avg)}$ but not exceeding $0.43 \times t_{RC(avg)}$. Output deratings are relative to the device input RE pulse that generated the DQS pulse.
- 12) The parameter t_{DIPW} is defined as the pulse width of the input signal between the first crossing of $V_{REFQ(DC)}$ and the consecutive crossing of $V_{REFQ(DC)}$.
- 13) t_{ADL} SPEC for SET FEATURES operations is 70ns.
- 14) t_{CR2} (MIN) is 150ns for Read ID sequence only. For all other command sequences t_{CR2} (MIN) requirement is 100ns.
- 15) t_{DQSRH} is only required if Matrix ODT is enabled.
- 16) Any command (including READ STATUS commands) cannot be issued during t_{WB} , even if R/B# or RDY is ready.
- 17) t_{CS2} should be applied when the device has any type of ODT enabled including ODT only enabled for data input.

Table 47: AC Characteristics: NV-DDR2/NV-DDR3 Command, Address, and Data for Timing Modes 5–7

Parameter	Symbol	Mode 5		Mode 6		Mode 7		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Clock period		7.5		6		5		ns	
Frequency		≈133		≈166		≈200		MHz	
Command and Address									
Access window of DQ[7:0] from RE# LOW or RE_t/RE_c	tAC	3	25	3	25	3	25	ns	
ALE to data loading time	tADL	150	–	150	–	150	–	ns	13
ALE to RE# LOW or RE_t/RE_c	tAR	10	–	10	–	10	–	ns	
DQ hold – command, address	tCAH	5	–	5	–	5	–	ns	
ALE, CLE hold	tCALH	5	–	5	–	5	–	ns	
ALE, CLE setup with ODT disabled	tCALS	15	–	15	–	15	–	ns	
ALE, CLE setup with ODT enabled	tCALS2	25	–	25	–	25	–	ns	
DQ setup – command, address	tCAS	5	–	5	–	5	–	ns	
CE# HIGH hold time	tCEH	20	–	20	–	20	–	ns	
Delay before CE# HIGH for any volume after a volume is selected	tCEVDLY	50	–	50	–	50	–	ns	
CE# hold	tCH	5	–	5	–	5	–	ns	
CE# HIGH to output High-Z	tCHZ	–	30	–	30	–	30	ns	1
CLE HIGH to output High-Z	tCLHZ	–	30	–	30	–	30	ns	1
CLE to RE# LOW or RE_t/RE_c	tCLR	10	–	10	–	10	–	ns	
CE# to RE# LOW or RE_t/RE_c	tCR	10	–	10	–	10	–	ns	
CE# to RE# LOW or RE_t/RE_c if CE# has been HIGH for >1μs	tCR2	100	–	100	–	100	–	ns	
	tCR2 (Read ID)	150	–	150	–	150	–	ns	14

4Tb TLC NAND Flash

UT81NDQ512G8T

Parameter	Symbol	Mode 5		Mode 6		Mode 7		Unit	Notes
		Min	Max	Min	Max	Min	Max		
CE# setup	t_{CS}	20	–	20	–	20	–	ns	
CE# setup for data output with ODT disabled	t_{CS1}	30	–	30	–	30	–	ns	
CE# setup for DQS/DQ[7:0] with ODT enabled	t_{CS2}	40	–	40	–	40	–	ns	17
CE# setup time to DQS (DQS_t) low after CE# has been HIGH for $>1\mu s$	t_{CD}	100	–	100	–	100	–	ns	
ALE, CLE, WE#, hold time from CE# HIGH	t_{CSD}	10	–	10	–	10	–	ns	
ENi LOW until any issued command is ignored	t_{ENi}	–	15	–	15	–	15	ns	
CE# LOW until ENo LOW	t_{ENo}	–	50	–	50	–	50	ns	
Ready to data output	t_{RR}	20	–	20	–	20	–	ns	
WE# HIGH to R/B# LOW	t_{WB}	–	100	–	100	–	100	ns	16
WE# cycle time	t_{WC}	25	–	25	–	25	–	ns	
WE# pulse width	t_{WH}	11	–	11	–	11	–	ns	
Command cycle to data output	t_{WHR}	80	–	80	–	80	–	ns	
WE# pulse width	t_{WP}	11	–	11	–	11	–	ns	
WP# transition to command cycle	t_{WW}	100	–	100	–	100	–	ns	
Delay before next command after a volume is selected	t_{VDLY}	50	–	50	–	50	–	ns	
Jitter									
The deviation of a given $t_{DQS(ABS)}/t_{DSC(ABS)}$ from a $t_{DQS(AVG)}/t_{DSC(AVG)}$	$t_{JITper} (DQS)$	-0.6	0.6	-0.48	0.48	-0.40	0.40	ns	3,5,7
The deviation of a given $t_{RC(ABS)}/t_{DSC(ABS)}$ from a $t_{RC(AVG)}/t_{DSC(AVG)}$	$t_{JITper} (RE\#)$	-0.45	0.45	-0.36	0.36	-0.30	0.30	ns	3,5,7
Cycle to cycle jitter for DQS	$t_{JITcc} (DQS)$	–	1.2	–	0.96	–	0.80	ns	3,6
Cycle to cycle jitter for RE#	$t_{JITcc} (RE\#)$	–	0.9	–	0.72	–	0.60	ns	3,6
Data Input									
DQS setup time for data input start	t_{CDQSS}	30	–	30	–	30	–	ns	
DQS hold time for data input burst end	t_{CDQSH}	100	–	100	–	100	–	ns	
DQS (DQS_t) HIGH and RE# (RE_t) HIGH setup to ALE, CLE and CE# LOW during data burst	t_{DBS}	5	–	5	–	5	–	ns	
Data In hold	t_{DH}	0.6	–	0.55	–	0.40	–	ns	10
Data In setup	t_{DS}	0.6	–	0.55	–	0.40	–	ns	10
DQ input pulse width	t_{DIPW}	0.31	–	0.31	–	0.31	–	$t_{DCS(AVG)}$	12
DQS input high pulse width	t_{DQSH}	0.43	–	0.43	–	0.43	–	$t_{DCS(AVG)}$	
DQS input low pulse width	t_{DQSL}	0.43	–	0.43	–	0.43	–	$t_{DCS(AVG)}$	

4Tb TLC NAND Flash

UT81NDQ512G8T

Parameter	Symbol	Mode 5		Mode 6		Mode 7		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Average DQS cycle time	$t_{DCS(avg)}$ or t_{DCS}	7.5	–	6	–	5	–	ns	2
Absolute DQS cycle time, from rising edge to rising edge	$t_{DCS(abs)}$	$t_{DSC(abs)MIN} = t_{DSC(avg)} + t_{JITper(DQS)MIN}$ $t_{DSC(abs)MAX} = t_{DSC(avg)} + t_{JITper(DQS)MAX}$						ns	
ENi LOW until any issued command is ignored	t_{ENi}	–	15	–	15	–	15	ns	
CE# LOW until ENo LOW	t_{ENo}	–	50	–	50	–	50	ns	
DQS write preamble with ODT disabled	t_{WPRE}	15	–	15	–	15	–	ns	
DQS write preamble with ODT enabled	t_{WPRE2}	25	–	25	–	25	–	ns	
DQS write postamble	t_{WPST}	6.5	–	6.5	–	6.5	–	ns	
DQS write postamble hold time	t_{WPSTH}	25	–	25	–	25	–	ns	
Data Output									
Access window of DQ[7:0] from CLK	t_{AC}	3	25	3	25	3	25	ns	
DQS (DQS_t) HIGH and RE# (RE_t) HIGH setup to ALE, CLE, and CE# LOW during data burst	t_{DBS}	5	–	5	–	5	–	ns	
DQS-DQ skew	t_{DQSQ}	–	0.6	–	0.5	–	0.4	ns	
Access window of DQS from RE# or RE_t/RE_c	t_{DQSRE}	3	25	3	25	3	25	ns	
RE# LOW to DQS or DQ[7:0] driven	t_{DQSD}	6	18	6	18	6	18	ns	
DQS hold time after RE# LOW or RE_t/RE_c crosspoint	t_{DQSRH}	5	–	5	–	5	–	ns	15
Data valid window	t_{DVW}	$t_{DVW} = t_{QH} - t_{DQSQ}$						ns	
DQ-DQS hold, DQS to first DQ to go nonvalid, per access	t_{QH}	0.37	–	0.37	–	0.37	–	$t_{RC(avg)}$	9,11
DQS (DQS_t/DQS_c) output HIGH time	t_{QSH}	0.37	–	0.37	–	0.37	–	$t_{RC(avg)}$	9,11
DQS (DQS_t/DQS_c) output LOW time	t_{QSL}	0.37	–	0.37	–	0.37	–	$t_{RC(avg)}$	9,11
Average RE# cycle time	$t_{RC(avg)}$ or t_{RC}	7.5	–	6	–	5	–	ns	2
Absolute RE# cycle time	$t_{RC(abs)}$	$t_{RC(abs)MIN} = t_{RC(avg)} + t_{JITper(RE\#)MIN}$ $t_{RC(abs)MAX} = t_{RC(avg)} + t_{JITper(RE\#)MAX}$						ns	
Average RE# HIGH hold time	$t_{REH(avg)}$	0.45	0.55	0.45	0.55	0.45	0.55	$t_{RC(avg)}$	4
Absolute RE# HIGH hold time	$t_{REH(abs)}$	0.43	–	0.43	–	0.43	–	$t_{RC(avg)}$	
Data output to command, address, or data input	t_{RHW}	100	–	100	–	100	–	ns	
Average RE# pulse width	$t_{RP(avg)}$	0.45	0.55	0.45	0.55	0.45	0.55	$t_{RC(avg)}$	4
Absolute RE# pulse width	$t_{RP(abs)}$	0.43	–	0.43	–	0.43	–	$t_{RC(avg)}$	
Read preamble with ODT disabled	t_{RPRE}	15	–	15	–	15	–	ns	

4Tb TLC NAND Flash

UT81NDQ512G8T

Parameter	Symbol	Mode 5		Mode 6		Mode 7		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read preamble with ODT enabled	t_{RPRE2}	25	–	25	–	25	–	ns	
Read postamble	t_{RPST}	$t_{RPST} (MIN) = t_{DQSRE} + 0.5 \times t_{RC}$ $t_{RPST} (MAX) = -$						ns	
Read postamble hold time	t_{RPSTH}	15	–	15	–	15	–	ns	

Notes:

- 1) t_{CHZ} and t_{CLHZ} are not referenced to a specific voltage level, but specify when the device output is no longer driving.
- 2) The parameters $t_{RC}(avg)$ and $t_{DSC}(avg)$ are the average over any 200 consecutive periods and $t_{RC}(avg)/t_{DSC}(avg)$ min are the smallest rates allowed, with the exception of a deviation due to t_{JIT} (per).
- 3) Input jitter is allowed provided it does not exceed values specified.
- 4) $t_{REH}(avg)$ and $t_{RP}(avg)$ are the average half clock period over any 200 consecutive clocks and is the smallest half period allowed, expect a deviation due to the allowed clock jitter. Input clock jitter is allowed provided it does not exceed values specified.
- 5) The period jitter t_{JIT} (per) is the maximum deviation in the t_{RC} or t_{DSC} period from the average or nominal t_{RC} or t_{DSC} period. It is allowed in either the positive or negative direction.
- 6) The cycle-to-cycle jitter t_{JITcc} is the amount the clock period can deviate from one cycle to the next.
- 7) The duty cycle jitter applies to either the high pulse or low pulse; however, the two cumulatively cannot exceed t_{JITper} . As long as the absolute minimum half period $t_{RP}(abs)$, $t_{REH}(abs)$, t_{DQSH} , or t_{DQSL} is not less than 43 percent of the average cycle.
- 8) All timing parameter values assume differential signaling for RE# and DQS is used.
- 9) When the device is operated with input clock jitter, t_{QSL} , t_{QSH} , and t_{QH} need to be derated by the actual t_{JITper} in the input clock. (output deratings are relative to the NAND input RE pulse that generated the DQS pulse).
- 10) The t_{DS} and t_{DH} times listed are based on an input slew rate greater than or equal to 1 V/ns for single-ended signal, and based on an input slew rate greater than or equal to 2 V/ns for differential signal. If the input slew rate is less than 1 V/ns for single-ended signal, or less than 2 V/ns for differential signal, then the derating methodology should be used.
- 11) When the device is operated with input RE (RE_t/RE_c) jitter, t_{QSL} , t_{QSH} , and t_{QH} need to be derated by the actual input duty cycle jitter beyond $0.45 \times t_{RC}(avg)$ but not exceeding $0.43 \times t_{RC}(avg)$. Output deratings are relative to the device input RE pulse that generated the DQS pulse.
- 12) The parameter t_{DIPW} is defined as the pulse width of the input signal between the first crossing of $V_{REFQ(DC)}$ and the consecutive crossing of $V_{REFQ(DC)}$.
- 13) t_{ADL} SPEC for SET FEATURES operations is 70ns.
- 14) t_{CR2} (MIN) is 150ns for Read ID sequence only. For all other command sequences t_{CR2} (MIN) requirement is 100ns.
- 15) t_{DQSRH} is only required if Matrix ODT is enabled.
- 16) Any command (including READ STATUS commands) cannot be issued during t_{WB} , even if R/B# or RDY is ready.
- 17) t_{CS2} should be applied when the device has any type of ODT enabled including ODT only enabled for data input.
- 18) Parameters t_{DQSQ} and t_{QH} are used to calculate overall t_{DVW} ($t_{DVW} = t_{QH} - t_{DQSQ}$). Since data eye training to optimize strobe placement is expected at high I/O speeds (≥ 533 MT/s), t_{DQSQ} and t_{QH} may borrow time from each other without changing t_{DVW} . For example, if there exists X ps of margin on t_{DQSQ} , then t_{QH} can be provided with an additional X ps without changing the value of t_{DVW} . When timing margin is borrowed from t_{DQSQ} to provide additional timing for t_{QH} , the same amount of timing margin can be used for additional timing for t_{QSL} or t_{QSH} .

4Tb TLC NAND Flash

UT81NDQ512G8T

Table 48: AC Characteristics: NV-DDR2/NV-DDR3 Command, Address, and Data for Timing Modes 8–9

Parameter	Symbol	Mode 8		Mode 9		Unit	Notes
		Min	Max	Min	Max		
Clock period		3.75		3		ns	
Frequency		≈266		≈333		MHz	
Command and Address							
Access window of DQ[7:0] from RE# LOW or RE_t/RE_c	t ^{AC}	3	25	3	25	ns	
ALE to data loading time	t ^{ADL}	150	–	150	–	ns	13
ALE to RE# LOW or RE_t/RE_c	t ^{AR}	10	–	10	–	ns	
DQ hold – command, address	t ^{CAH}	5	–	5	–	ns	
ALE, CLE hold	t ^{CALH}	5	–	5	–	ns	
ALE, CLE setup with ODT disabled	t ^{CALS}	15	–	15	–	ns	
ALE, CLE setup with ODT enabled	t ^{CALS2}	25	–	25	–	ns	
DQ setup – command, address	t ^{CAS}	5	–	5	–	ns	
CE# HIGH hold time	t ^{CEH}	20	–	20	–	ns	
Delay before CE# HIGH for any volume after a volume is selected	t ^{CEVDLY}	50	–	50	–	ns	
CE# hold	t ^{CH}	5	–	5	–	ns	
CE# HIGH to output High-Z	t ^{CHZ}	–	30	–	30	ns	1
CLE HIGH to output High-Z	t ^{CLHZ}	–	30	–	30	ns	1
CLE to RE# LOW or RE_t/RE_c	t ^{CLR}	10	–	10	–	ns	
CE# to RE# LOW or RE_t/RE_c	t ^{CR}	10	–	10	–	ns	
CE# to RE# LOW or RE_t/RE_c if CE# has been HIGH for >1μs	t ^{CR2}	100	–	100	–	ns	
	t ^{CR2 (Read ID)}	150	–	150	–	ns	14
CE# setup	t ^{CS}	20	–	20	–	ns	
CE# setup for data output with ODT disabled	t ^{CS1}	30	–	30	–	ns	
CE# setup for DQS/DQ[7:0] with ODT enabled	t ^{CS2}	40	–	40	–	ns	18
CE# setup time to DQS (DQS_t) low after CE# has been HIGH for>1μs	t ^{CD}	100	–	100	–	ns	
ALE, CLE, WE#, hold time from CE# HIGH	t ^{CSD}	10	–	10	–	ns	
ENi LOW until any issued command is ignored	t ^{ENi}	–	15	–	15	ns	
CE_# LOW until ENo LOW	t ^{ENo}	–	50	–	50	ns	
Ready to data output	t ^{RR}	20	–	20	–	ns	
WE# HIGH to R/B# LOW	t ^{WB}	–	100	–	100	ns	17
WE# cycle time	t ^{WC}	25	–	25	–	ns	
WE# pulse width	t ^{WH}	11	–	11	–	ns	

4Tb TLC NAND Flash

UT81NDQ512G8T

Parameter	Symbol	Mode 8		Mode 9		Unit	Notes
		Min	Max	Min	Max		
Command cycle to data output	t_{WHR}	80	–	80	–	ns	
WE# pulse width	t_{WP}	11	–	11	–	ns	
WP# transition to command cycle	t_{WW}	100	–	100	–	ns	
Delay before next command after a volume is selected	t_{VDLY}	50	–	50	–	ns	
Jitter							
The deviation of a given $t_{DQS(ABS)}$ / $t_{DSC(ABS)}$ from a $t_{DQS(AVG)}$ / $t_{DSC(AVG)}$	$t_{JITper(DQS)}$	-0.30	0.30	-0.24	0.24	ns	3,5,7
The deviation of a given $t_{RC(ABS)}$ / $t_{DSC(ABS)}$ from a $t_{RC(AVG)}$ / $t_{DSC(AVG)}$	$t_{JITper(RE\#)}$	-0.225	0.225	-0.18	0.18	ns	3,5,7
Cycle to cycle jitter for DQS	$t_{JITcc(DQS)}$	–	0.6	–	0.48	ns	3,6
Cycle to cycle jitter for RE#	$t_{JITcc(RE\#)}$	–	0.45	–	0.36	ns	3,6
Data Input							
DQS setup time for data input start	t_{CDQSS}	30	–	30	–	ns	
DQS hold time for data input burst end	t_{CDQSH}	100	–	100	–	ns	
DQS (DQS _t) HIGH and RE# (RE _t) HIGH setup to ALE, CLE and CE# LOW during data burst	t_{DBS}	5	–	5	–	ns	
Data In hold	t_{DH}	0.30	–	0.24	–	ns	10
Data In setup	t_{DS}	0.30	–	0.24	–	ns	10
DQ input pulse width	t_{DIPW}	0.31	–	0.31	–	$t_{DCS(AVG)}$	12
DQS input high pulse width	t_{DQSH}	0.43	–	0.43	–	$t_{DCS(AVG)}$	
DQS input low pulse width	t_{DQSL}	0.43	–	0.43	–	$t_{DCS(AVG)}$	
Average DQS cycle time	$t_{DCS(AVG)}$ or t_{DCS}	3.75	–	3	–	ns	2
Absolute DQS cycle time, from rising edge to rising edge	$t_{DCS(ABS)}$	$t_{DSC(ABS) MIN} = t_{DSC(AVG)} + t_{JITper(DQS) MIN}$ $t_{DSC(ABS) MAX} = t_{DSC(AVG)} + t_{JITper(DQS) MAX}$				ns	
ENi LOW until any issued command is ignored	t_{ENi}	–	15	–	15	ns	
CE# LOW until ENo LOW	t_{ENo}	–	50	–	50	ns	
DQS write preamble with ODT disabled	t_{WPRE}	15	–	15	–	ns	
DQS write preamble with ODT enabled	t_{WPRE2}	25	–	25	–	ns	
DQS write postamble	t_{WPST}	6.5	–	6.5	–	ns	
DQS write postamble hold time	t_{WPSTH}	25	–	25	–	ns	
Data Output							
Access window of DQ[7:0] from CLK	t_{AC}	3	25	3	25	ns	
DQS (DQS _t) HIGH and RE# (RE _t) HIGH setup to ALE, CLE, and CE# LOW during data burst	t_{DBS}	5	–	5	–	ns	

4Tb TLC NAND Flash

UT81NDQ512G8T

Parameter	Symbol	Mode 8		Mode 9		Unit	Notes
		Min	Max	Min	Max		
DQS-DQ skew	t^{DQSQ}	–	0.350	–	0.30	ns	
Access window of DQS from RE# or RE_t/RE_c	t^{DQSRE}	3	25	3	25	ns	
RE# LOW to DQS or DQ[7:0] driven	t^{DQSD}	6	18	6	18	ns	
DQS hold time after RE# LOW or RE_t/RE_c crosspoint	t^{DQSRH}	5	–	5	–	ns	15
Data valid window	t^{DVW}	$t^{\text{DVW}} = t^{\text{QH}} - t^{\text{DQSQ}}$				ns	
DQ-DQS hold, DQS to first DQ to go nonvalid, per access	t^{QH}	0.37	–	0.37	–	$t^{\text{RC}}(\text{avg})$	9,11
DQS (DQS_t/DQS_c) output HIGH time	t^{QSH}	0.37	–	0.37	–	$t^{\text{RC}}(\text{avg})$	9,11
DQS (DQS_t/DQS_c) output LOW time	t^{QSL}	0.37	–	0.37	–	$t^{\text{RC}}(\text{avg})$	9,11
Average RE# cycle time	$t^{\text{RC}}(\text{avg})$ or t^{RC}	3.75	–	3	–	ns	2
Absolute RE# cycle time	$t^{\text{RC}}(\text{abs})$	$t^{\text{RC}}(\text{abs}) \text{ MIN} = t^{\text{RC}}(\text{avg}) + t^{\text{JITper}}(\text{RE\#}) \text{ MIN}$ $t^{\text{RC}}(\text{abs}) \text{ MAX} = t^{\text{RC}}(\text{avg}) + t^{\text{JITper}}(\text{RE\#}) \text{ MAX}$				ns	
Average RE# HIGH hold time	$t^{\text{REH}}(\text{avg})$	0.45	0.55	0.45	0.55	$t^{\text{RC}}(\text{avg})$	4
Absolute RE# HIGH hold time	$t^{\text{REH}}(\text{abs})$	0.43	–	0.43	–	$t^{\text{RC}}(\text{avg})$	
Data output to command, address, or data input	t^{RHW}	100	–	100	–	ns	
Average RE# pulse width	$t^{\text{RP}}(\text{avg})$	0.45	0.55	0.45	0.55	$t^{\text{RC}}(\text{avg})$	4
Absolute RE# pulse width	$t^{\text{RP}}(\text{abs})$	0.43	–	0.43	–	$t^{\text{RC}}(\text{avg})$	
Read preamble with ODT disabled	t^{RPRE}	15	–	15	–	ns	
Read preamble with ODT enabled	t^{RPRE2}	25	–	25	–	ns	
Read postamble	t^{RPST}	$t^{\text{RPST}}(\text{MIN}) = t^{\text{DQSRE}} + 0.5 \times t^{\text{RC}}$ $t^{\text{RPST}}(\text{MAX}) = \text{–}$				ns	
Read postamble hold time	t^{RPSTH}	15	–	15	–	ns	

Notes:

- 1) t^{CHZ} and t^{CLHZ} are not referenced to a specific voltage level, but specify when the device output is no longer driving.
- 2) The parameters $t^{\text{RC}}(\text{avg})$ and $t^{\text{DSC}}(\text{avg})$ are the average over any 200 consecutive periods and $t^{\text{RC}}(\text{avg})/t^{\text{DSC}}(\text{avg})$ min are the smallest rates allowed, with the exception of a deviation due to $t^{\text{JIT}}(\text{per})$.
- 3) Input jitter is allowed provided it does not exceed values specified.
- 4) $t^{\text{REH}}(\text{avg})$ and $t^{\text{RP}}(\text{avg})$ are the average half clock period over any 200 consecutive clocks and is the smallest half period allowed, expect a deviation due to the allowed clock jitter. Input clock jitter is allowed provided it does not exceed values specified.
- 5) The period jitter $t^{\text{JIT}}(\text{per})$ is the maximum deviation in the t^{RC} or t^{DSC} period from the average or nominal t^{RC} or t^{DSC} period. It is allowed in either the positive or negative direction.
- 6) The cycle-to-cycle jitter t^{JITcc} is the amount the clock period can deviate from one cycle to the next.
- 7) The duty cycle jitter applies to either the high pulse or low pulse; however, the two cumulatively cannot exceed t^{JITper} . As long as the absolute minimum half period $t^{\text{RP}}(\text{abs})$, $t^{\text{REH}}(\text{abs})$, t^{DQSH} , or t^{DQSL} is not less than 43 percent of the average cycle.
- 8) All timing parameter values assume differential signaling for RE# and DQS is used.
- 9) When the device is operated with input clock jitter, t^{QSL} , t^{QSH} , and t^{QH} need to be derated by the actual t^{JITper} in the input clock. (output deratings are relative to the NAND input RE pulse that generated the DQS pulse).
- 10) The t^{DS} and t^{DH} times listed are based on an input slew rate greater than or equal to 1 V/ns for single-ended signal, and based on an input slew rate greater than or equal to 2 V/ns for differential signal. If the input slew rate is less than 1 V/ns for single-ended signal, or less than 2 V/ns for differential signal, then the derating methodology should be used.
- 11) When the device is operated with input RE (RE_t/RE_c) jitter, t^{QSL} , t^{QSH} , and t^{QH} need to be derated by the actual

UT81NDQ512G8T

input duty cycle jitter beyond $0.45 \times t_{RC(avg)}$ but not exceeding $0.43 \times t_{RC(avg)}$. Output deratings are relative to the device input RE pulse that generated the DQS pulse.

- 12) The parameter t_{DIPW} is defined as the pulse width of the input signal between the first crossing of $V_{REFQ(DC)}$ and the consecutive crossing of $V_{REFQ(DC)}$.
- 13) t_{ADL} SPEC for SET FEATURES operations is 70ns.
- 14) t_{CR2} (MIN) is 150ns for Read ID sequence only. For all other command sequences t_{CR2} (MIN) requirement is 100ns.
- 15) t_{DQSRH} is only required if Matrix ODT is enabled.
- 16) Parameters t_{DQSQ} and t_{QH} are used to calculate overall t_{DVW} ($t_{DVW} = t_{QH} - t_{DQSQ}$). Since data eye training to optimize strobe placement is expected at high I/O speeds (≥ 533 MT/s), t_{DQSQ} and t_{QH} may borrow time from each other without changing t_{DVW} . For example, if there exists X ps of margin on t_{DQSQ} , then t_{QH} can be provided with an additional X ps without changing the value of t_{DVW} . When timing margin is borrowed from t_{DQSQ} to provide additional timing for t_{QH} , the same amount of timing margin can be used for additional timing for t_{QSL} or t_{QSH} .
- 17) Any command (including READ STATUS commands) cannot be issued during t_{WB} , even if R/B# or RDY is ready.
- 18) t_{CS2} should be applied when the device has any type of ODT enabled including ODT only enabled for data input.

12.11 Array Characteristics

Table 49: TLC Array Characteristics

Parameter	Symbol	Typ	Max	Unit	Notes
ERASE BLOCK operation time	t_{BERS}	15	30	ms	10
ERASE SUSPEND operation time	t_{ESPD}	–	150	μs	13
ERASE RESUME to ERASE SUSPEND delay	t_{RSESPD}	–	–	ms	11
Busy time when ERASE SUSPEND is issued when LUN is already in the suspend state or ERASE RESUME is issued when no erase is suspended or ongoing	t_{ESPDN}	–	18	μs	
PROGRAM PAGE operation effective time (per page) without V_{PP}	t_{PROG_eff}	1900	–	μs	
PROGRAM PAGE operation time (per program command operation)	t_{PROG}	–	9500	μs	9
LAST PAGE PROGRAM operation time	t_{LPROG}	–	–	μs	4
Cache busy	t_{CBSY}	1400	9500	μs	9
Page Buffer Transfer Busy time	t_{PBSY}	12	14	μs	
PROGRAM SUSPEND operation time	t_{PSPD}	–	150	μs	
PROGRAM RESUME to PROGRAM SUSPEND delay	t_{RSPSPD}	–	–	μs	12
Busy time when PROGRAM SUSPEND is issued when LUN is already in suspend state or PROGRAM RESUME is issued when no program is suspended or ongoing	t_{PSPDN}	–	18	μs	
READ PAGE operation time without V_{PP}	t_R	88	150	μs	7,8
SNAP READ operation time without V_{PP}	t_{RSNAP}	51	100	μs	
Cache read busy time	t_{RCBSY}	11	150	μs	7,8

4Tb TLC NAND Flash

UT81NDQ512G8T

Parameter	Symbol	Typ	Max	Unit	Notes
Auto Read Calibration time	t_{RARC}	600	1122	μs	
Soft Data Busy Time	t_{SBSY}	4	15	μs	
Soft Data Read Time (One-Bit Soft Data/Two-Bits Soft Data)	t_{RSD}	340/485	625/875	μs	
Single Bit Soft Bit Read (SBSBR) Cache Read Busy Time	t_{RCBSY_SBSBR}	52	350	μs	
Single Bit Soft Bit Read (SBSBR) Time	t_{R_SBSBR}	185	350	μs	
Number of partial page programs	NOP	–	1	Cycles	1
Change column setup time to data in/out or next command for both single LUN and multi-LUN operations	t_{CCS}	–	–	ns	3
Dummy busy time	t_{DBSY}	0.5	1	μs	
Busy time for SET FEATURES and GET FEATURES operations	t_{FEAT}	–	1	μs	
Busy time for interface change	t_{ITC}	–	1	μs	2
Busy time for OTP DATA PROGRAM operation if OTP is protected	t_{OBSY}	–	100	μs	
Power-on reset time	t_{POR}	–	4	ms	
Device reset time (Read/Program/Erase)	t_{RST}	–	15/30/500	μs	5
Busy time for read operation from NAND status bit RDY going HIGH to NAND status bit ARDY going HIGH in completion of array read operation	t_{RTABSY}	10	12.5	μs	14
Full calibration time	t_{ZQCL}	1	–	μs	6
Short calibration time	t_{ZQCS}	0.3	–	μs	6

Notes:

- 1) The pages in the OTP Block have an NOP of 2.
- 2) t_{ITC} (MAX) is the busy time when the interface changes from Asynchronous to NV-DDR2 using the SET FEATURES (EFh) or SET FEATURES by LUN (D5h) command or NV-DDR2 to asynchronous using the RESET (FFh) command. During the t_{ITC} time, any command, including READ STATUS (70h) and READ STATUS ENHANCED (78h), is prohibited.
- 3) t_{CCS} (MIN) = 400ns
- 4) t_{LPROG} = t_{PROG} (last page) + t_{PROG} (last page - 1) - command load time (last page) - address load time (last page) - data load time (last page). t_{LPROG} only applies to SLC pages and Lower Pages without shared UP/XP programmed
- 5) If RESET command is issued at any other time other than Read/Program/Erase array busy times, the target goes busy for a maximum of 8 μs . If RESET command is issued during t_{PBSY} time, t_{RST} may be up to 13 μs . If RESET command is issued during t_{FEAT} time during a Temperature Sensor Readout (FA=E7h), then t_{RST} may be up to 150 μs .
- 6) Increased time beyond TYP may result when greater than 8 LUNs share a ZQ resistor.
- 7) Read performance numbers are with Flag Check trim = 0 (flags not read). MAX spec is the worst t_R and t_{RCBSY} time when reading a page with all shared pages programmed. If all shared pages are not programmed, t_R and t_{RCBSY} MAX

4Tb TLC NAND Flash

UT81NDQ512G8T

will be higher.

- 8) For Read Retry options 8 to 15, 'R and 'RCBSY MAX may be up to 480μs
- 9) In the case of a program operation that exceeds 'PROG/'CBSY MAX, that specific NAND block may be retired by the host system.
- 10) In the case of an erase operation that exceeds 'BERS MAX, that specific NAND block may be retired by the host system. 'BERS TYP value represents approximately 30% of specified endurance life.
- 11) 'RSESPD (MIN) = 4ms; If the delay from the ERASE RESUME (D2h) to the subsequent ERASE SUSPEND (61h) command is less than the minimum value of 'RSESPD there may not be forward progress in the suspended Erase operation.
- 12) 'RSPSPD (MIN) = 325μs; If the delay from the PROGRAM RESUME (13h) to the subsequent PROGRAM SUSPEND (84h) command is less than the minimum value of 'RSPSPD there may not be forward progress in the suspended Program operation.
- 13) When in the quad plane Erase case, 'ESPD may be up to 165us
- 14) 'RTABSY applies to all array Read operations. In Cache Read based operations 'RTABSY still applies before the next array Cache Read operation begins.'

Any parameters not referenced in Table 50 should be referenced in Table 49.

Table 50: SLC Array Characteristics

Parameter	Symbol	Typ	Max	Unit	Notes
ERASE BLOCK operation time	'BERS	15	30	ms	4
ERASE SUSPEND operation time	'ESPD	–	150	μs	9
ERASE RESUME to ERASE SUSPEND delay	'RSESPD	–	–	ms	5
Busy time when ERASE SUSPEND is issued when LUN is already in the suspend state or ERASE RESUME is issued when no erase is suspended or ongoing	'ESPDN	–	18	μs	
PROGRAM PAGE operation time without V _{PP}	'PROG	226	750	μs	3
LAST PAGE PROGRAM operation time	'LPROG	–	–	μs	1
Cache busy	'CBSY	31	700	μs	3
PROGRAM SUSPEND operation time	'PSPD	–	150	μs	
PROGRAM RESUME to PROGRAM SUSPEND delay	'RSPSPD	–	–	μs	6
Busy time when PROGRAM SUSPEND is issued when LUN is already in suspend state or PROGRAM RESUME is issued when no program is suspended or ongoing	'PSPDN	–	18	μs	
READ PAGE operation time without V _{PP}	'R	57	60	μs	2,11
SNAP READ operation time	'RSNAP	27	37	μs	
Cache read busy time	'RCBSY	11	60	μs	2,8,11
Number of partial page programs	NOP	–	2	Cycles	7
Busy time for read operation from NAND status bit RDY going HIGH to NAND status bit ARDY going HIGH in completion of array read operation	'RTABSY	10	12.5	μs	10

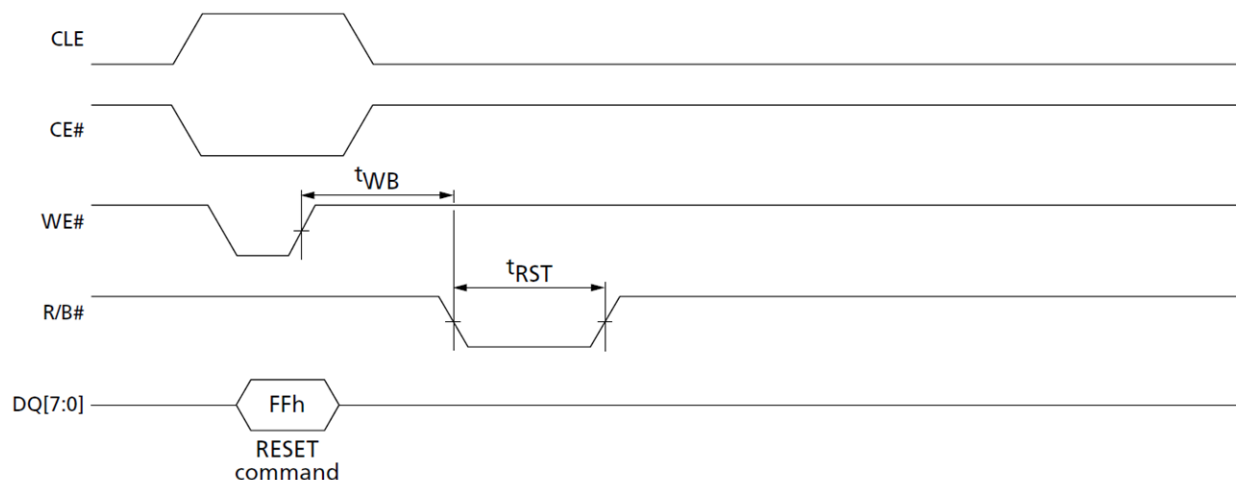
Notes:

UT81NDQ512G8T

- 1) $t_{LPROG} = t_{PROG}(\text{last page}) + t_{PROG}(\text{last page} - 1) - \text{command load time}(\text{last page}) - \text{address load time}(\text{last page}) - \text{data load time}(\text{last page})$.
- 2) For Read Retry options 8 to 15, t_R and t_{RCBSY} MAX may be up to 180 μ s
- 3) In the case of a program operation that exceeds t_{PROG}/t_{CBSY} MAX, that specific NAND block may be retired by the host system.
- 4) In the case of an erase operation that exceeds t_{BERS} MAX, that specific NAND block may be retired by the host system. t_{BERS} TYP value represents approximately 30% of specified endurance life.
- 5) $t_{RSESPD}(\text{MIN}) = 4\text{ms}$; If the delay from the ERASE RESUME (D2h) to the subsequent ERASE SUSPEND (61h) command is less than the minimum value of t_{RSESPD} there may not be forward progress in the suspended Erase operation.
- 6) $t_{RSPSPD}(\text{MIN}) = 325\mu\text{s}$; If the delay from the PROGRAM RESUME (13h) to the subsequent PROGRAM SUSPEND (84h) command is less than the minimum value of t_{RSPSPD} there may not be forward progress in the suspended Program operation.
- 7) The pages in the OTP Block have an NOP of 2.
- 8) If the next READ PAGE CACHE (31h, 00h-31h) or READ PAGE (00h-30h) command is issued when the device is still busy with the cache operation ($RDY = 1$, $ARDY = 0$), the next t_{RCBSY} time may be up to $t_{RCBSY}(\text{MAX}) + t_{RCBSY}(\text{TYP})$.
- 9) When in the quad plane Erase case, t_{ESPD} may be up to 165 μ s
- 10) t_{RTABSY} applies to all array Read operations. In Cache Read based operations t_{RTABSY} still applies before the next array Cache Read operation begins.
- 11) If a multi-plane read is issued that includes a factory bad block or out of bound block, the maximum t_R and t_{RCBSY} will be 62 μ s.

12.12 Asynchronous Interface Timing

Table 51: RESET Operation



4Tb TLC NAND Flash

UT81NDQ512G8T

Table 52: RESET LUN Operation

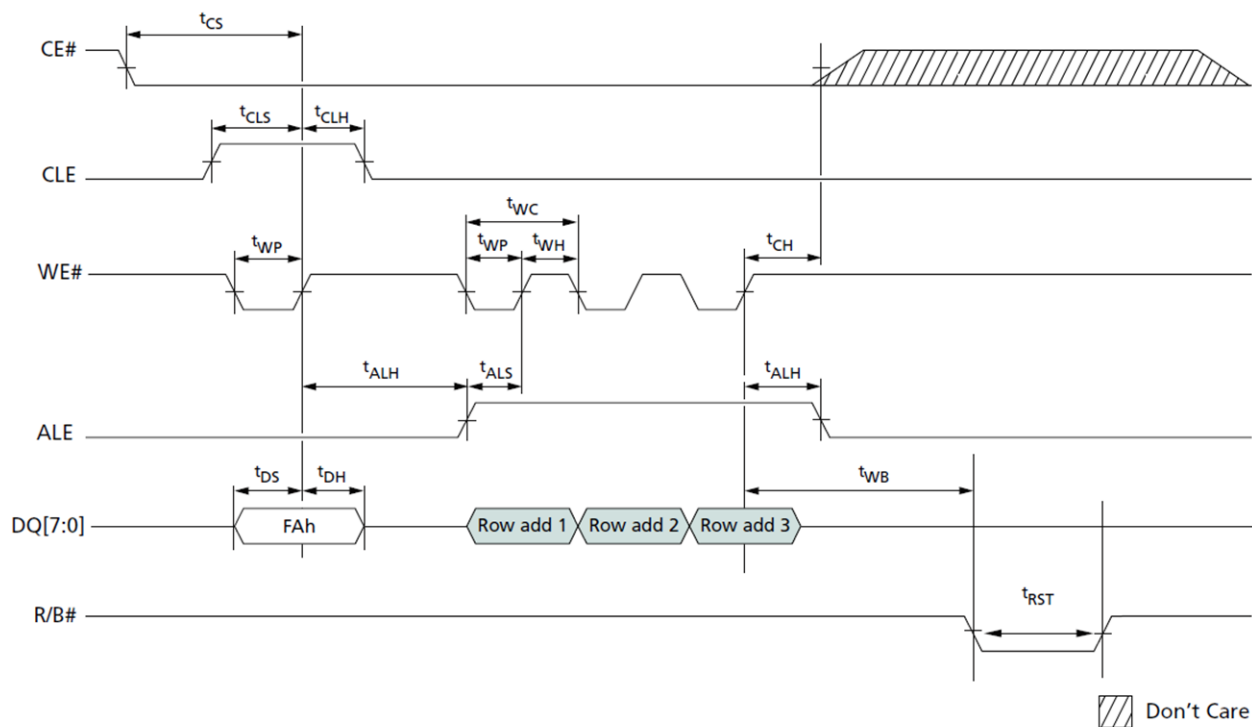
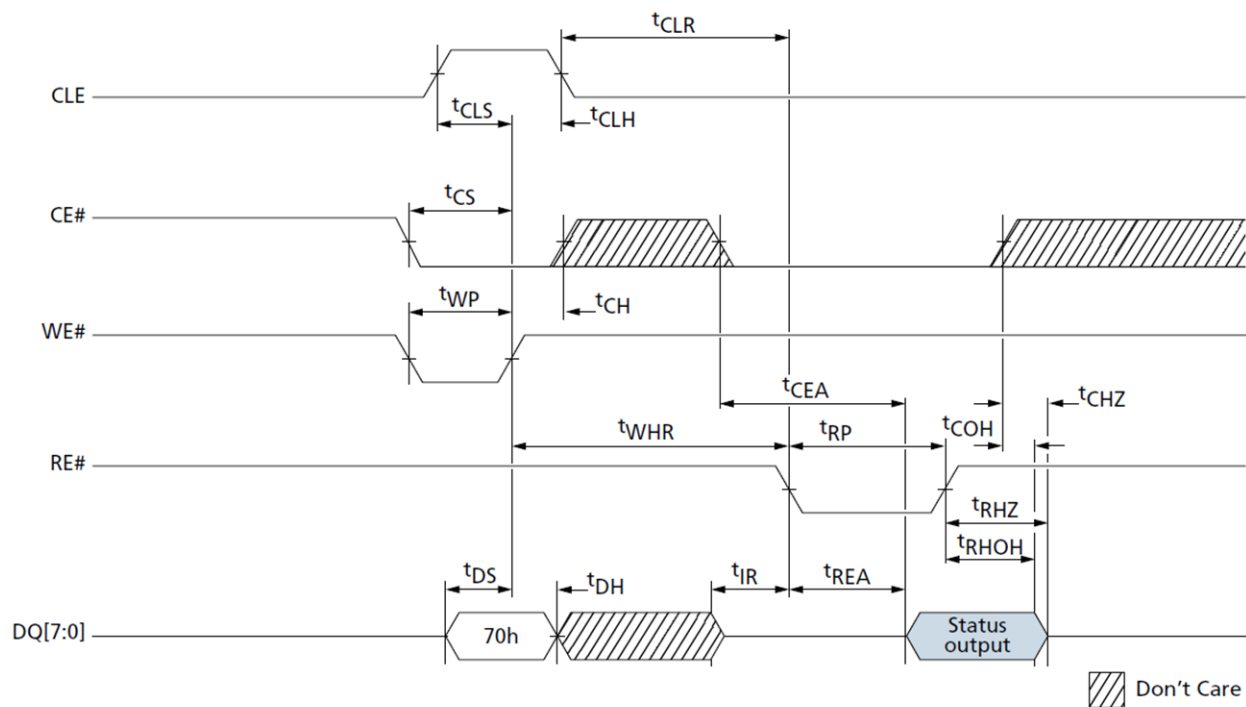


Table 53: READ STATUS Cycle



4Tb TLC NAND Flash

UT81NDQ512G8T

Table 54: READ STATUS ENHANCED Cycle

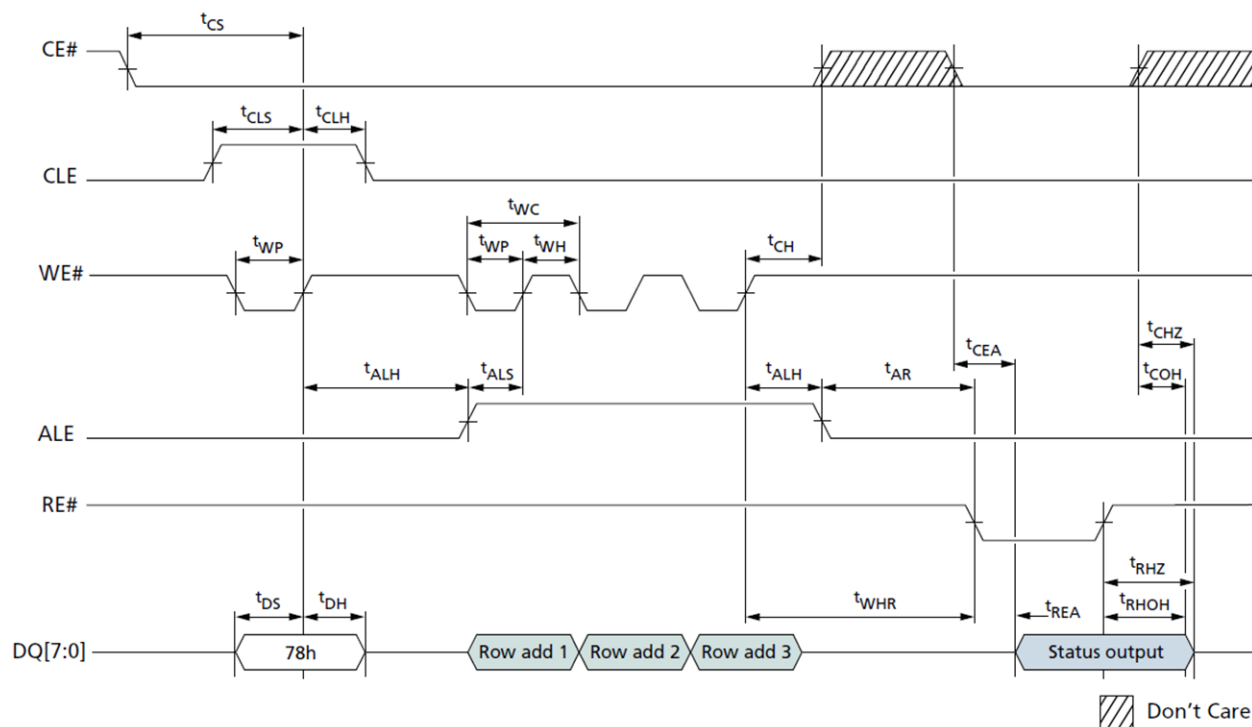
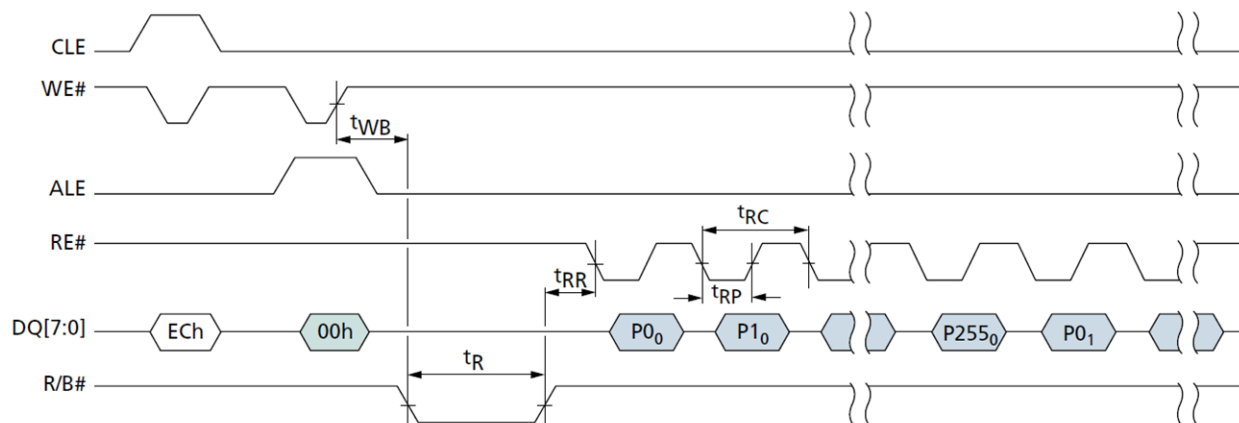


Table 55: READ PARAMETER PAGE



4Tb TLC NAND Flash

UT81NDQ512G8T

Table 56: READ PAGE

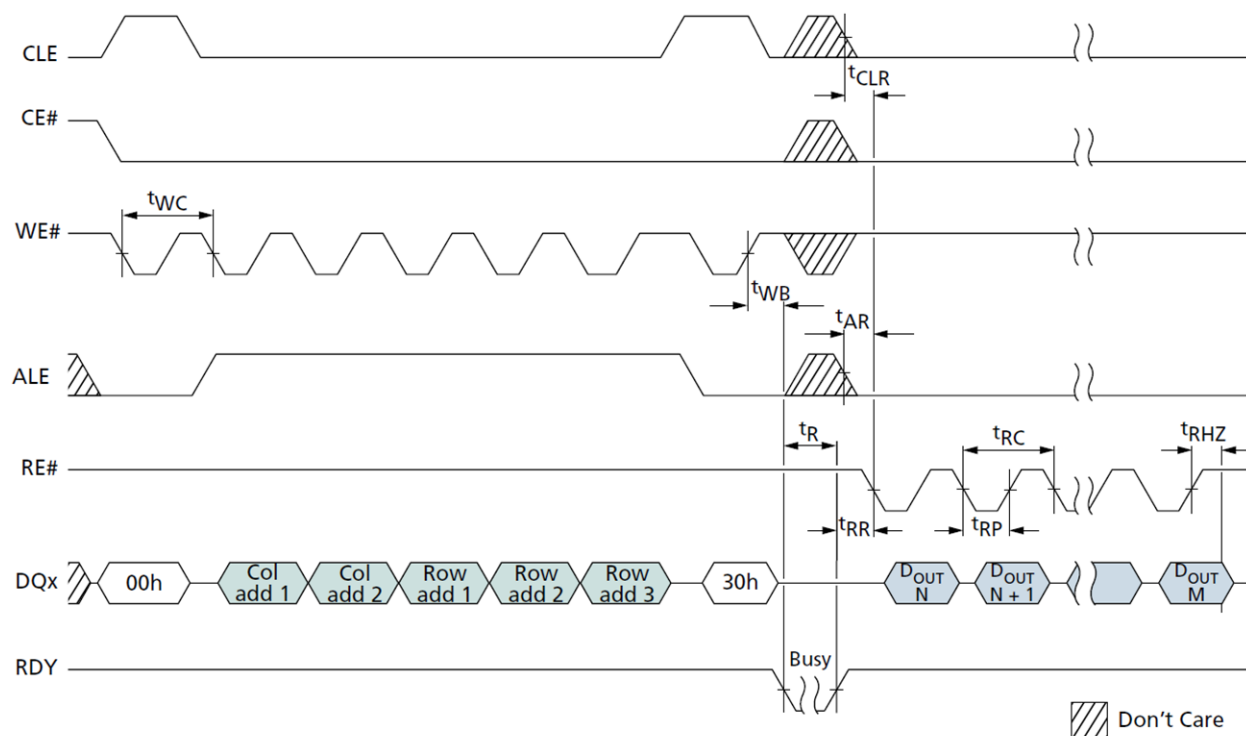
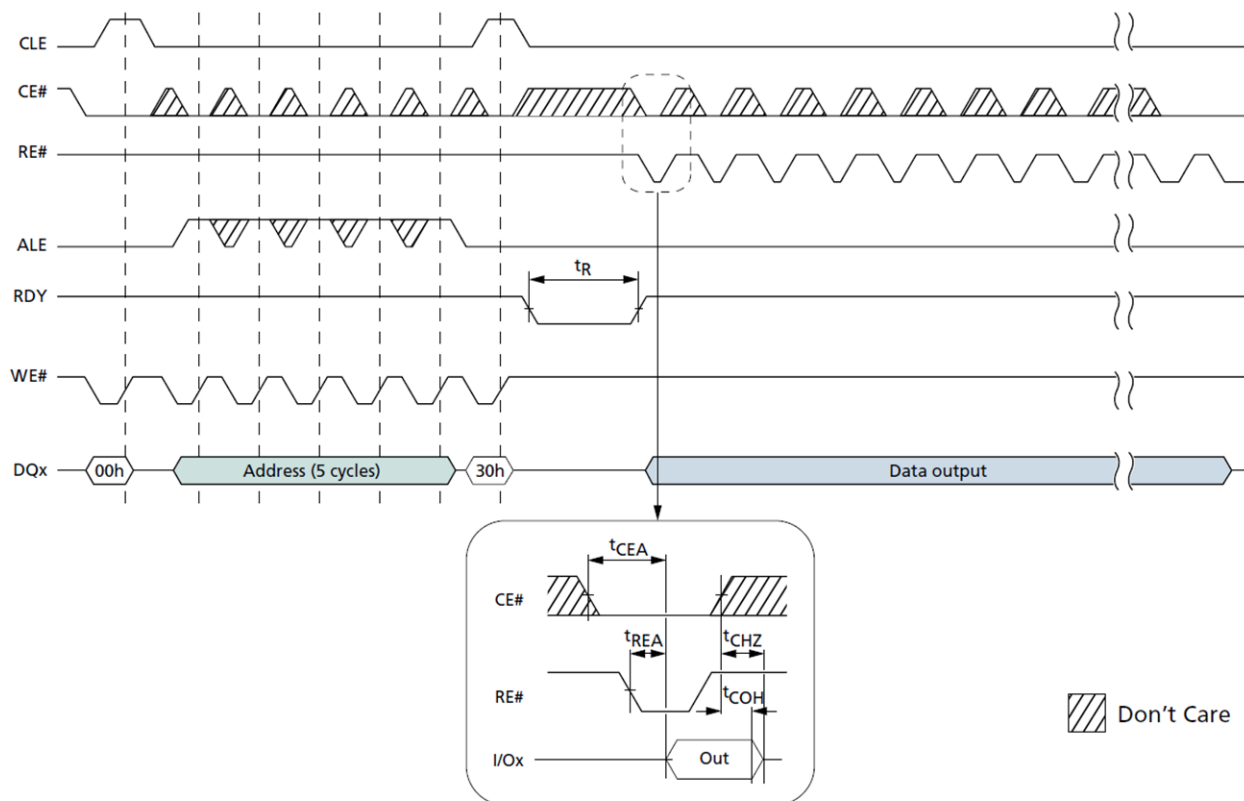


Table 57: READ PAGE Operation With CE# "Don't Care"



UT81NDQ512G8T

Table 58: CHANGE READ COLUMN

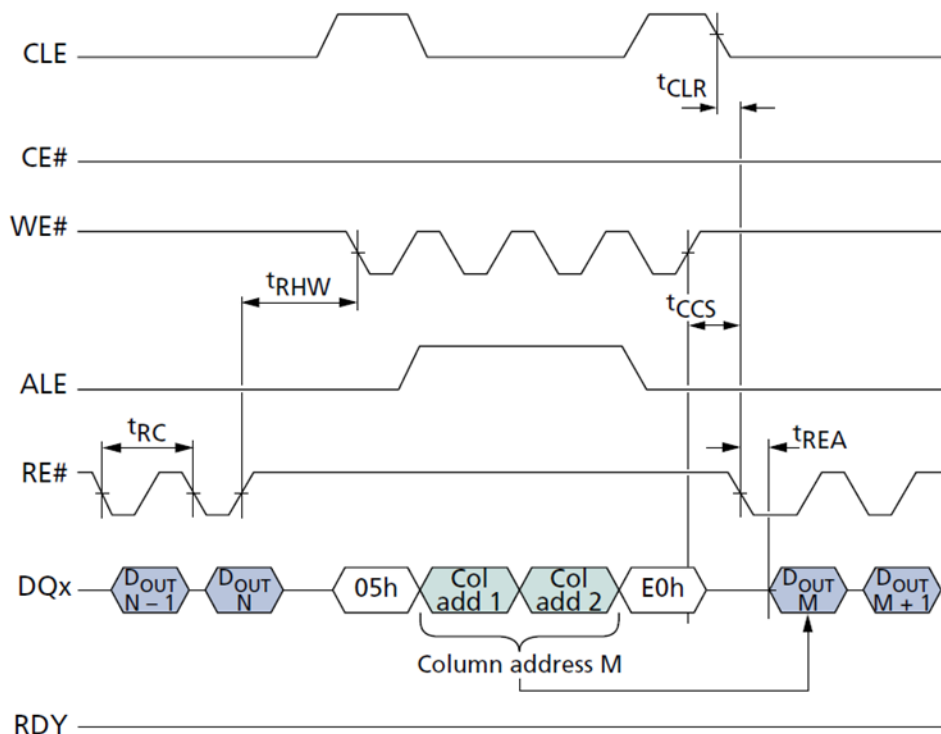
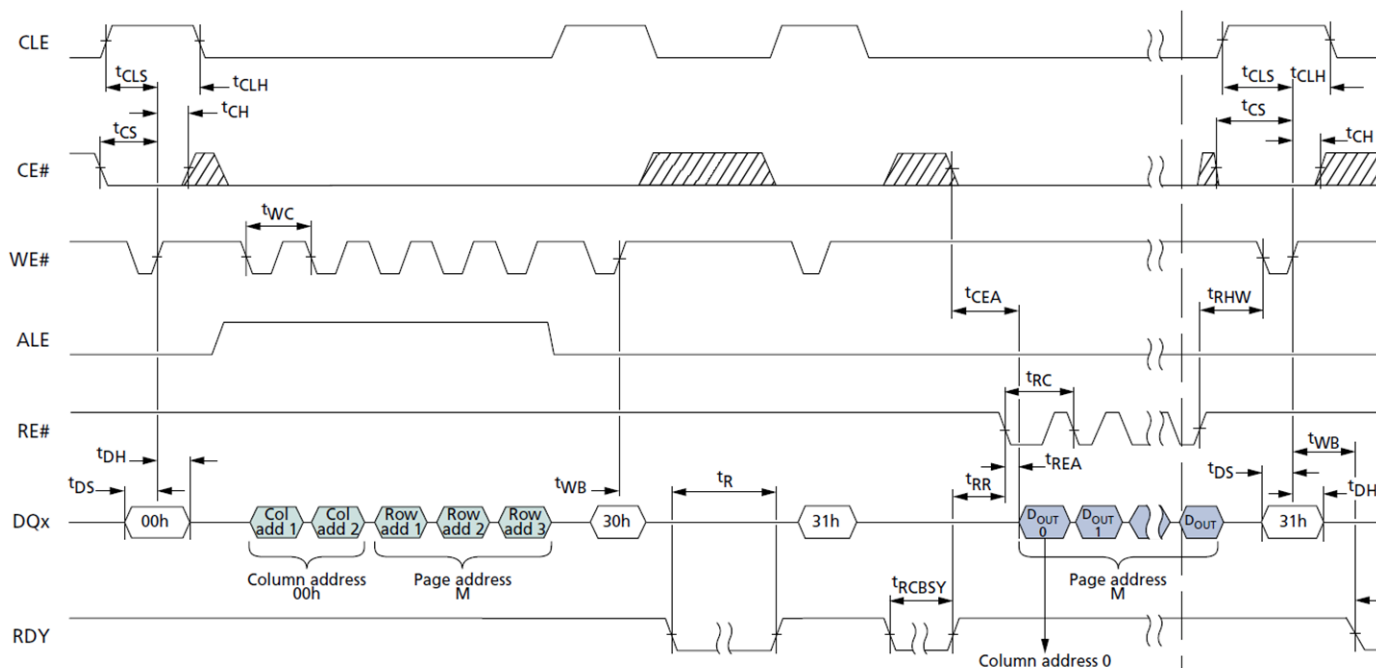


Table 59: READ PAGE CACHE SEQUENTIAL



4Tb TLC NAND Flash

UT81NDQ512G8T

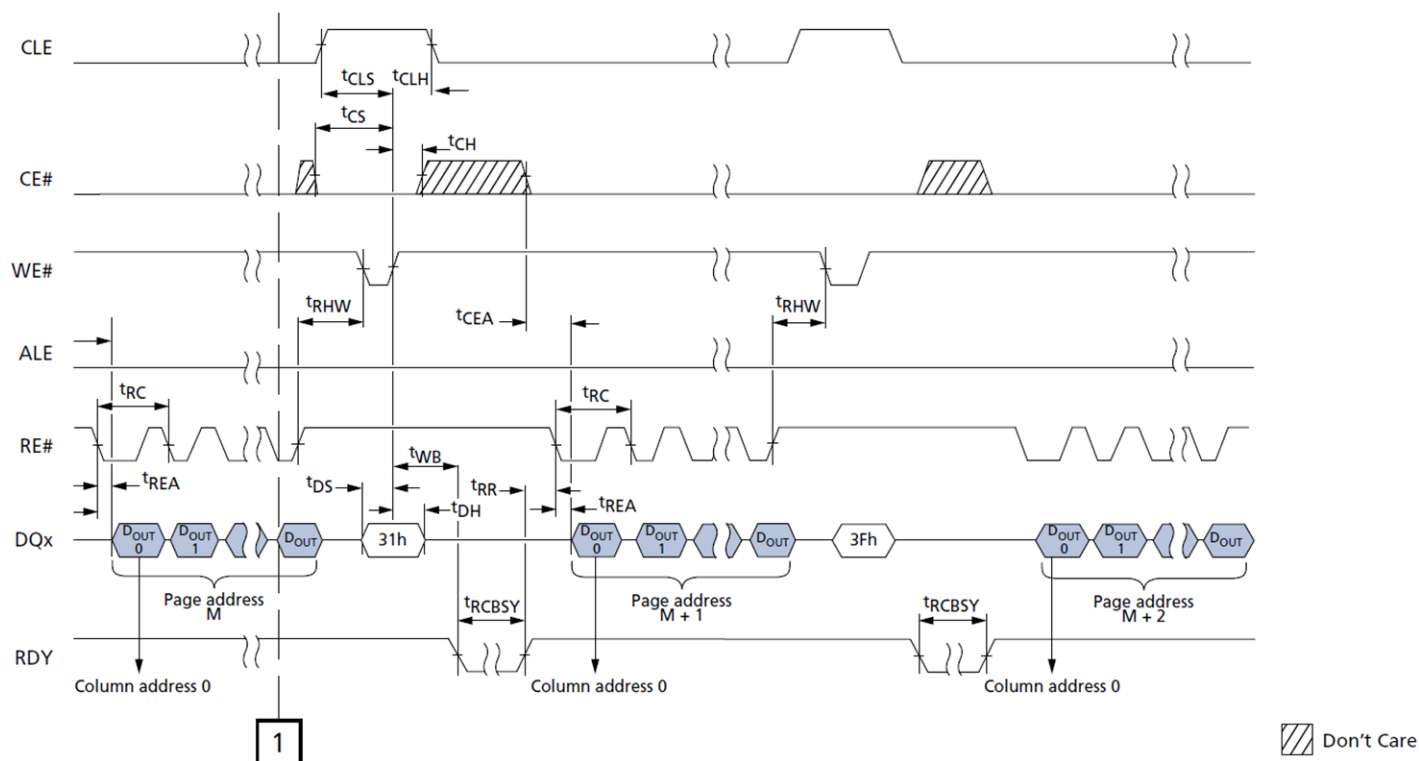
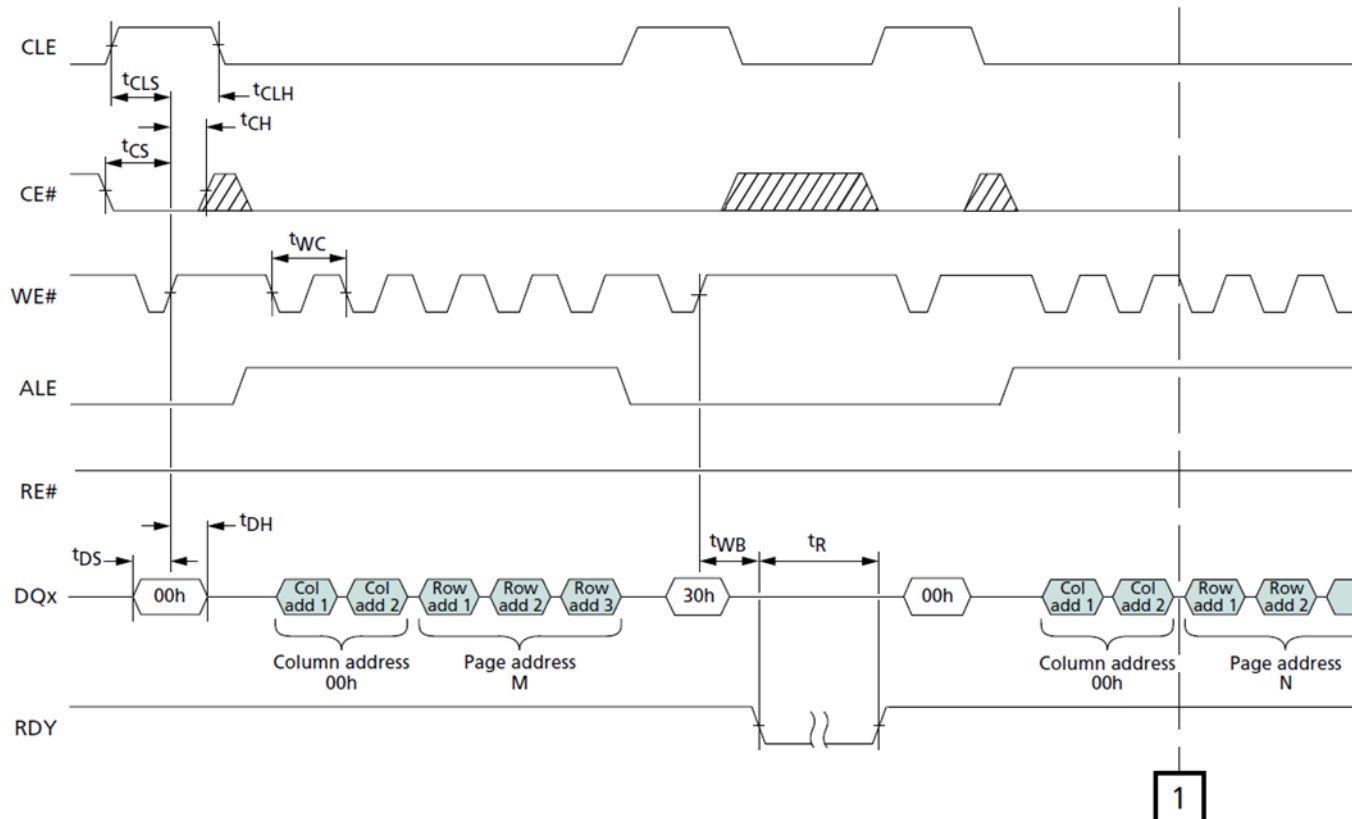


Table 60: READ PAGE CACHE RANDOM



4Tb TLC NAND Flash

UT81NDQ512G8T

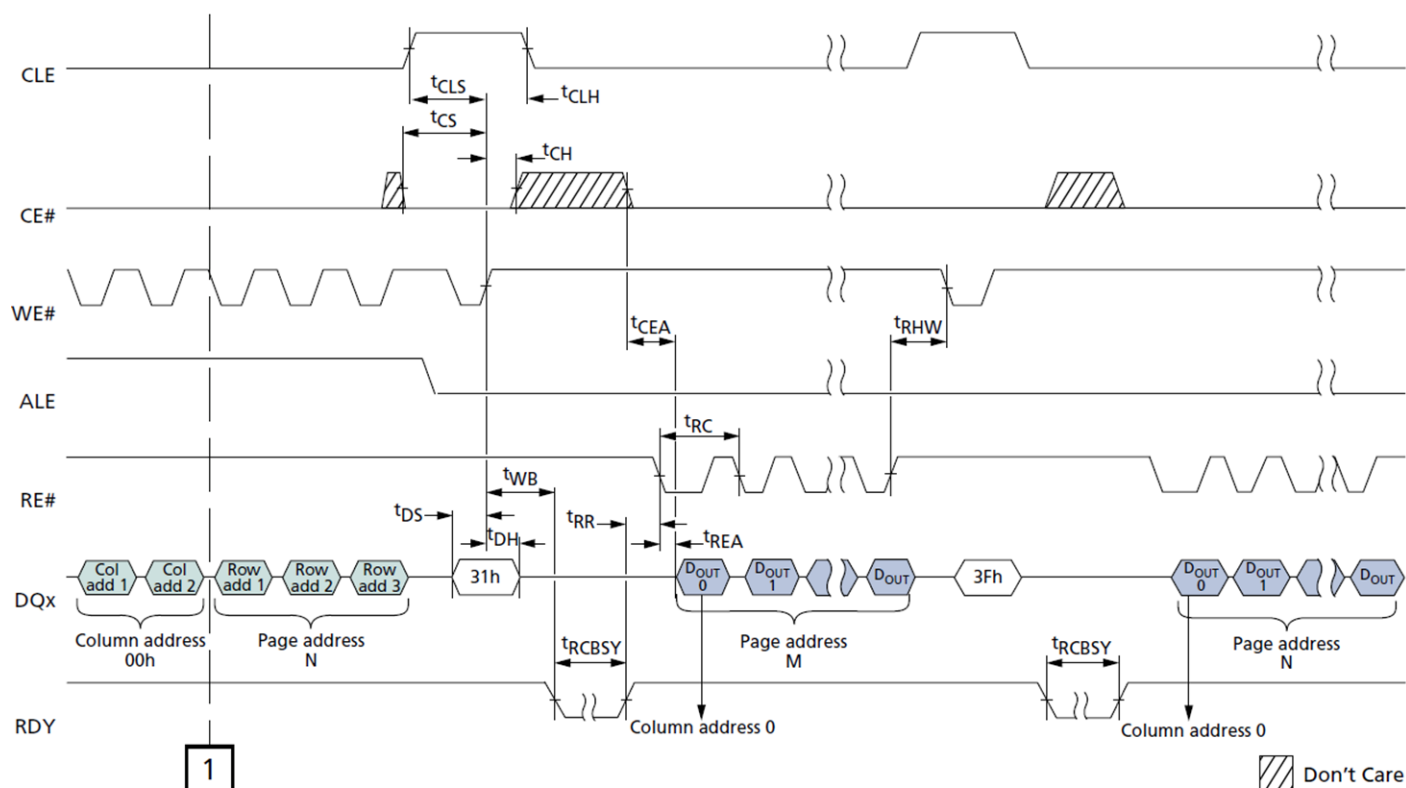
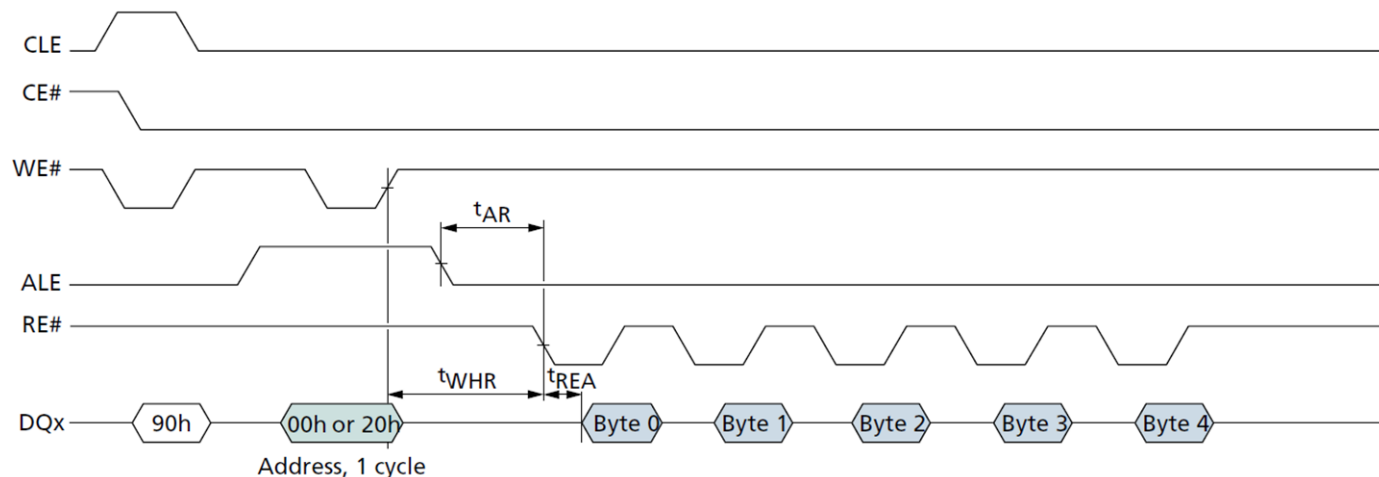


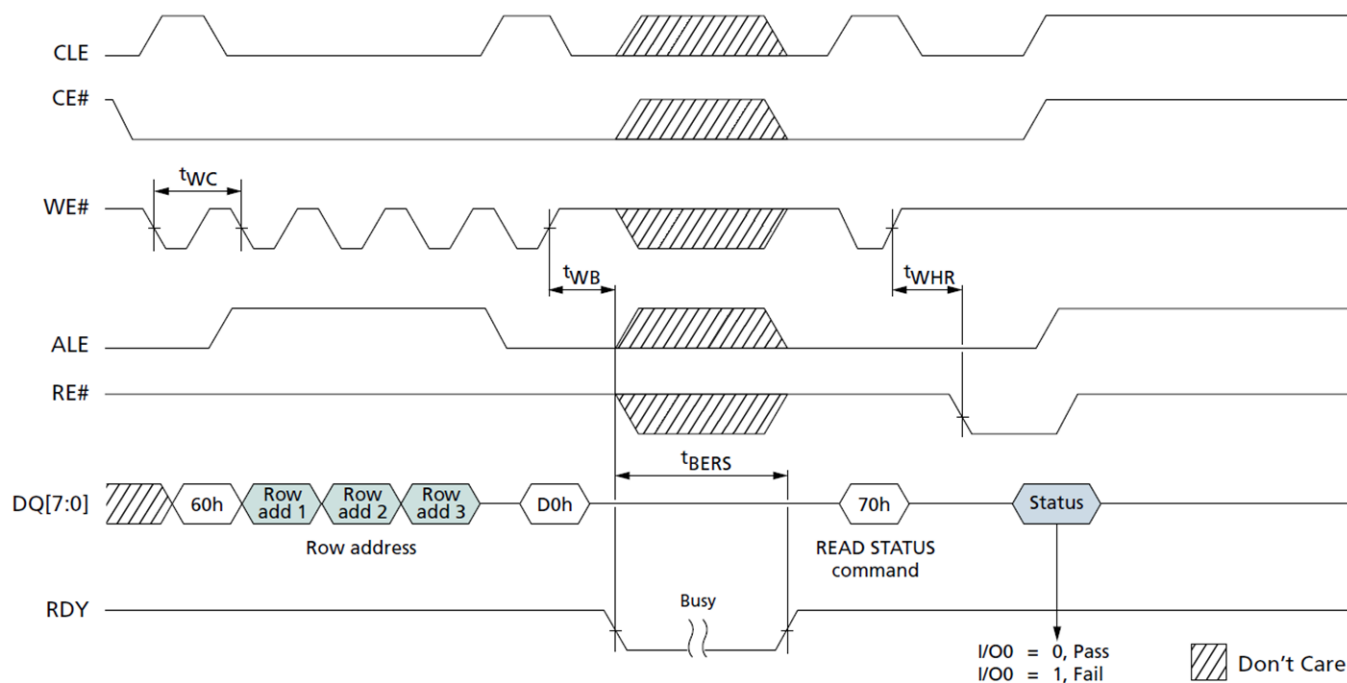
Table 61: Read ID Operation



4Tb TLC NAND Flash

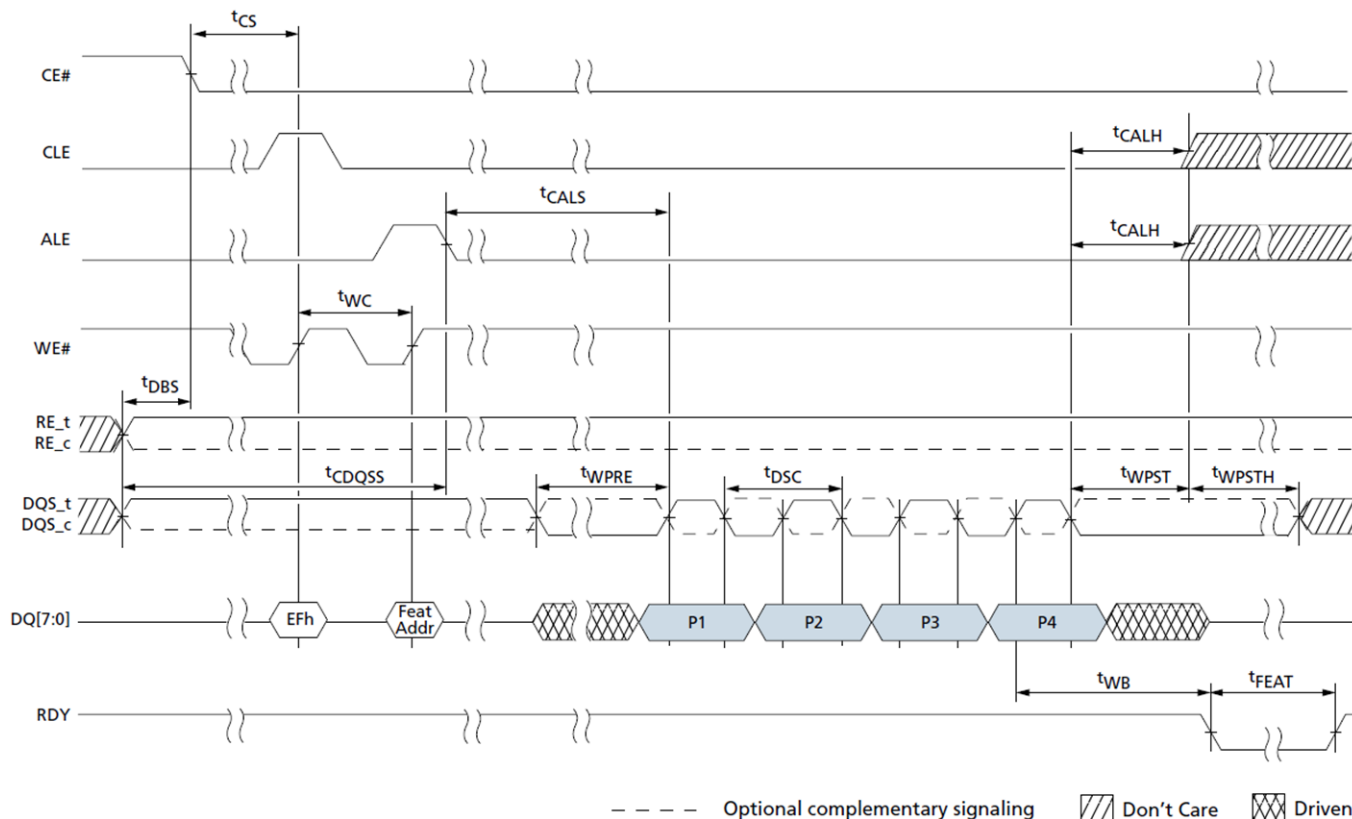
UT81NDQ512G8T

Table 62: ERASE BLOCK Operation



12.13 NV-DDR2, NV-DDR3 Interface Timing

Table 63: SET FEATURES Operation

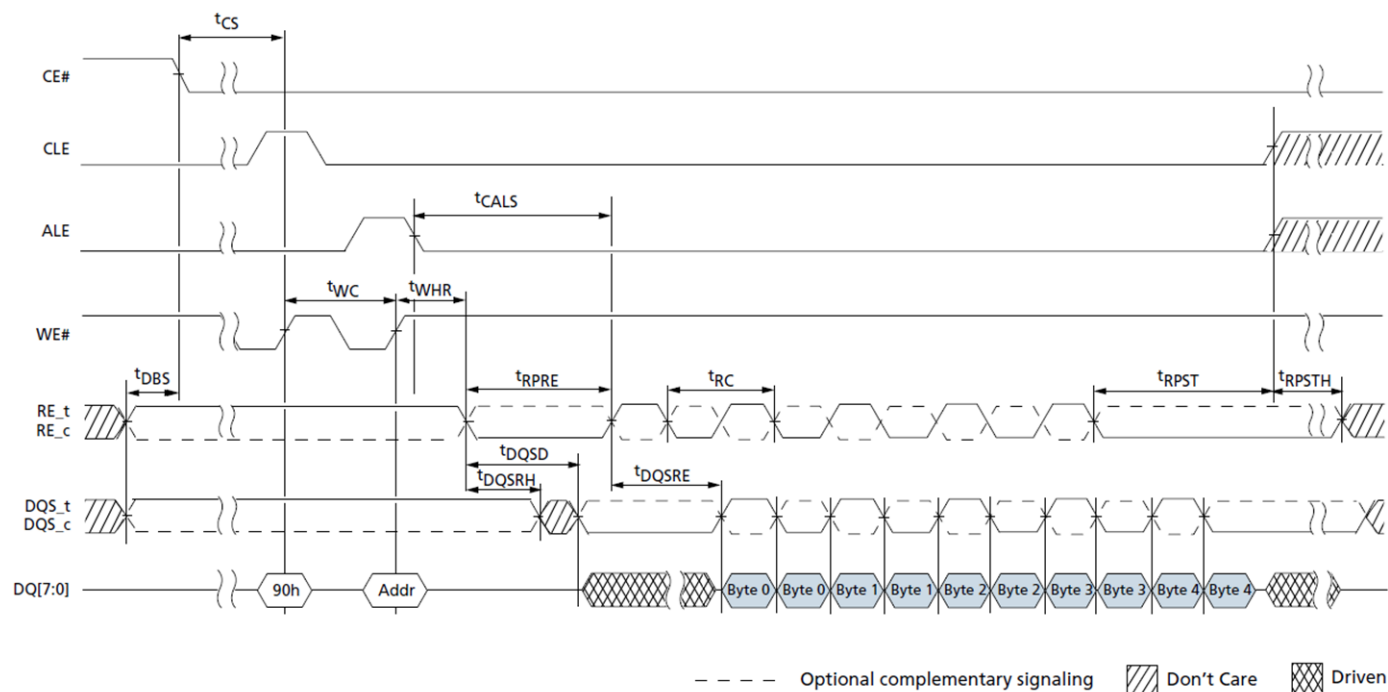


Note: DQS is Don't Care during ACTIVE command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.

4Tb TLC NAND Flash

UT81NDQ512G8T

Table 64: READ ID Operation

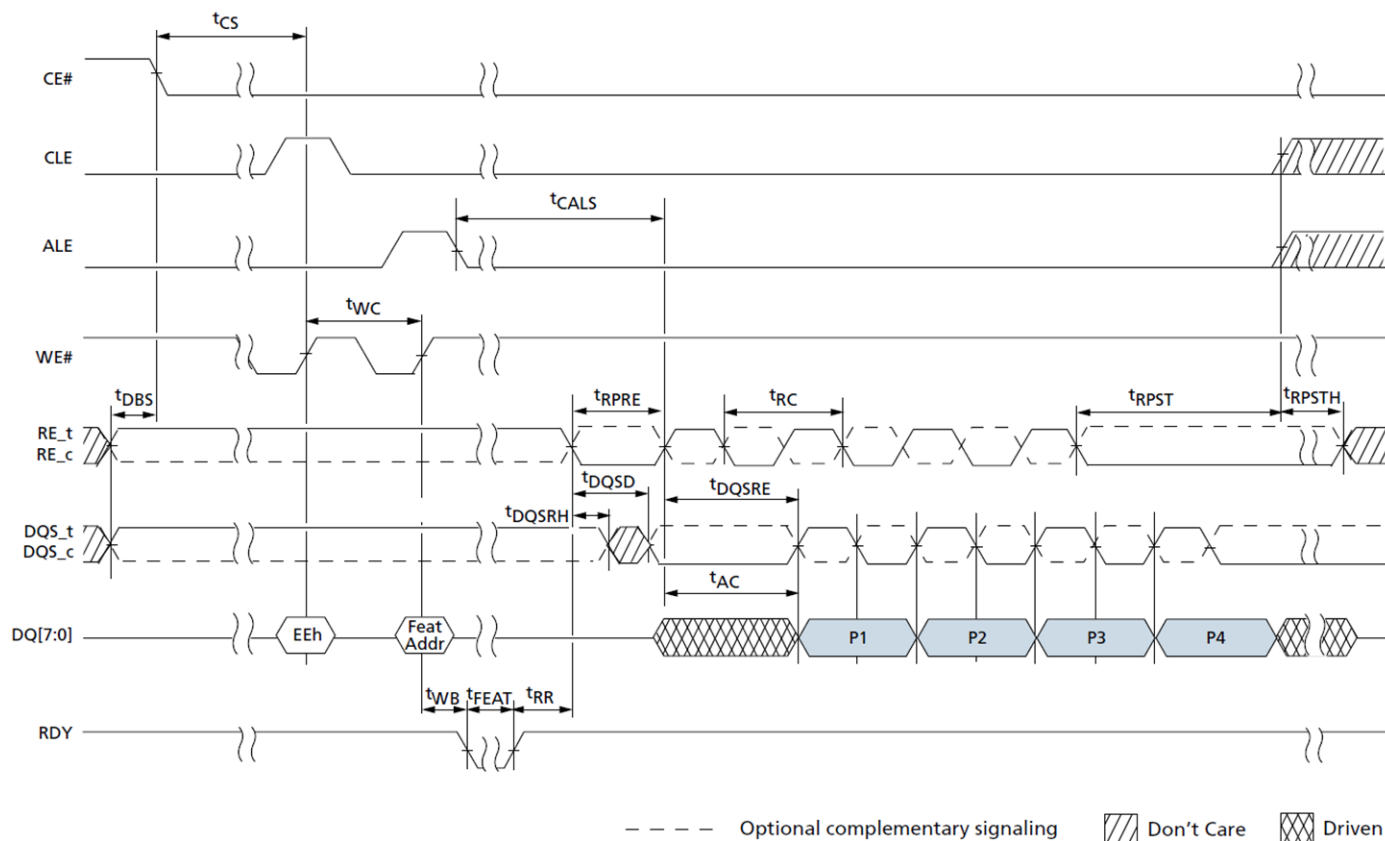


Note: DQS is Don't Care during ACTIVE command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.

4Tb TLC NAND Flash

UT81NDQ512G8T

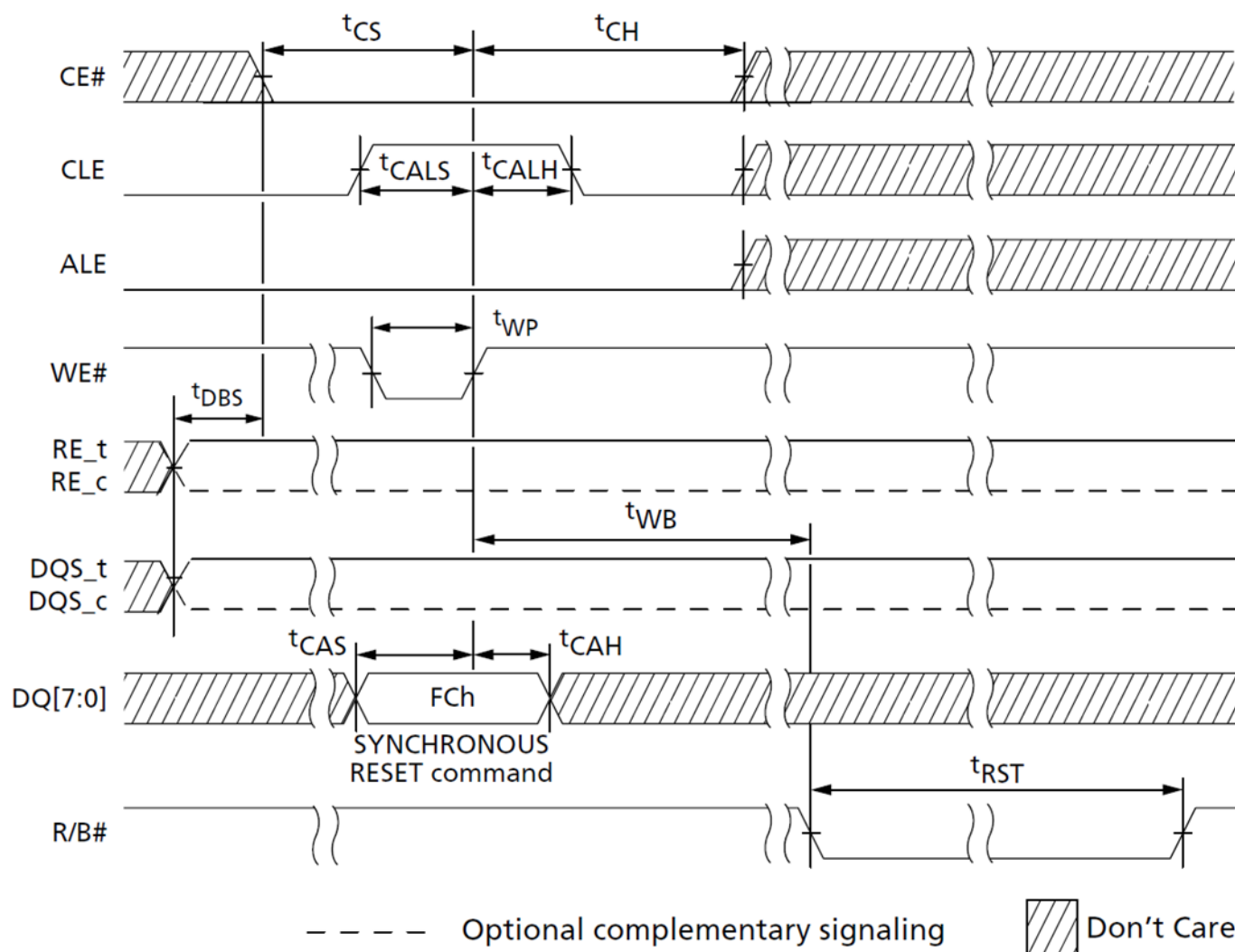
Table 65: GET FEATURES Operation



Note: DQS is Don't Care during ACTIVE command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.

UT81NDQ512G8T

Table 66: RESET (FCh) Operation

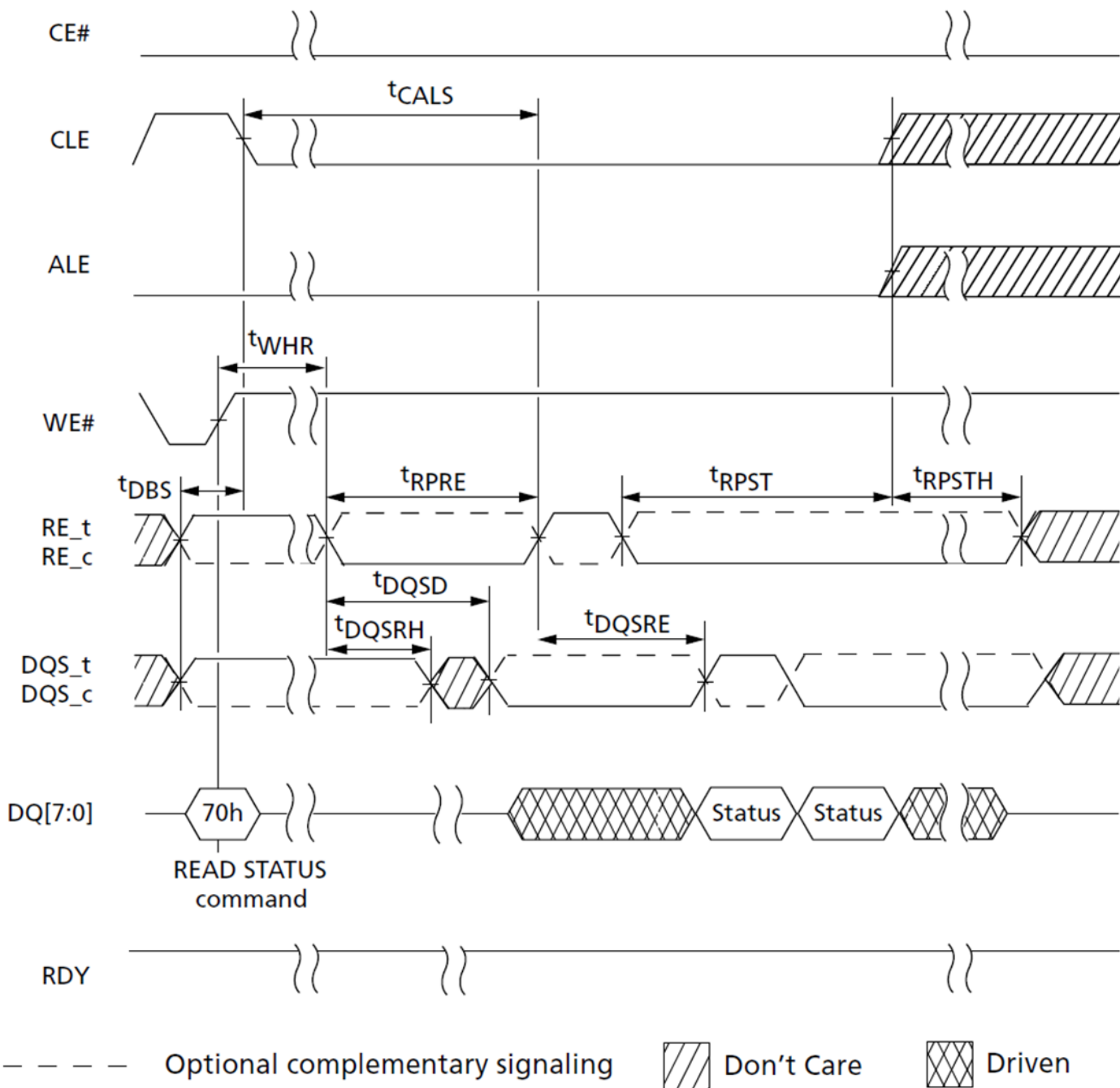


Note: DQS is Don't Care during ACTIVE command cycle (CLE is high). When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.

4Tb TLC NAND Flash

UT81NDQ512G8T

Table 67: READ STATUS Cycle

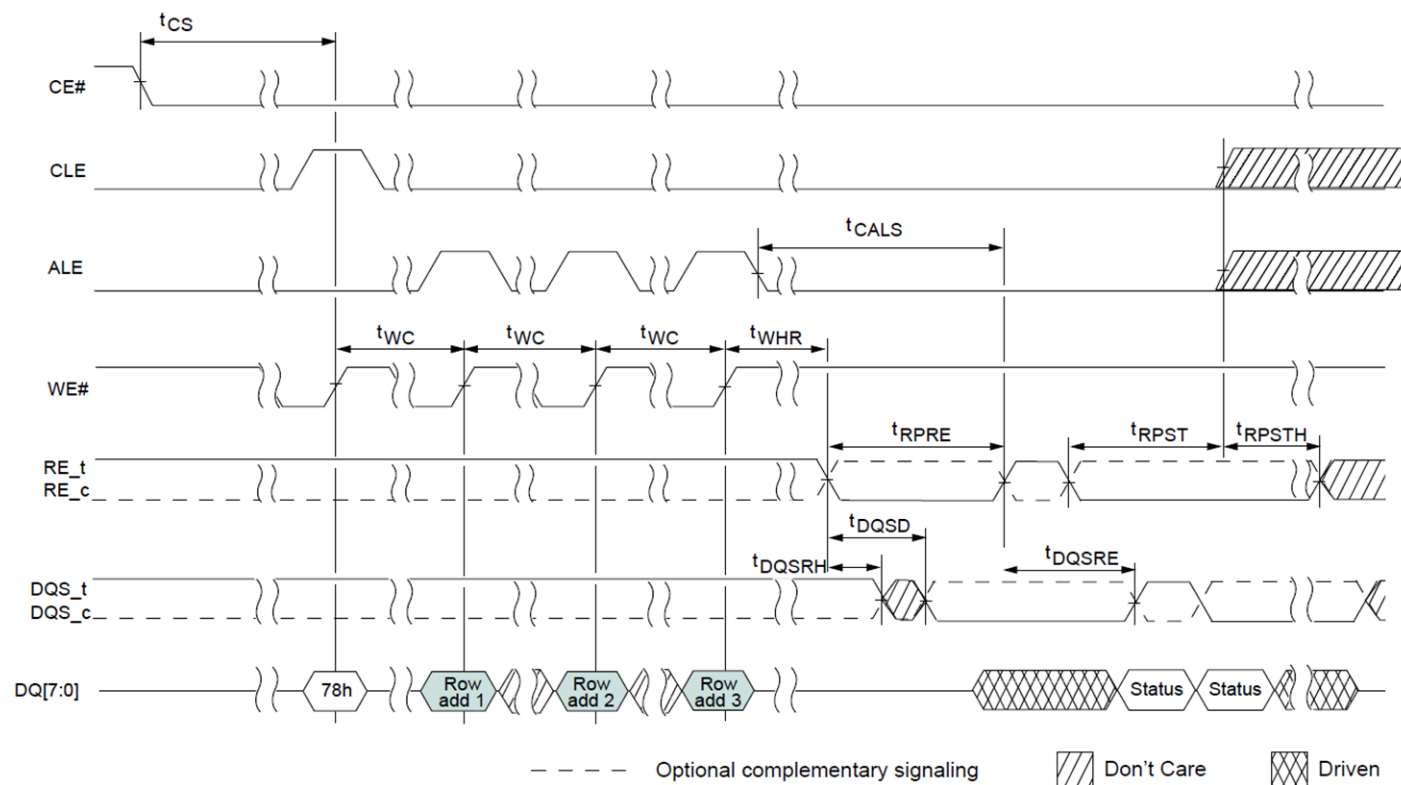


Note: DQS is Don't Care during ACTIVE command cycle (CLE is high). When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.

4Tb TLC NAND Flash

UT81NDQ512G8T

Table 68: READ STATUS ENHANCED Operation

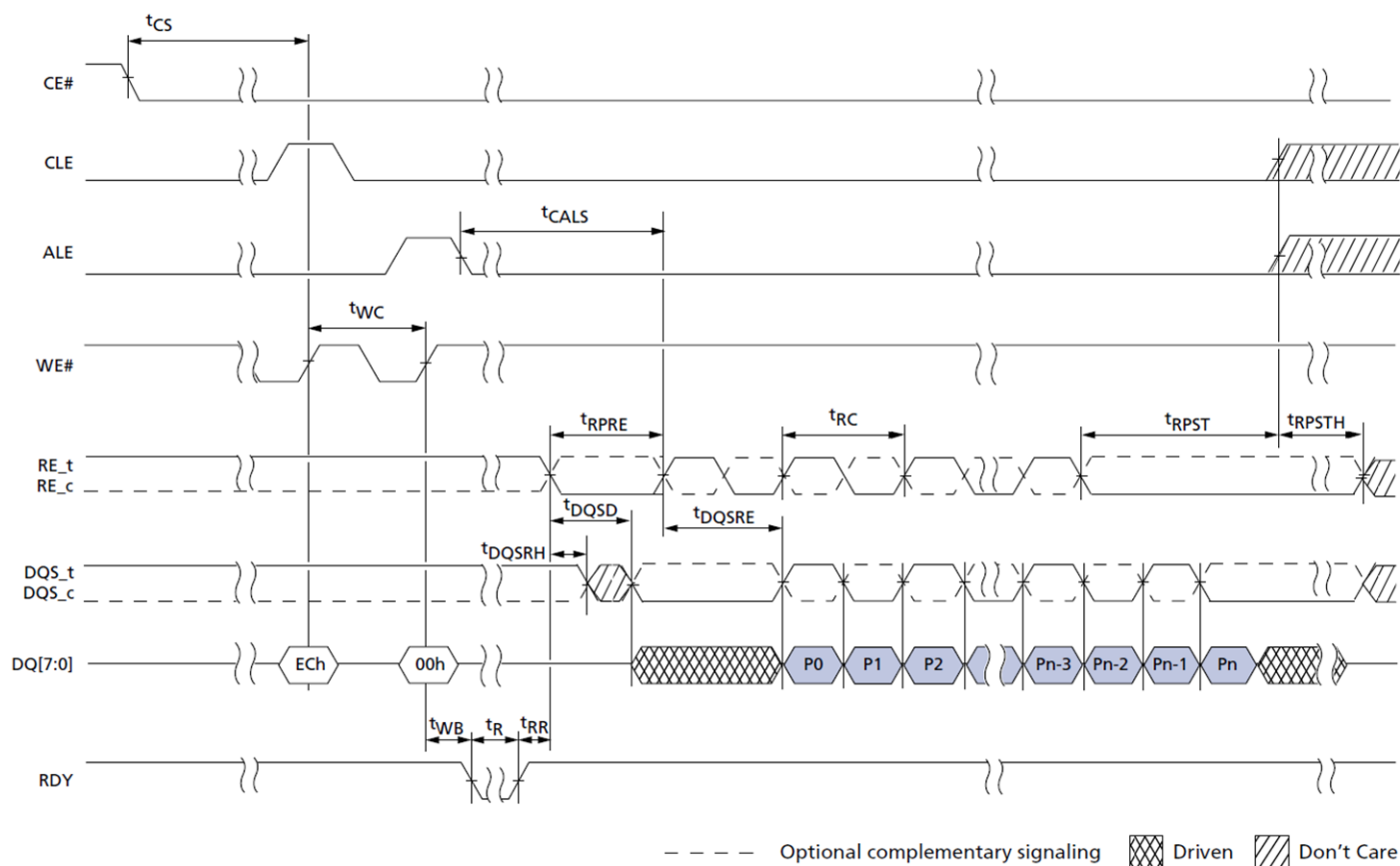


Note: DQS is Don't Care during ACTIVE command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.

4Tb TLC NAND Flash

UT81NDQ512G8T

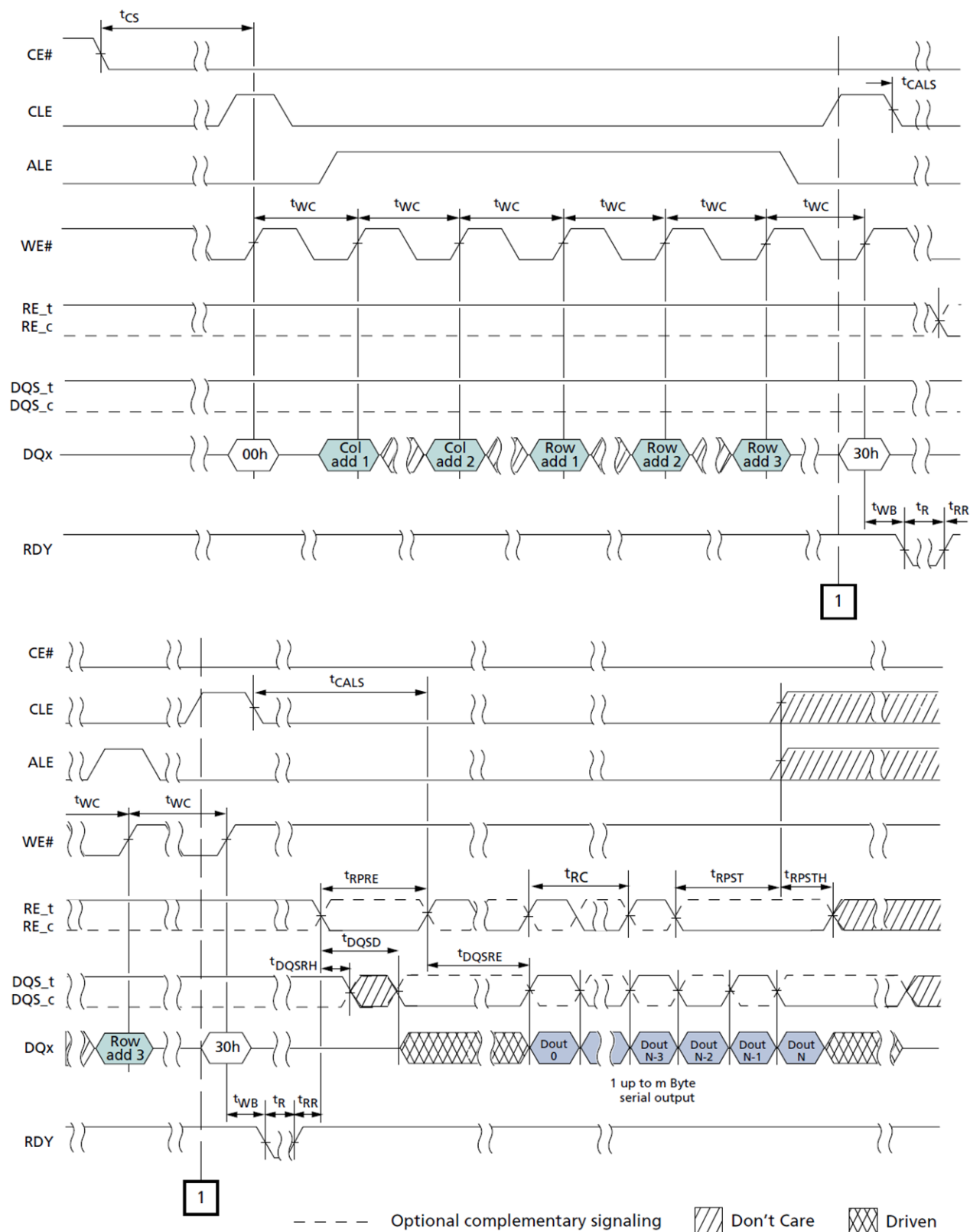
Table 69: READ PARAMETER PAGE Operation



Note: DQS is Don't Care during ACTIVE command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.

UT81NDQ512G8T

Table 70: READ PAGE Operation

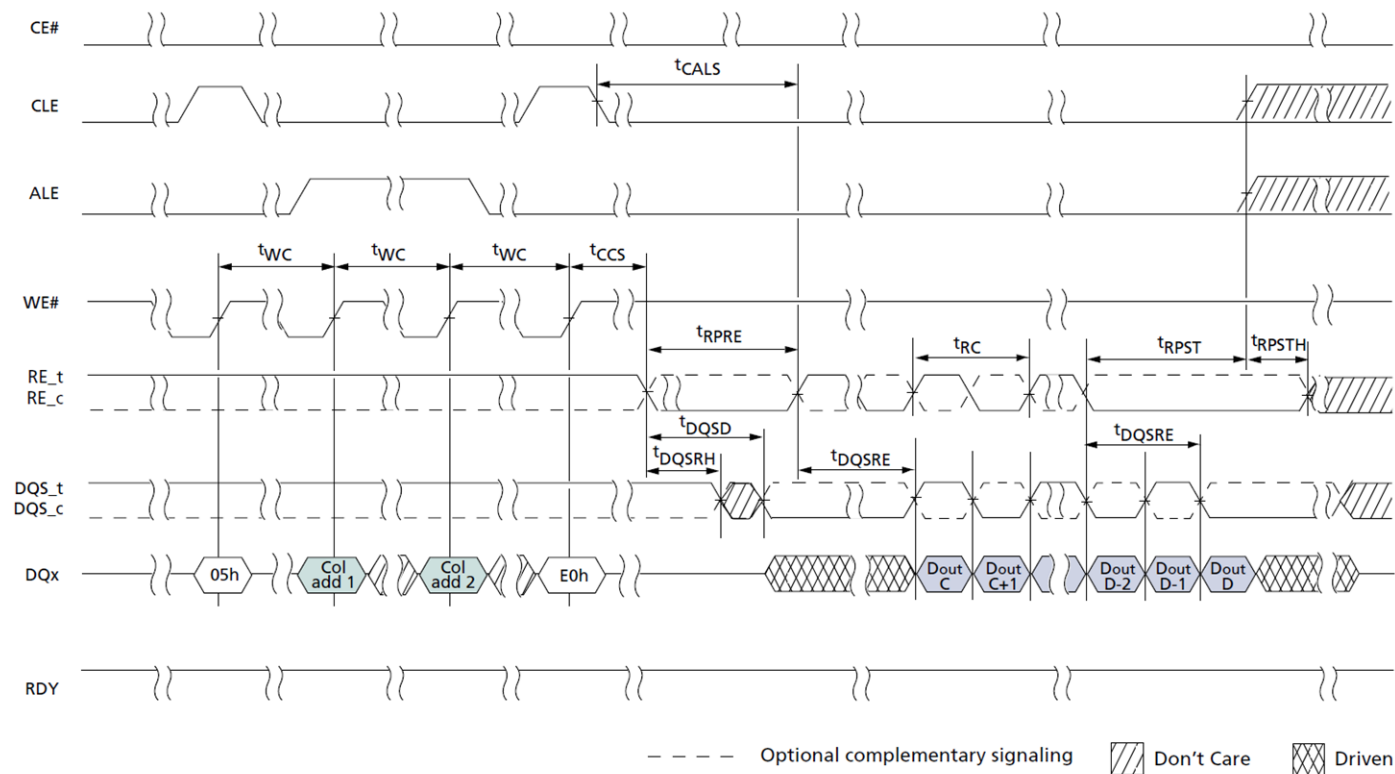


Note: DQS is Don't Care during ACTIVE command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.

4Tb TLC NAND Flash

UT81NDQ512G8T

Table 71: CHANGE READ COLUMN

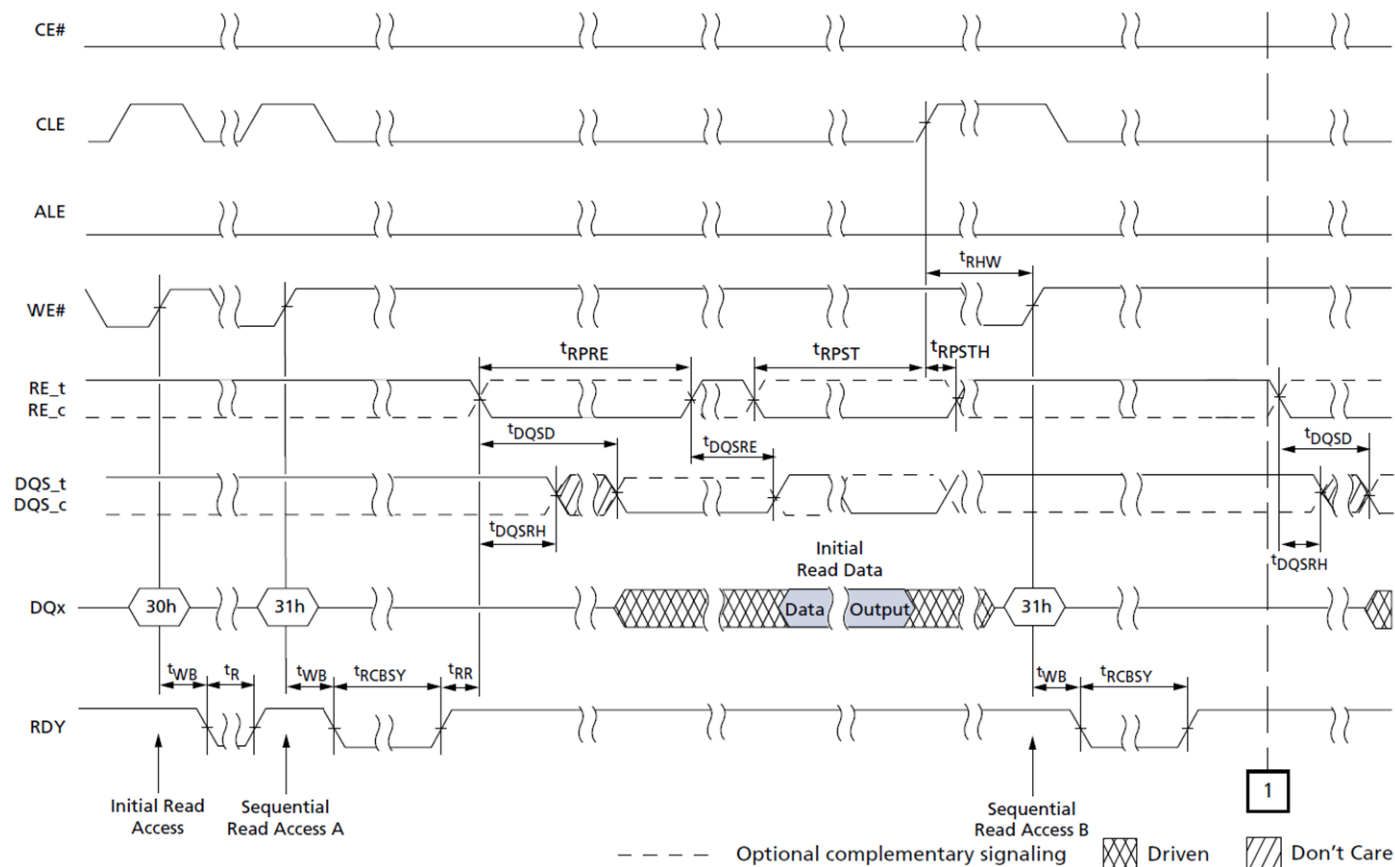


Note: DQS is Don't Care during ACTIVE command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.

4Tb TLC NAND Flash

UT81NDQ512G8T

Table 72: READ PAGE CACHE SEQUENTIAL (1 of 2)

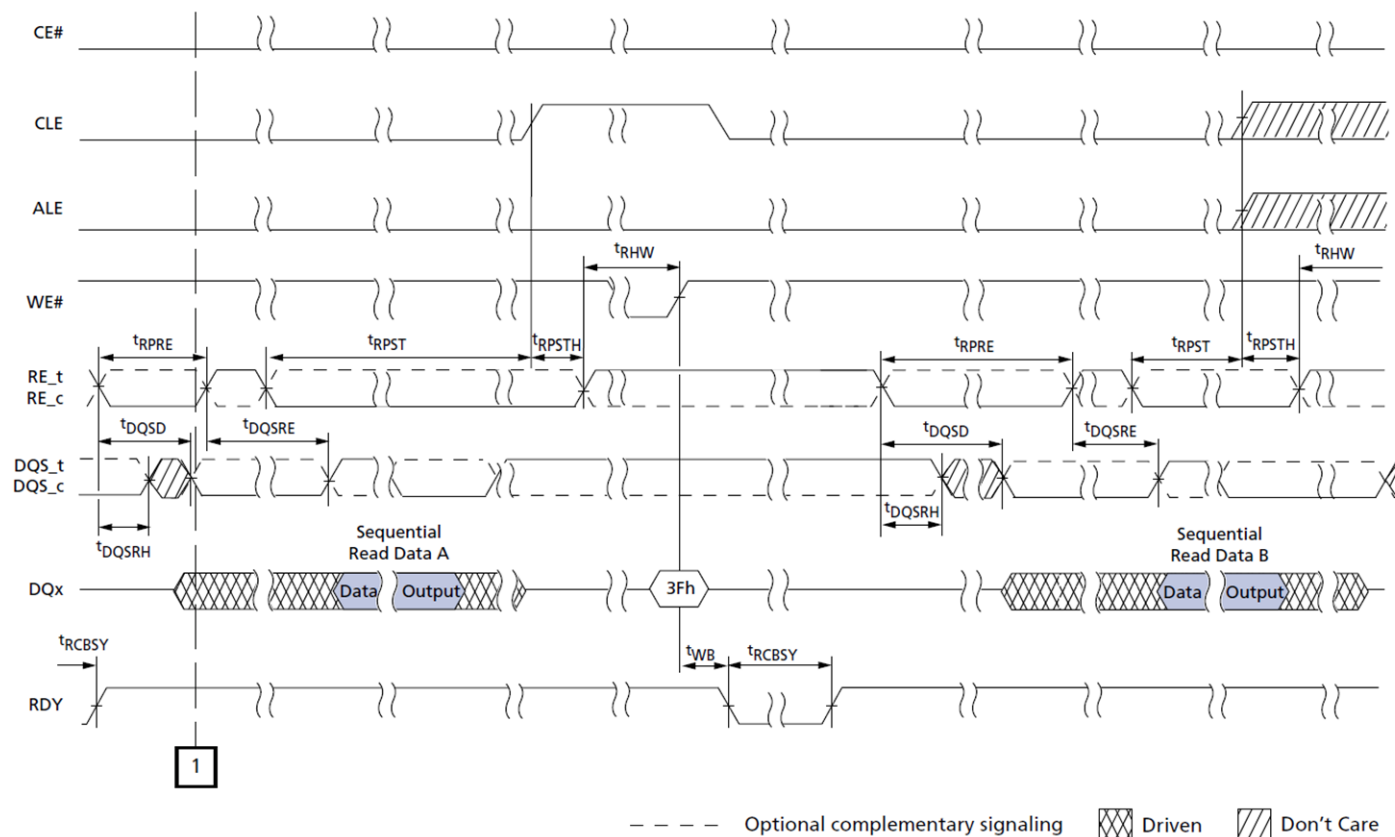


Note: DQS is Don't Care during ACTIVE command cycle (CLE is high). When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.

4Tb TLC NAND Flash

UT81NDQ512G8T

Table 73: READ PAGE CACHE SEQUENTIAL (2 of 2)

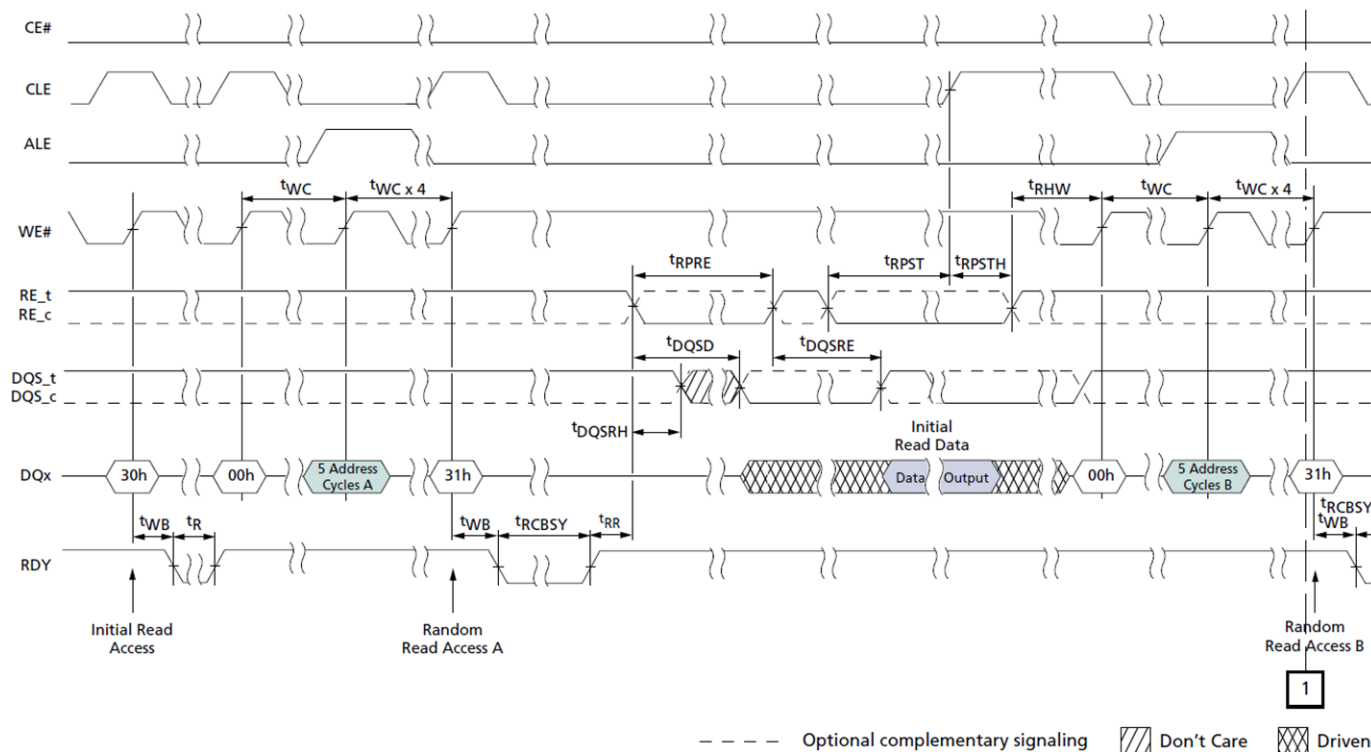


Note: DQS is Don't Care during ACTIVE command cycle (CLE is high). When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.

4Tb TLC NAND Flash

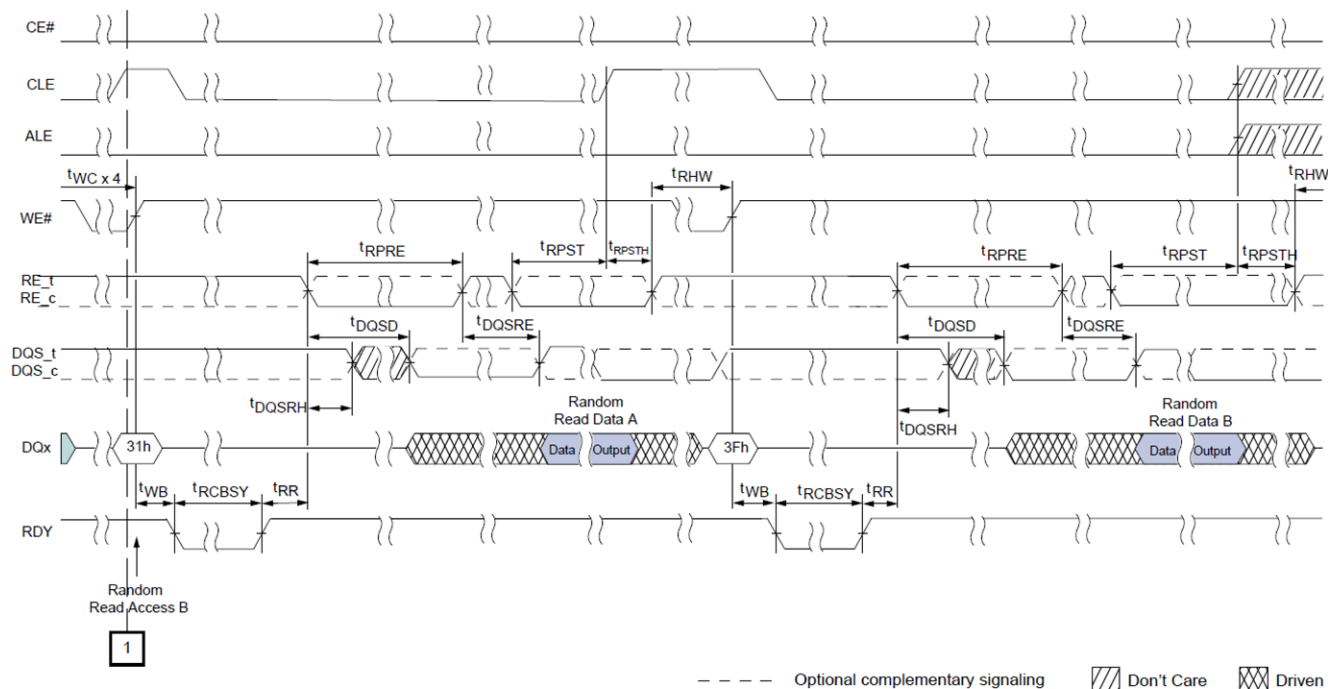
UT81NDQ512G8T

Table 74: READ PAGE CACHE RANDOM (1 of 2)



Note: DQS is Don't Care during ACTIVE command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.

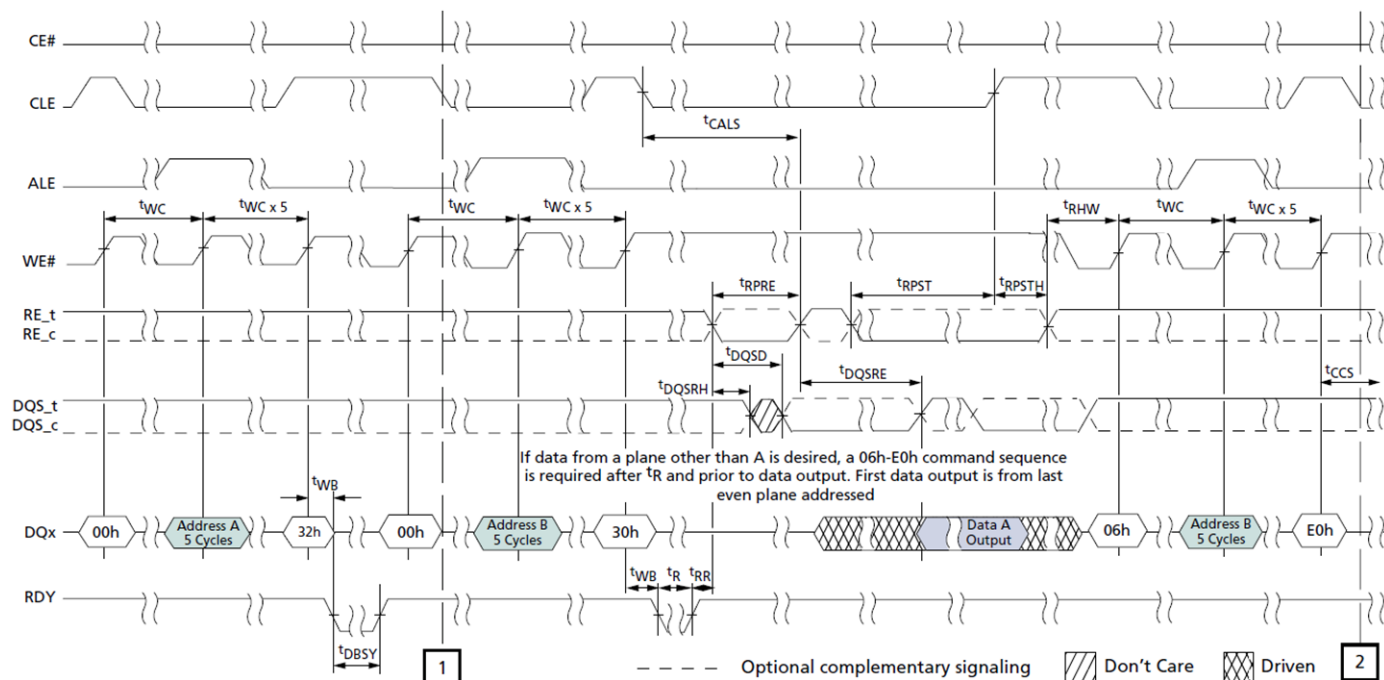
Table 75: READ PAGE CACHE RANDOM (2 of 2)



Note: DQS is Don't Care during ACTIVE command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.

UT81NDQ512G8T

Table 76: Multi-Plane Read Page (1 of 2)

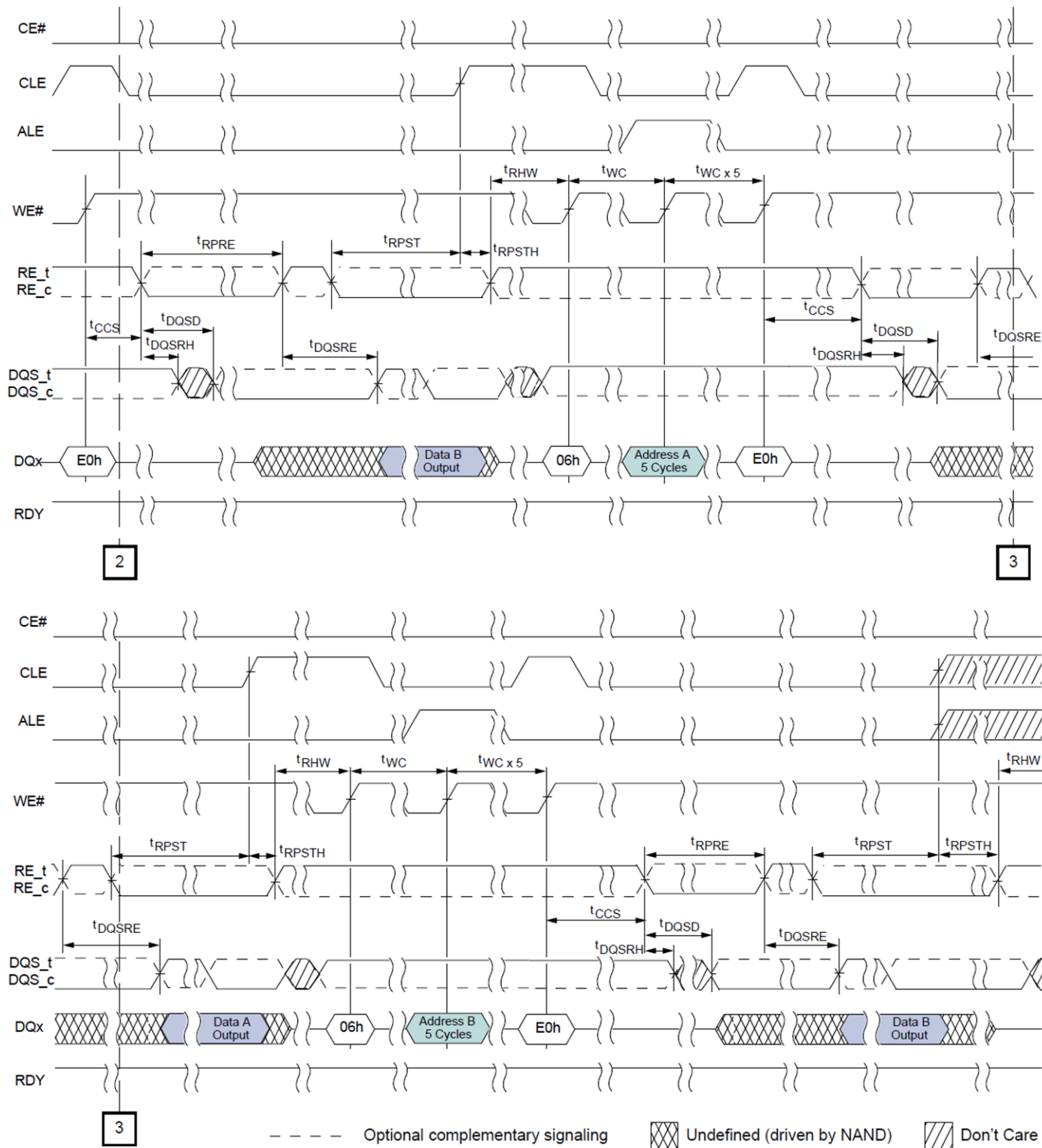


Note: DQS is Don't Care during ACTIVE command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.

4Tb TLC NAND Flash

UT81NDQ512G8T

Table 77: Multi-Plane Read Page (2 of 2)

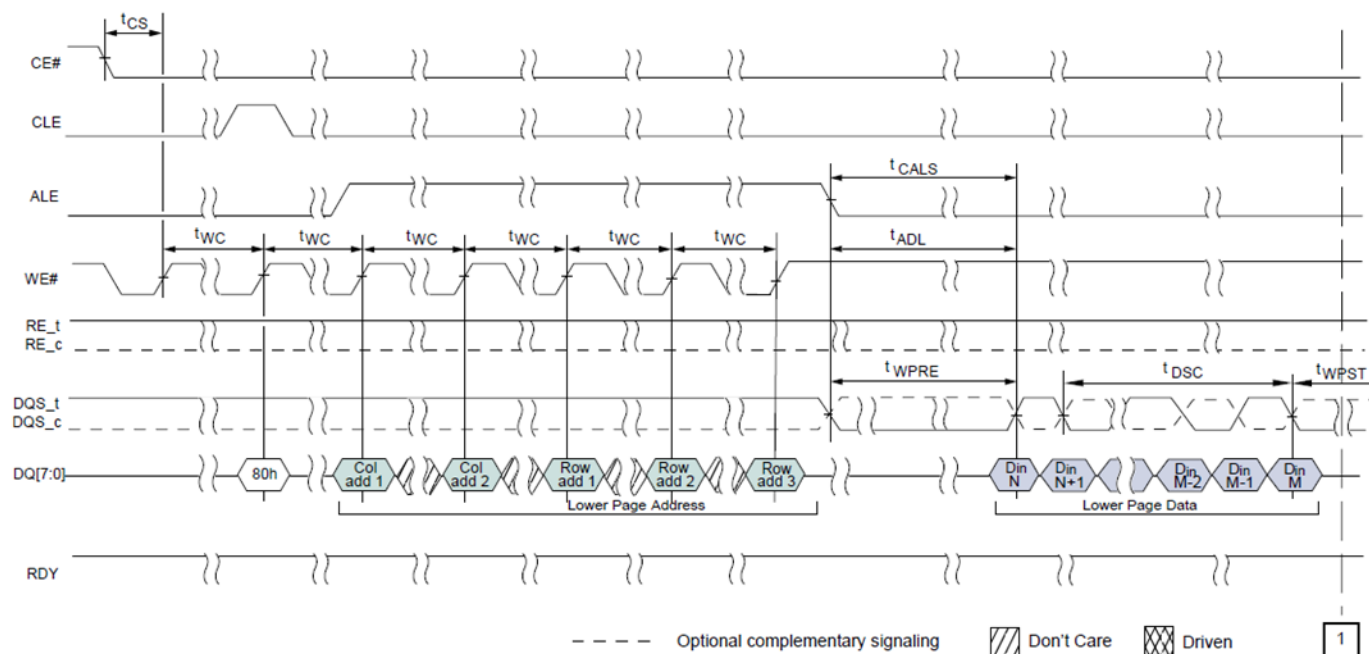


Note: 1. DQS is Don't Care during ACTIVE command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.

4Tb TLC NAND Flash

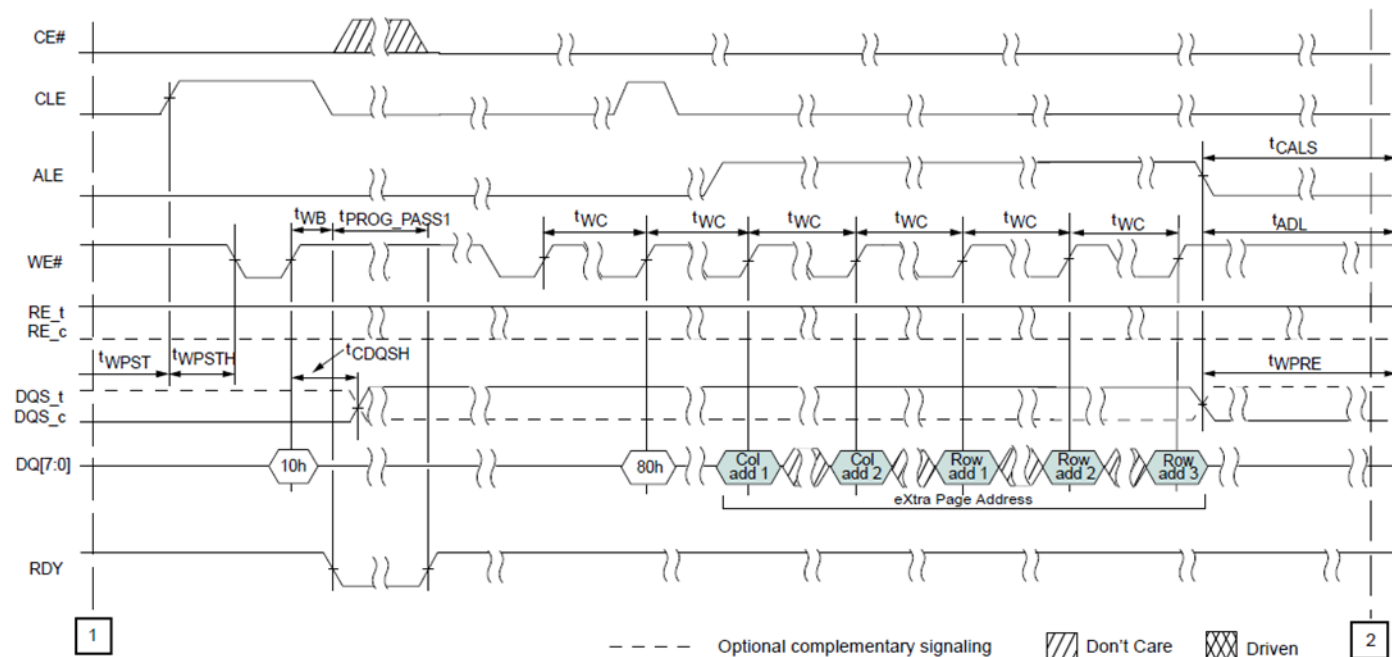
UT81NDQ512G8T

Table 78: PROGRAM PAGE Operation (1 of 5)



Note: DQS is "don't care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE and DQS are low additional current may result.

Table 79: PROGRAM PAGE Operation (2 of 5)

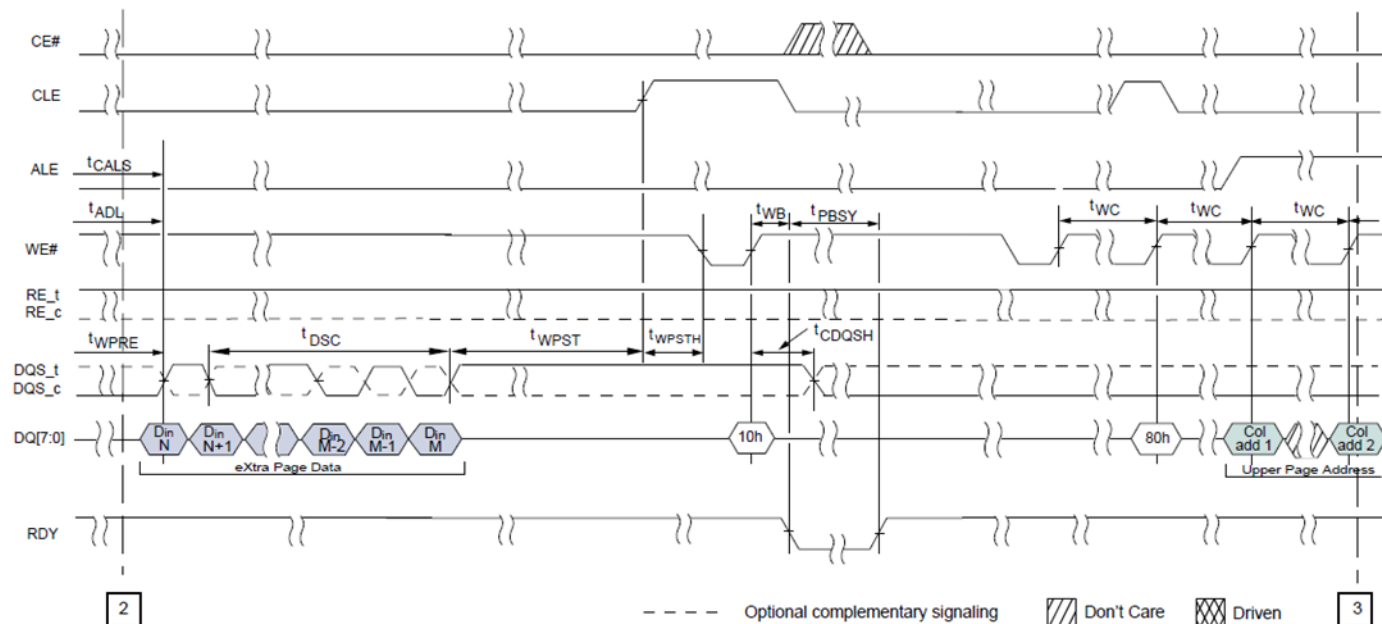


Note: DQS is "don't care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE and DQS are low additional current may result.

4Tb TLC NAND Flash

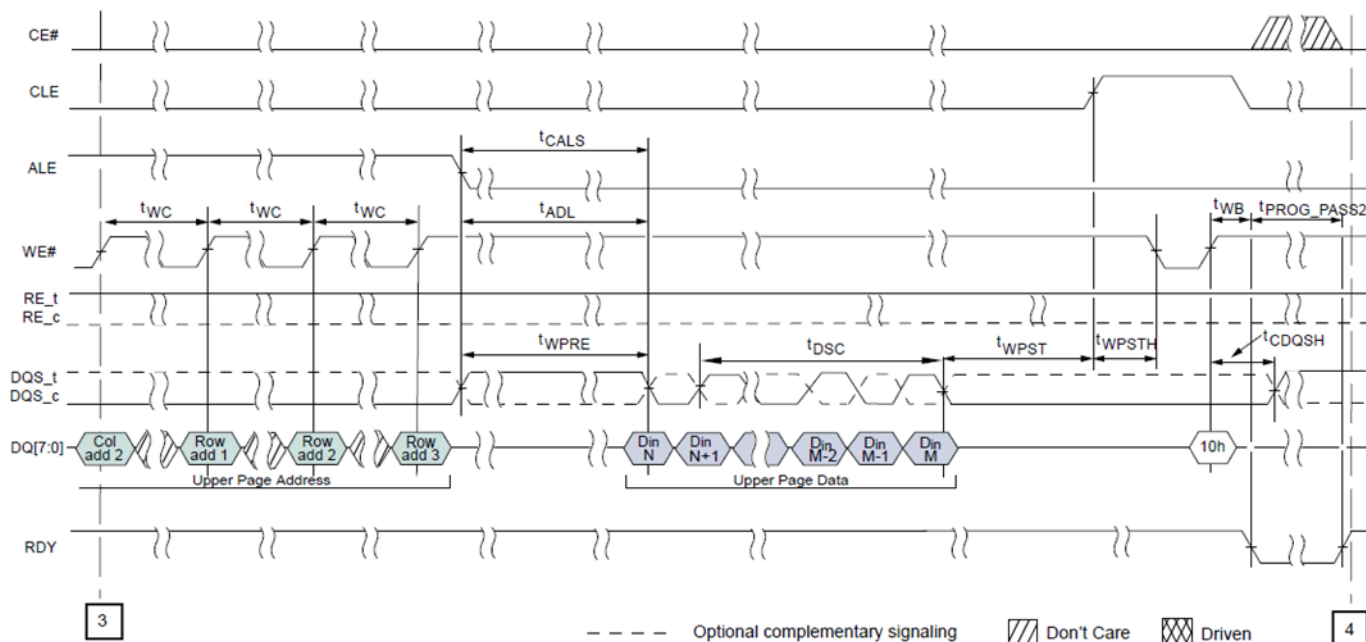
UT81NDQ512G8T

Table 80: PROGRAM PAGE Operation (3 of 5)



Note: DQS is "don't care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE and DQS are low additional current may result.

Table 81: PROGRAM PAGE Operation (4 of 5)

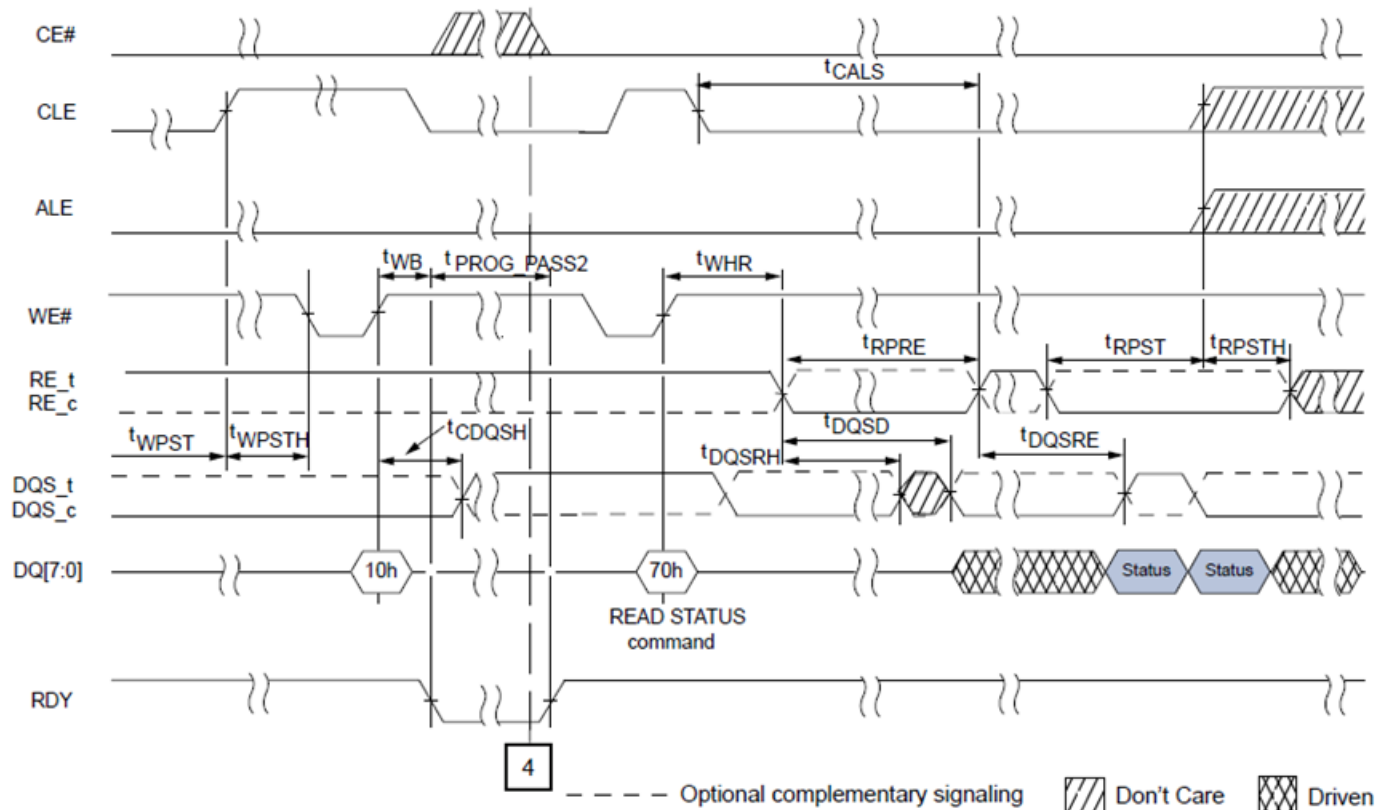


Note: DQS is "don't care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE and DQS are low additional current may result.

4Tb TLC NAND Flash

UT81NDQ512G8T

Table 82: PROGRAM PAGE Operation (5 of 5)

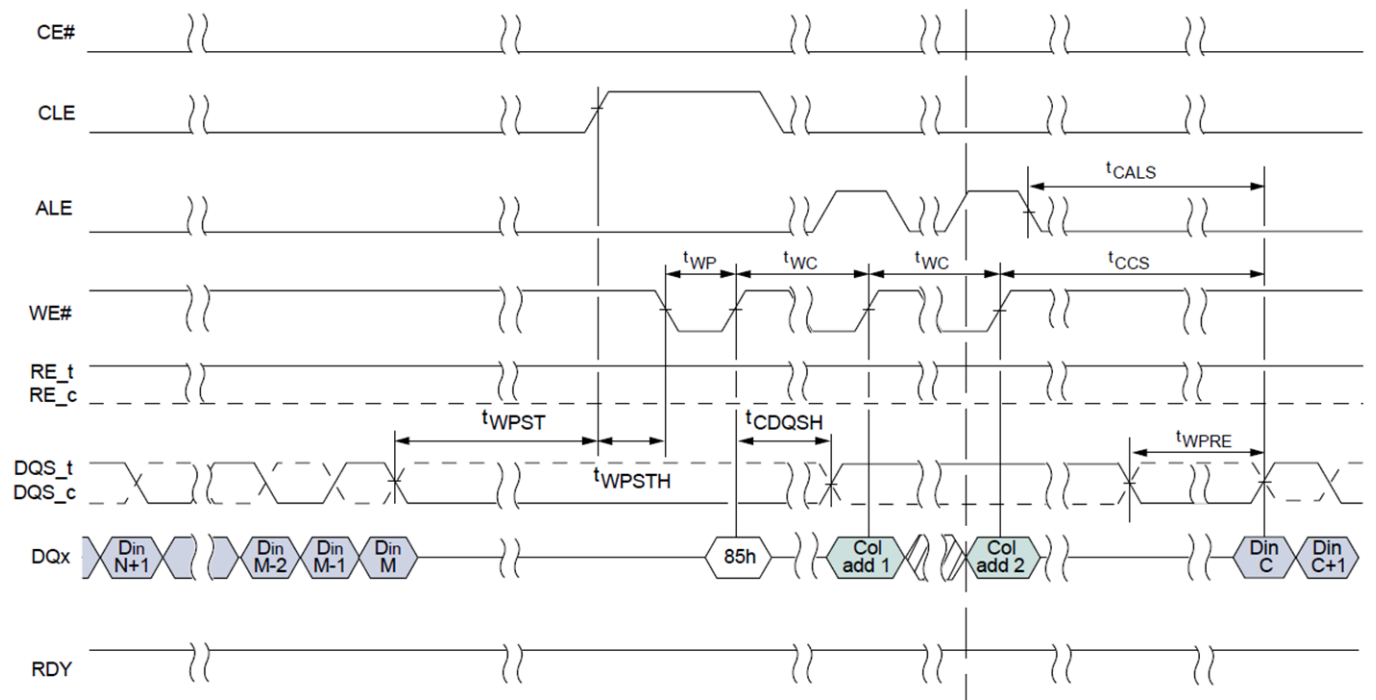


Note: DQS is "don't care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE and DQS are low additional current may result.

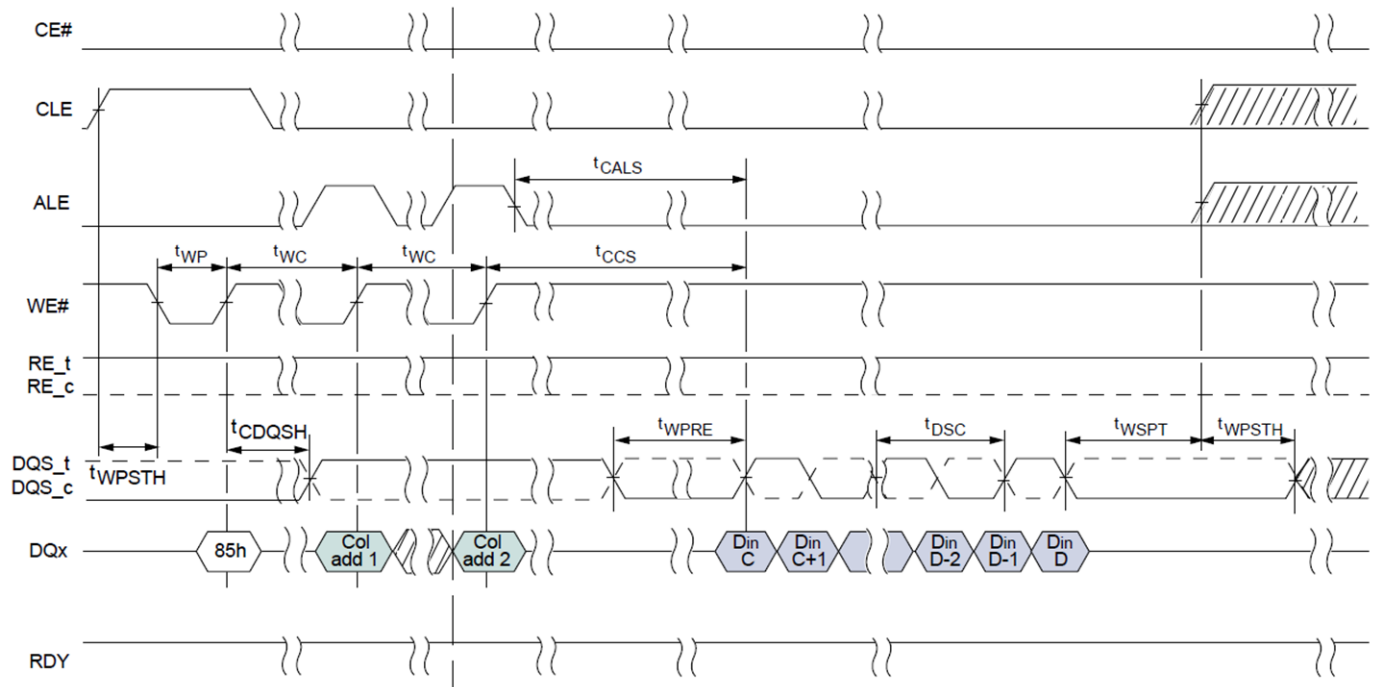
4Tb TLC NAND Flash

UT81NDQ512G8T


Table 83: CHANGE WRITE COLUMN



1



1

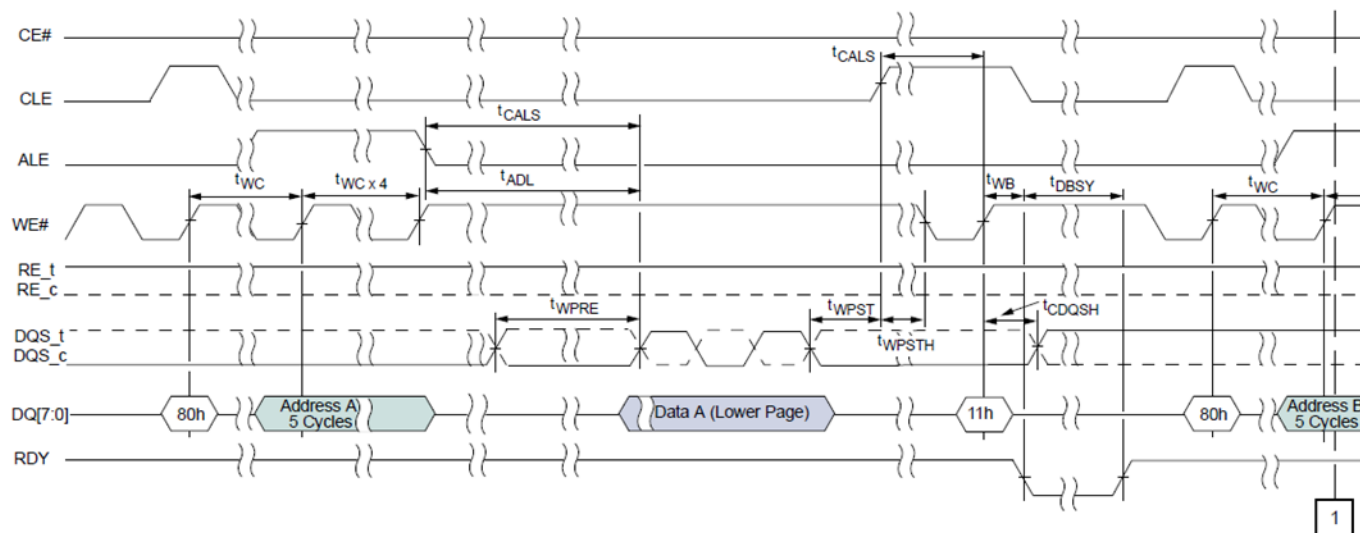
— — — — Optional complementary signaling  Don't Care

Note: DQS is Don't Care during ACTIVE command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.

4Tb TLC NAND Flash

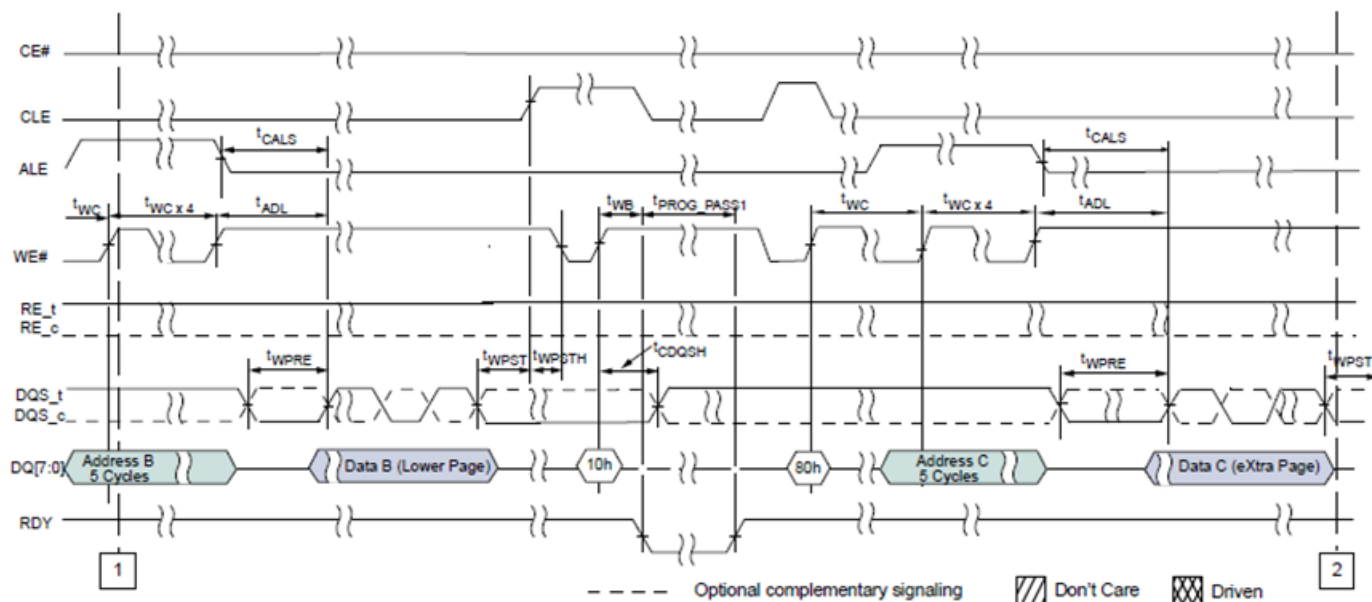
UT81NDQ512G8T

Table 84: Multi-Plane Program Page (1 of 5)



Note: DQS is "don't care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE and DQS are low additional current may result.

Table 85: Multi-Plane Program Page (2 of 5)

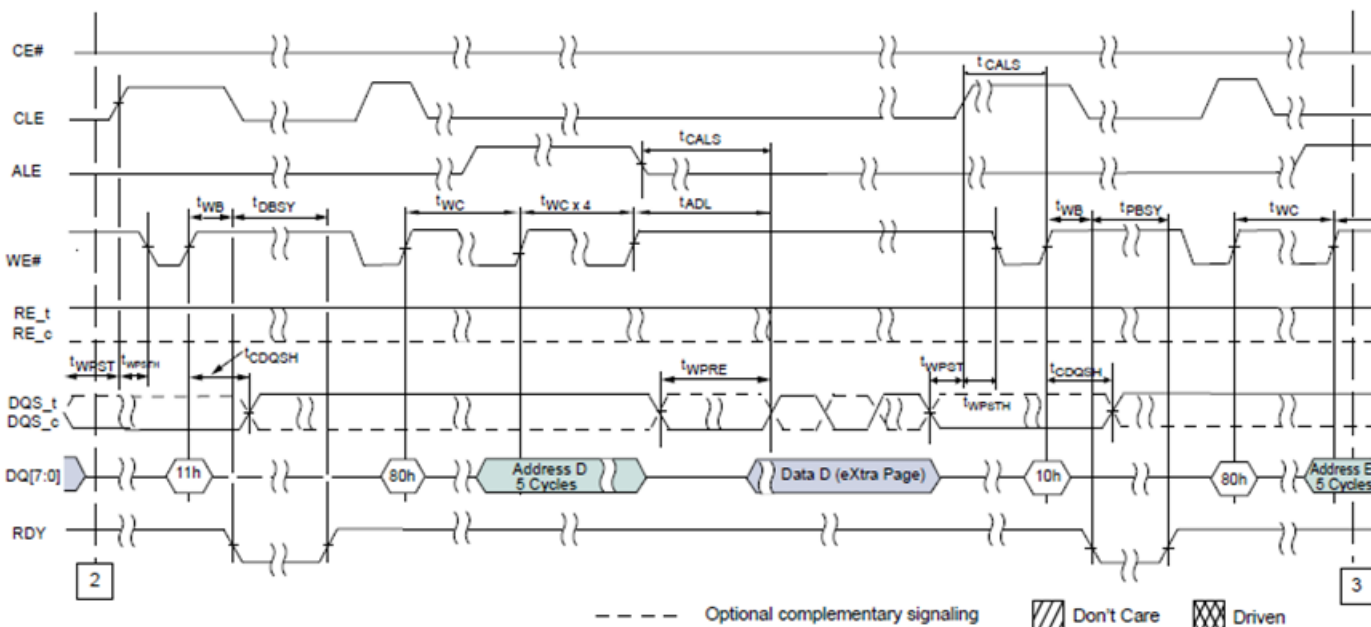


Note: DQS is "don't care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE and DQS are low additional current may result.

4Tb TLC NAND Flash

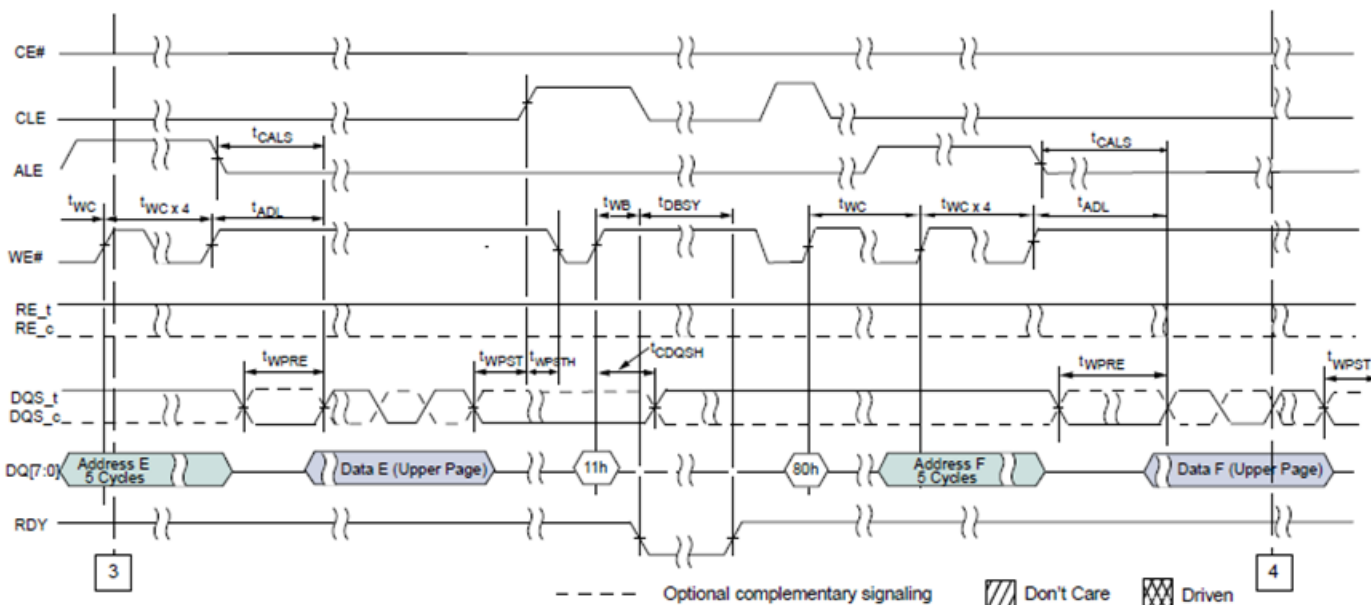
UT81NDQ512G8T

Table 86: Multi-Plane Program Page (3 of 5)



Note: DQS is "don't care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE and DQS are low additional current may result.

Table 87: Multi-Plane Program Page (4 of 5)

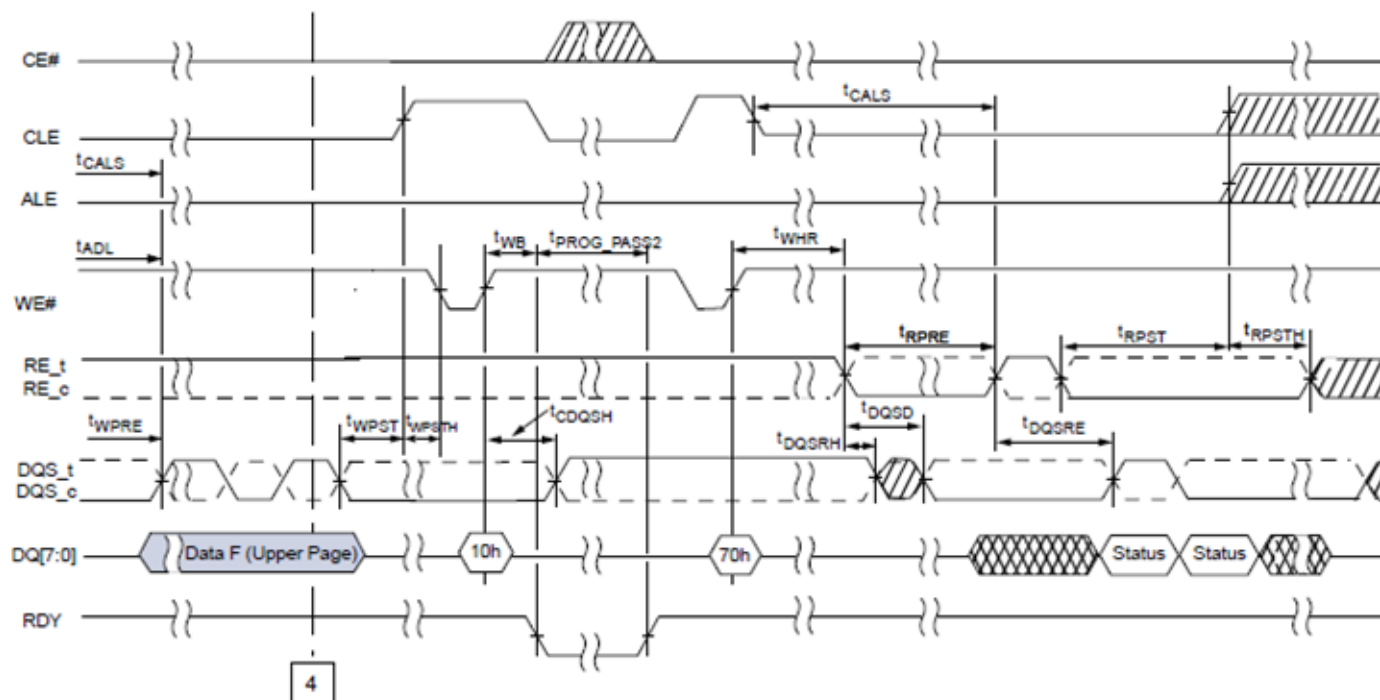


Note: DQS is "don't care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE and DQS are low additional current may result.

4Tb TLC NAND Flash

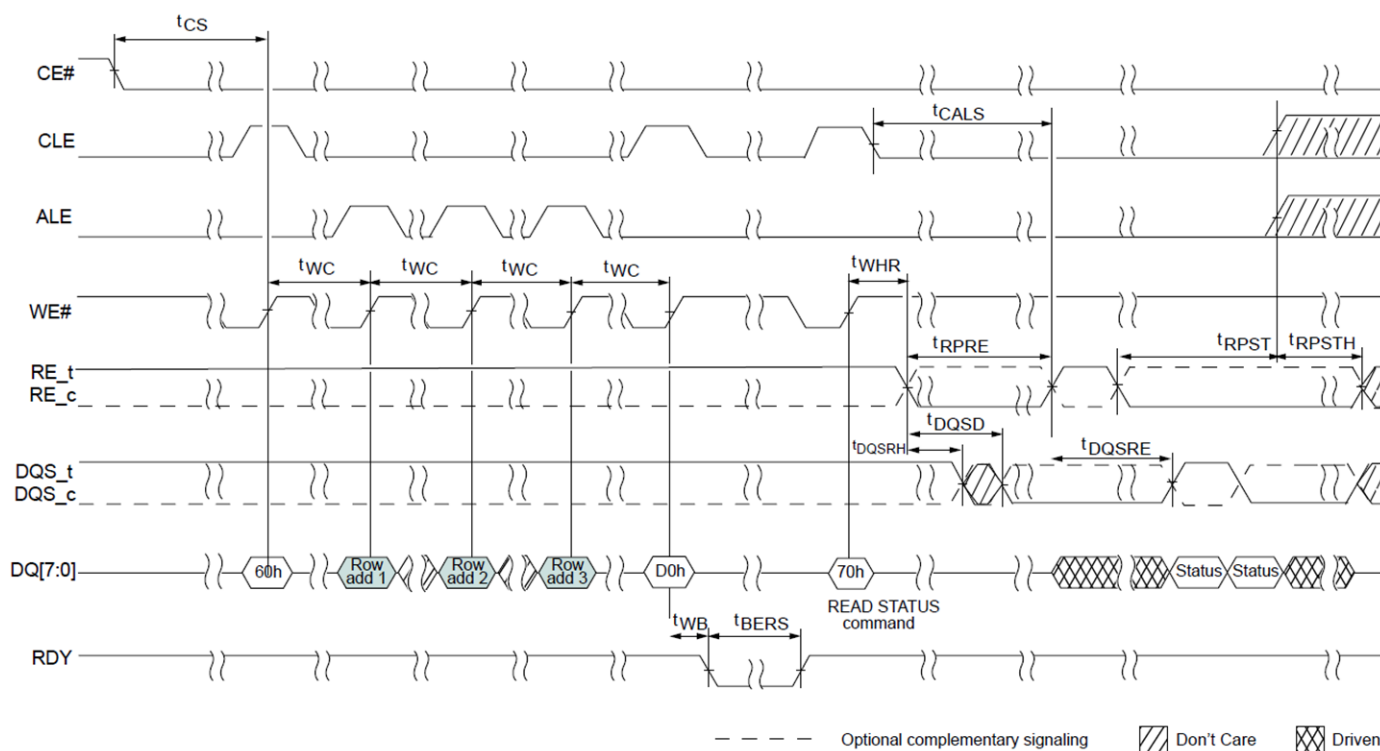
UT81NDQ512G8T

Table 88: Multi-Plane Program Page (5 of 5)



Note: DQS is "don't care" during active command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE and DQS are low additional current may result.

Table 89: ERASE BLOCK

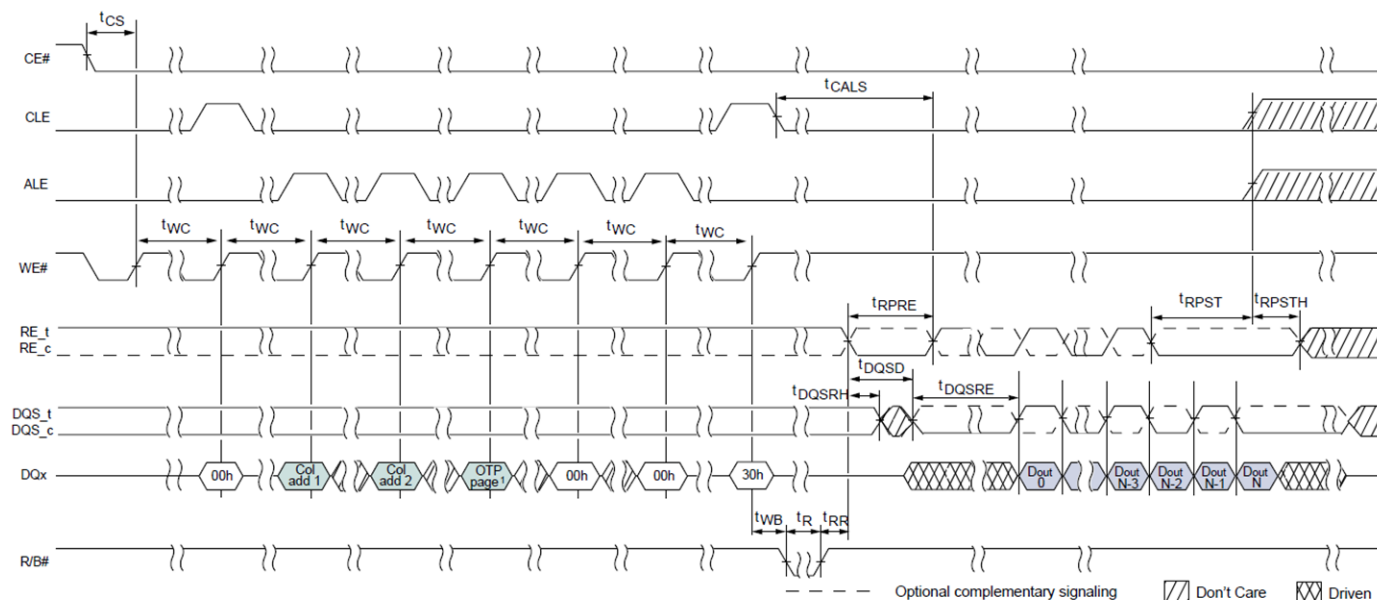


Note: DQS is Don't Care during ACTIVE command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.

4Tb TLC NAND Flash

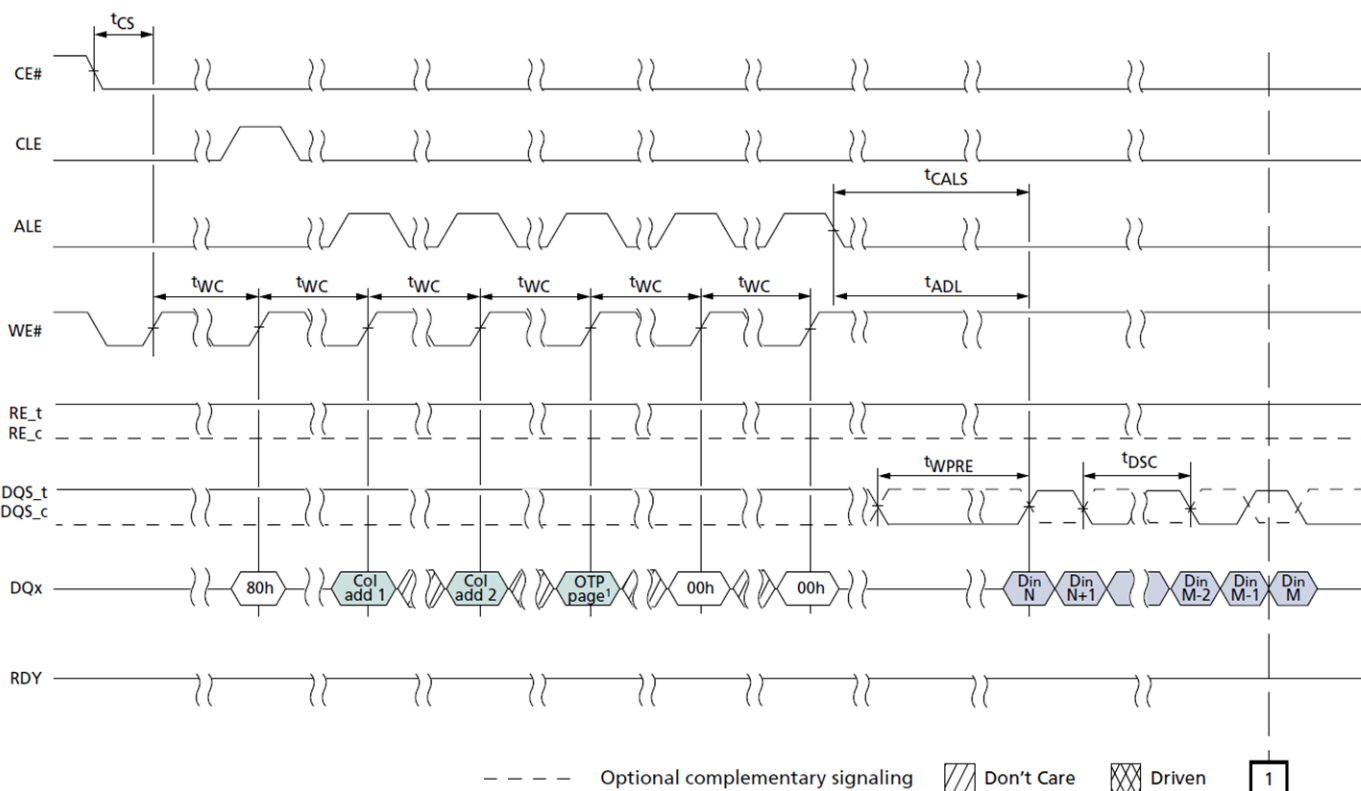
UT81NDQ512G8T

Table 90: READ OTP PAGE



Note: DQS is Don't Care during ACTIVE command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.

Table 91: PROGRAM OTP PAGE (1 of 2)

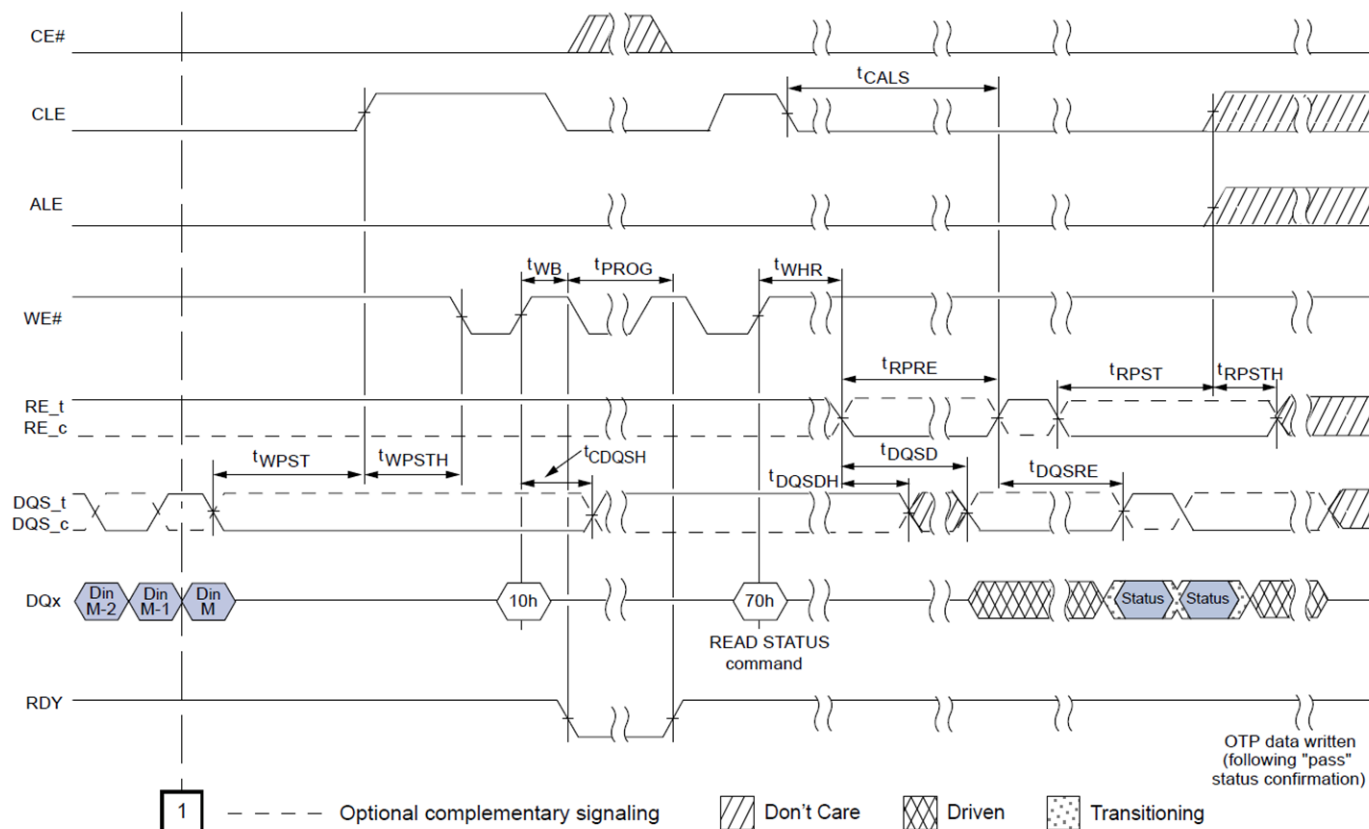


Note: DQS is Don't Care during ACTIVE command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.

4Tb TLC NAND Flash

UT81NDQ512G8T

Table 92: PROGRAM OTP PAGE (2 of 2)

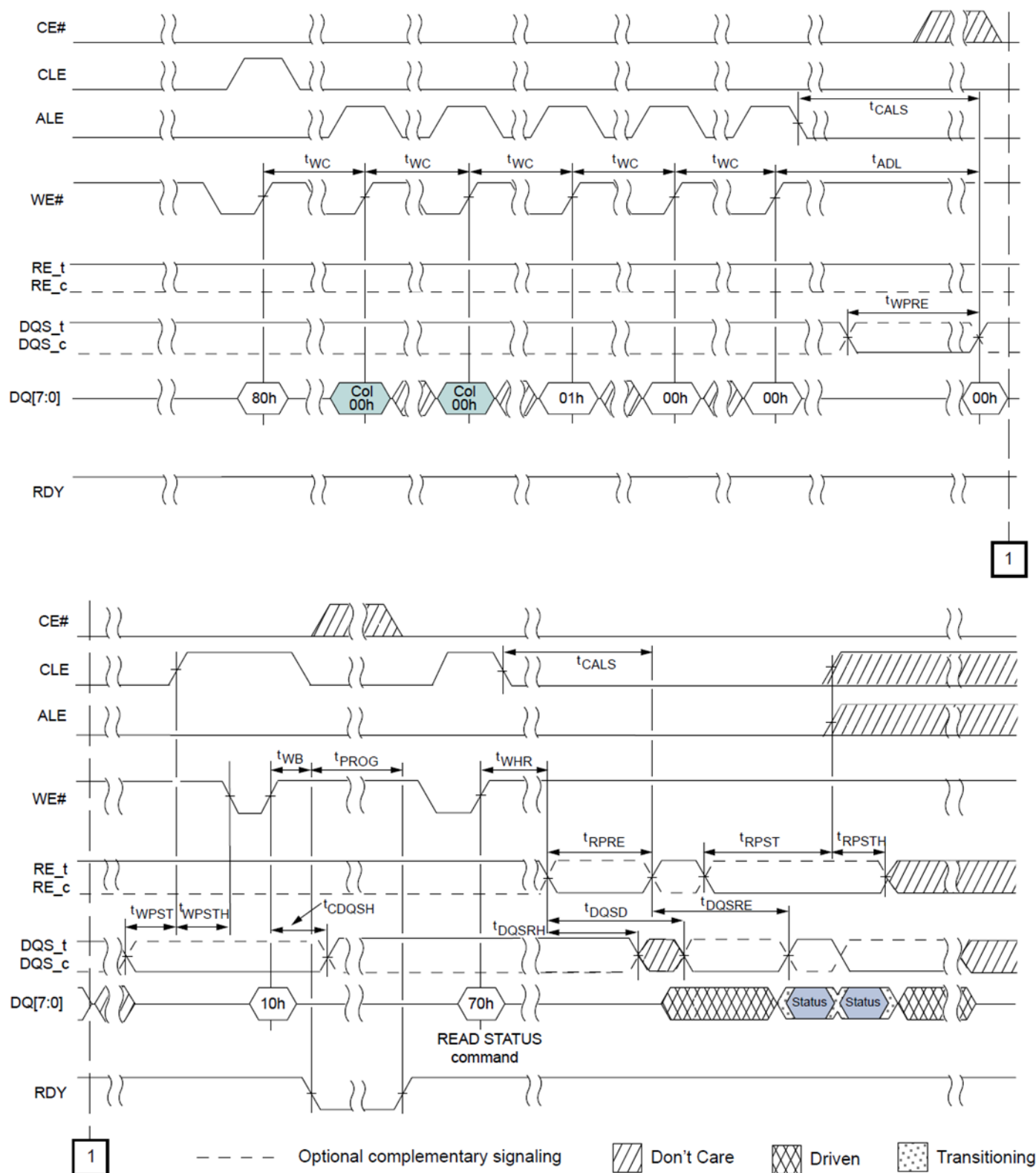


Note: DQS is Don't Care during ACTIVE command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.

4Tb TLC NAND Flash

UT81NDQ512G8T

Table 93: PROTECT OTP AREA



Note: DQS is Don't Care during ACTIVE command cycle (CLE is high) and active addresses cycle (ALE is high). When ODT is enabled and anytime CE#, ALE, CLE, and DQS are low additional current may result.

4Tb TLC NAND Flash

UT81NDQ512G8T

13 Ordering information

Generic Data Sheet Part Numbering

UT81NDQ

*

*

*

Screening Level: Notes 1, 2, & 3)

(P) = Prototype Flow

(I) = Industrial PEM

(X2) = Space PEM L2

(Temperature Range: 25°C only)

(Temperature Range: -40°C to 85°C)

(Temperature Range: -40°C to 85°C)

Case Outline:

(B) = 132-Plastic Ball Grid Array (1mm Pitch, 63Sn 37Pb Solder Balls)

Radiation Assurance: (Note: 4 & 5)

(-) = No Radiation Assurance

(D) = 1E4 (10 krad(Si)) – effective dose rate 0.1 rad(Si)/s

(P) = 3E4 (30 krad(Si)) – effective dose rate 0.1 rad(Si)/s

(L) = 5E4 (50 krad(Si)) – effective dose rate 0.1 rad(Si)/s (Contact Factory)

Device Type

(512G8T) = 4Tb TLC NAND (Octal Die Package)

UT81NDQ = NAND Flash

Notes:

- 1) Space PEM L2 is a Frontgrade specific flow for space grade plastic encapsulated modules based on NASA PEM-INST-001 Level 2. Space PEM QD is a Frontgrade defined flow for plastic encapsulated modules having quantified radiation performance and lot pedigree, but less screening than Space PEM L2.
- 2) Datapacks may be ordered separately for Space PEM QD and Space PEM L2 orders.
- 3) If the flow ordered is Industrial "I" with an RHA designation "L", "P", or "D", the product will be supplied to the Frontgrade Space PEM QD flow.
- 4) Radiation assurance levels may ONLY be applied to Space PEM QD and L2 orders.
- 5) "Contact Factory" is listed for options that are subject to availability.

4Tb TLC NAND Flash

UT81NDQ512G8T

14 Revision History

Date	Change Description
11/22	Initial release
08/23	Changed ordering page options and notes. Updated document template

4Tb TLC NAND Flash

UT81NDQ512G8T

Datasheet Definitions

	DEFINITION
Advanced Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet is subject to change . Specifications can be TBD and the part package and pinout are not final .
Preliminary Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

The following United States (U.S.) Department of Commerce statement shall be applicable if these commodities, technology, or software are exported from the U.S.: These commodities, technology, or software were exported from the United States in accordance with the Export Administration Regulations. Diversion contrary to U.S. law is prohibited.

Frontgrade Colorado Springs LLC (Frontgrade) reserves the right to make changes to any products and services described herein at any time without notice. Consult an authorized sales representative to verify that the information in this data sheet is current before using this product. The company does not assume any responsibility or liability arising out of the application or use of any product or service described herein, except as expressly agreed to in writing; nor does the purchase, lease, or use of a product or service convey a license under any patent rights, copyrights, trademark rights, or any other of the intellectual rights of the company or of third parties.