DATASHEET

RELEASED 8/19/21

8-bit Bus Switch

UT54BS3245

Features

- 3.3V operating power supply with typical 11Ω switch connection between ports
- 5.0V operating power supply with typical 5Ω switch connection between ports
- Bidirectional operation
- Ultra-low power CMOS technology
- ESD Rating HBM: 2000V, Class 2
- Signal Isolation: -60dB
- Channel Bandwidth (3dB): 500MHz
- Standard Microcircuit Drawing (SMD):
  - 5962-15244
  - QML Q and V compliant part
- Package Options: 20-Lead Flatpack

Operational Environment

- Temperature Range: -55°C to +125°C
- Total Dose: 300 krad(Si)
- SEL Immune: ≤100 MeV-cm^2/mg

Applications

- Memory Interface
- Bus Isolation
- Redundancy
- Supports Analog Applications

Introduction

The UT54BS3245 provides 8 bits of high-speed CMOS-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay. The device is organized as one 8-bit low-impedance switch. When output enable (/EN) is low, the 8-bit bus switch is on and port A is connected to port B. When /EN is high, the switch is open and a high-impedance state exists between the two ports.

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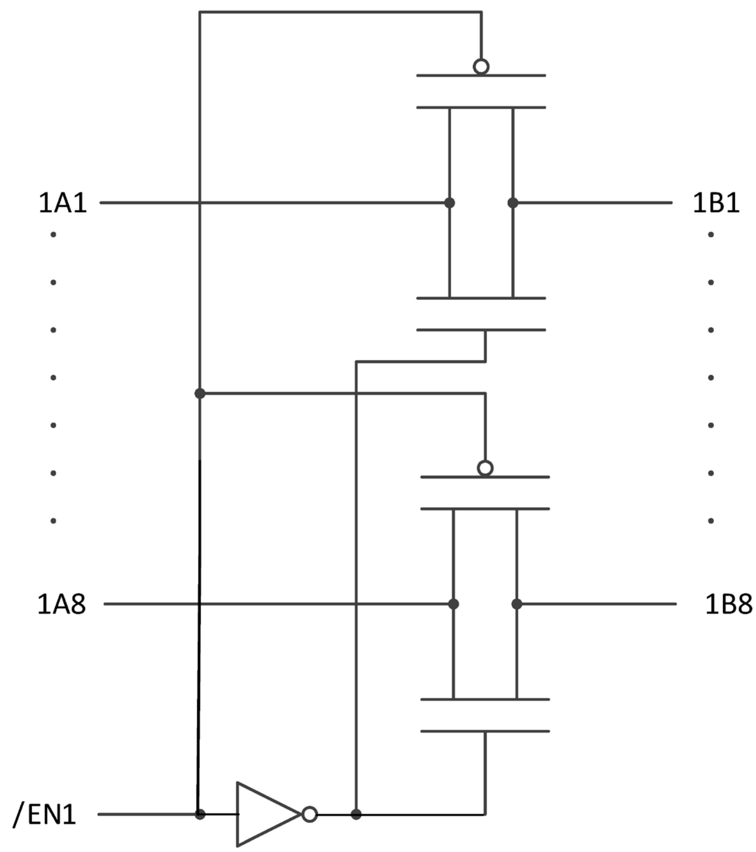

Pinlist

TO	=	TTL Output
TTB	=	Three-State TTL Bidirectional
CI	=	CMOS Input
TUI	=	TTL Input (Internally Pulled High)
TI	=	TTL Input
TTO	=	Three-State TTL Output
DIO	=	Differential Input/Output

Table 1: Pinlist

Number	Name	Description
2, 3, 4, 5, 6, 7, 8, 9,	nA	Port A Pins
11, 12, 13, 14, 15, 16, 17, 18	nB	Port B pins
19	/EN	Active LOW enable pin
10	V_{SS}	Ground Pin
20	V_{DD}	Supply Pin, +3.3V or +5.0V
1	NC	No Connect (electrically not connected to die)

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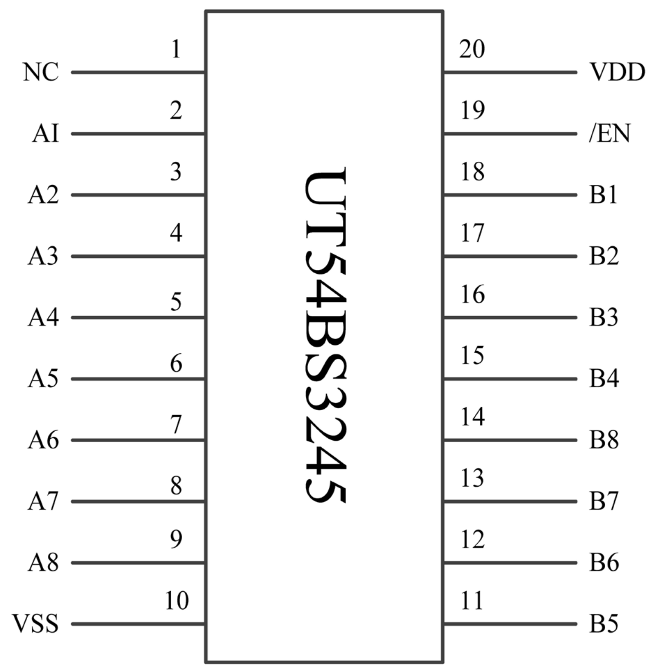
Package Pinout Diagram



Absolute Maximum Ratings [1, 2]

Table 2: Absolute Maximum Ratings

Symbol	Parameter	MIN	MAX	Units
V_{DD}	Positive Supply Voltage	-0.5	+7.2	V
V_I	Input Voltage	-0.5	V_{DD}+0.3	V
I_{CCC}	DC Channel Current		65	mA
P_D	Max Power Dissipation (3)		1.6	W
T_J	Junction Temperature		+150	°C
θ_{JC}	Thermal resistance, junction-to-case		15	°C/W
T_{STG}	Storage Temperature	-65	+150	°C
ESD_{HBM}	ESD Protection (4)		2000	V

Notes:

1) Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification are not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2) All voltages referenced to V_{SS}
3) Per MIL-STD-883, method 1012, section 3.4.1, $P_D=(T_J(max)-T_C(max))/\theta_{JC}$)
4) Per MIL-STD-883, method 3015, Table 3

Operational Environment (1)

Table 3: Operational Environment

Symbol	Parameter	Limit	Units
TID	Total Ionizing Dose (2)	300	krad(Si)
SEL	Single Event Latchup Immunity (3)	≤100	MeV-cm²/mg

Notes:

1) For devices with procured with a total ionizing dose tolerance guarantee, post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to maximum TID level procured.
2) Per MIL-STD-883, method 1019, condition A
3) SEL is performed at VDD = Max Voltage at 125°C

Recommended Operating Conditions (1)

Table 4: Recommended Operating Conditions

Symbol	Parameter	Conditions	MIN	MAX	Units
V_{DD}	Positive Supply Voltage		3.0 or 4.5	3.6 or 5.5	V
V_{IN}	Input Voltage on any pin		0.0	V_{DD}	V
T_C	Case Temperature Range		-55	+125	°C
t_R	Rise time, logic inputs	Transition from V_{IL} to V_{IH}		5	ns
t_F	Fall time, logic inputs	Transition from V_{IH} to V_{IL}		5	ns
I_{CCC}	DC Channel Current			60	mA

Note:

1) All voltages referenced to V_{SS}

DC Electrical Characteristics [1]

(V_{DD}= 5.0V ± 0.5V, 3.3V ± 0.3V, -55°C< T_C <+125°C); Unless otherwise noted, T_C is per the temperature range ordered

Table 5: DC Electrical Characteristics

Symbol	Parameter	Conditions	MIN	MAX	Units
V_{IH}	High digital input voltage	V_{DD} = 3.6, 5.5	0.7* V_{DD}		V
V_{IL}	Low digital input voltage	V_{DD} = 3.0, 4.5		0.3* V_{DD}	V
I_{ID}	Leakage current digital	V_{DD} (max); V_I=V_{DD} or V_{SS}	-1	1	µA
I_{IA}	Leakage current analog	V_{DD} (max); V_I=V_{DD} or V_{SS}	-1	1	µA
I_{DD}	Active supply current	V_{DD} = 3.6, 5.5		0.1	mA/MHz
I_{DDQ}	Quiescent Supply Current	V_{DD} (max); I_O=0mA; /EN=V_{DD}		10	µA
C_I	Input Capacitance (/EN) [2]	V_I=V_{DD} or V_{SS}		18	pF
$C_{IO(OFF)}$	Channel pin capacitance (channel disabled) [2]	V_{DD} (max); V_O=V_{DD} or V_{SS}; V_I=V_{DD}/2; /EN=V_{DD}		18	pF
R_{ONL}	Resistance through switch (channel input low) [3]	V_{DD}=4.5V, V_I=V_{SS}, /EN=0V, I_O=30mA		10	Ω
		V_{DD}=4.5V, V_I=V_{SS}, /EN=0V, I_O=15mA		10	Ω
		V_{DD}=3.0V, V_I=V_{SS}, /EN=0V, I_O=30mA		12	Ω
		V_{DD}=3.0V, V_I=V_{SS}, /EN=0V, I_O=15mA		12	Ω
R_{ONH}	Resistance through switch (channel input high) [3]	V_{DD}=4.5V, V_I=V_{DD}, /EN=0V, I_O=-30mA		10	Ω
		V_{DD}=4.5V, V_I=V_{DD}, /EN=0V, I_O=-15mA		10	Ω
		V_{DD}=3.0V, V_I=V_{DD}, /EN=0V, I_O=-30mA		12	Ω
		V_{DD}=3.0V, V_I=V_{DD}, /EN=0V, I_O=-15mA		12	Ω
$R_{ON(FLAT)}$	Switch on resistance [3]	V_{DD}=4.5V, /EN=0V, I_O=$^{+/-}$15mA, 25°C V_{IN} = V_{SS}, V_{DD} /2, V_{DD}		2	Ω
		V_{DD}=3.0V, /EN=0V, I_O=$^{+/-}$15mA, 25°C V_{IN} = V_{SS}, V_{DD} /2, V_{DD}		10	Ω

Notes:

1) All voltages referenced to V_{SS}
2) Per MIL-STD-883, method 3012
3) Guaranteed by Characterization

AC Electrical Characteristics [1]

(V_{DD}= 5.0V ± 0.5V, 3.3V ± 0.3V, -55°C< T_C <+125°C); Unless otherwise noted, T_C is per the temperature range ordered

Table 6: AC Electrical Characteristics

Symbol	Parameter	Conditions	MIN	MAX	Units
t_{PD15}	Channel Propagation Delay (1)	V_{DD}= 5.0V ± 0.5V, I1=+/-15mA, /EN=V_{SS}		250	ps
t_{EN}	Channel Enable Delay (2)	V_{DD}= 5.0V ± 0.5V	1	5	ns
t_{DIS}	Channel Disable Delay (2)	V_{DD}= 5.0V ± 0.5V	1	5	ns
t_{PD15}	Channel Propagation Delay (1)	V_{DD}= 3.3V ± 0.3V, I1=+/-15mA, /EN=V_{SS}		250	ps
t_{EN}	Channel Enable Delay (2)	V_{DD}= 3.3V ± 0.3V	1	7	ns
t_{DIS}	Channel Disable Delay (2)	V_{DD}= 3.3V ± 0.3V	1	7	ns

Notes:

1) The propagation delay through the channel is based on the RC time constant of the channel capacitance and maximum channel resistance for defined V_{DD}
2) Measured at 300mV above or below steady state output voltage using output test load circuit

Table 7: Signal Characteristics

Symbol	Parameter	Conditions	MIN	TYP	MAX	Units
X_{TALK} [1]	Channel Cross-Talk (1, 2)	V_{DD} = 5.0V			-60	dB
X_{TALK} [1]	Channel Cross-Talk (1, 2)	V_{DD} = 3.3V			-60	dB
ISO_{OFF} [1]	Off Isolation (1,2)				-60	dB

Notes:

1) Guaranteed by design
2) RL = 50Ω, CL = 50pF, fin = 1MHz, Vin = 1VRMS centered at $V_{DD}/2$

Timing Diagram

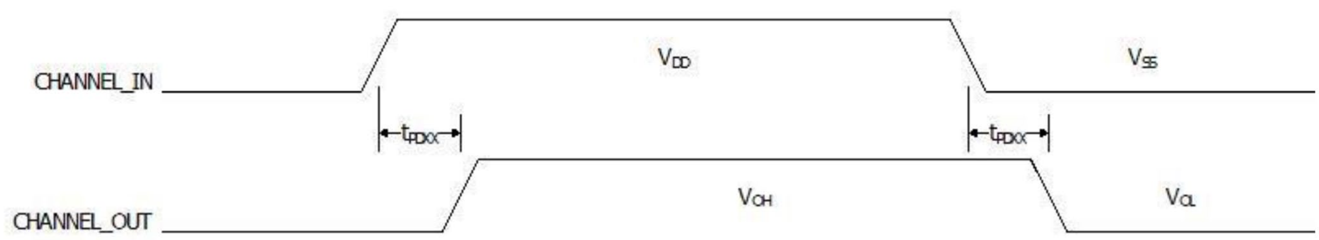


Figure 3: Channel Propagations Delay (/EN = V_{SS})

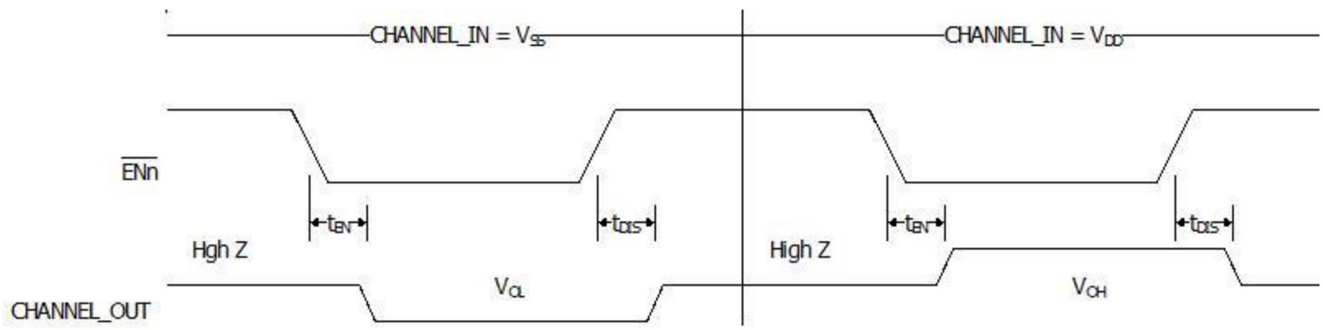


Figure 4: Enable Timing

Test Loads

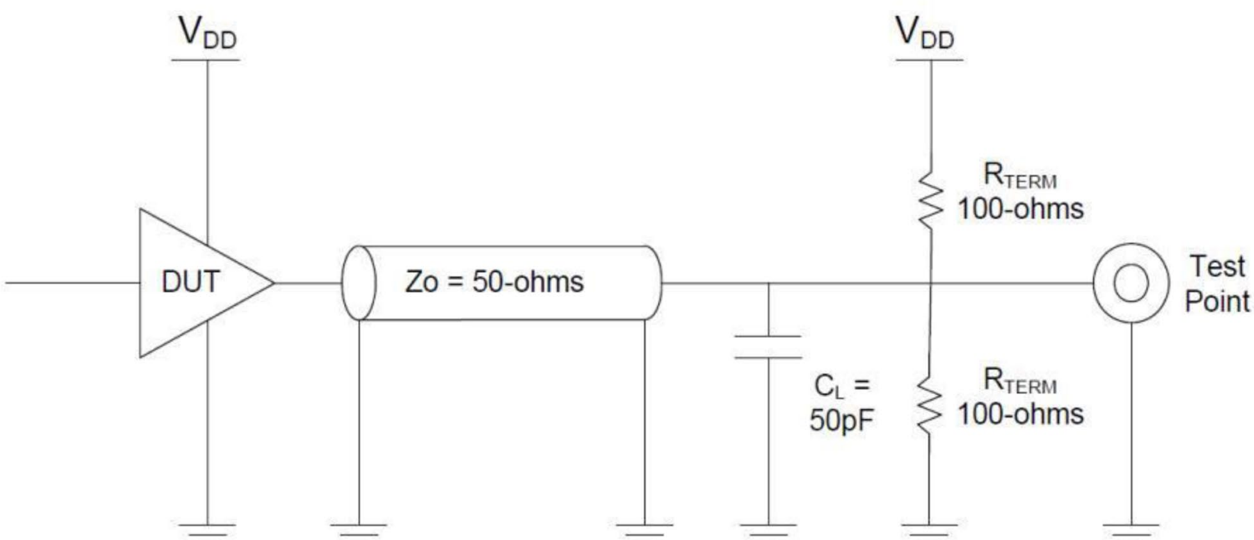


Figure 5: Standard Test Load

Package Drawings

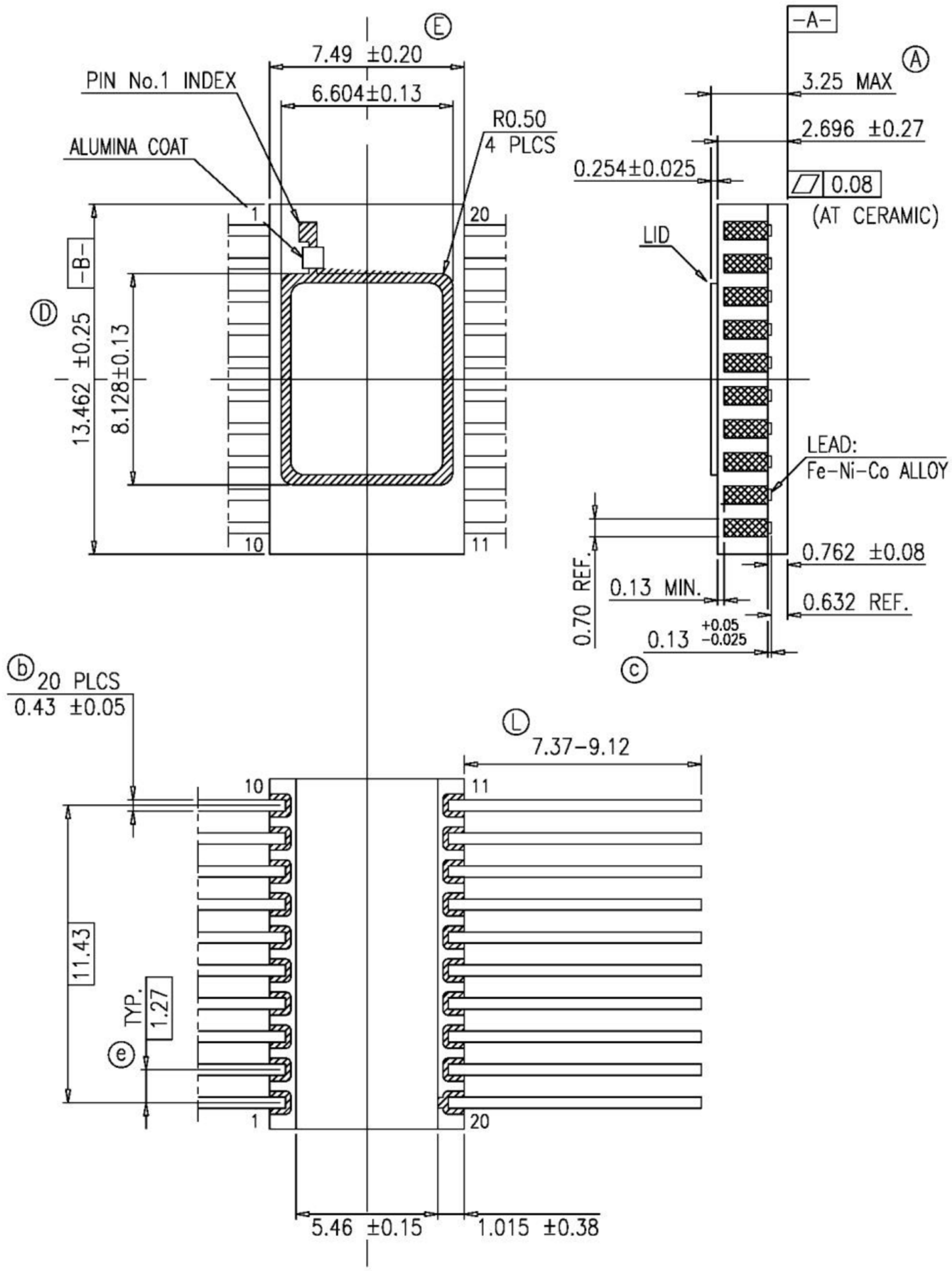


Figure 6: 20-Lead Flatpack

Notes:

1) The Lid Is Connected to VSS.
2) Dimensions are in Millimeters.

Ordering Information

Generic Datasheet Part Numbering

UTxxxxx * * * *

Lead Finish: (Notes: 1, 2)
(A) = Hot Solder Dipped or Tinned
(C) = Gold
(X) = Factory options (gold or solder)

Screening Level: (Notes: 3, 4)
(P) = Prototype Flow (Temperature Range: 25°C only)
(C) = HiRel Flow (Temperature Range: -55°C to +125°C)

Case Outline:
(U) = 20-lead Flatpack

Access Time:
(-) =

54BS3245

Notes:

1) Lead finish (A, C, F, or X) must be specified.
2) If an "X" is specified when ordering, then the part marking will match the lead finish applied to the device shipped
3) Prototype Flow per CAES Manufacturing Flows Document. Lead finish is Factory Option "C" only. Radiation is neither tested nor guaranteed.
4) HiRel Flow per CAES Manufacturing Flows Document. Radiation TID tolerance may (or may not) be ordered.

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Ordering Information

SMD Part Numbering

5962 * ***** ** * * *

Lead Finish: (Note: 1)
(A) = Hot Solder Dipped or Tinned
(C) = Gold
(X) = Factory options (gold or solder)

Case Outline:
(X) = 20-Lead Ceramic Bottom-brazed Flatpack

QML/JAN Class:
(Q) = Class Q
(V) = Class V

Device Type:
(01) = UT54BS3245 (Temperature Range: -55C to +125C)

SMD Project Number:
(15244) = UT54BS3245 8-bit Bus Switch

Radiation Hardness Assurance: (Note: 2)
(R) = 100 krad (Si)
(F) = 300 krad (Si)

Federal Stock Class Designator

Notes:

1) Lead finish must be specified. If "X" is specified when ordering, the factory will determine lead finish. Part marking will reflect the lead finish applied to the device shipped.
2) A radiation hardness assurance level must be selected. The use of "-" indicates no radiation hardness assurance guarantee.

Revision History

Table 8: Revision History

Date	Rev. #	Change Description	Initials
05/01/2016	1.0.0	Updated datasheet to reflect CAES logo, colors, and modified format. Updated the following specifications: R_{ON}, I_{IA}, I_{DD}, I_{DDQ}, T_{EN}, and T_{DIS}.	MM
06/23/2016	2.0.0	Released Datasheet. Updated capacitance, propagation delay, and minor formatting.	BM
6/30/2016	2.0.1	FEATURES: 20-Lead Flatpack; IDDQ: CONDITIONS: /EN=VDD	BM
01/04/2017	2.0.2	FEATURES: QML Q, V compliant part	BM
09/12/2019	2.0.3	Package Pinout Diagram, Fig. 2, p.3 - Error Correction: Pins 11-14	BM
08/19/2021	2.0.5	ROC Table, p.4: Input t_R, t_F parameter updates.	BM

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Datasheet Definitions

	DEFINITION
Advanced Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet **is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final**.
Preliminary Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

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