

# UT54ACS85/UT54ACTS85

## Features

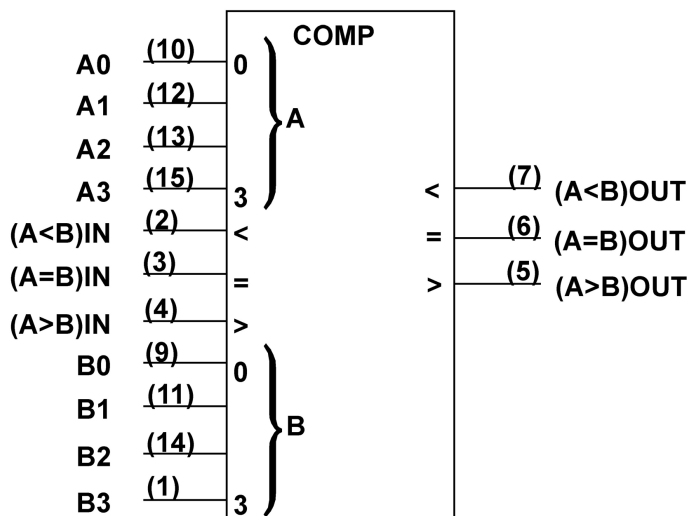
- 1.2μ CMOS
  - Latchup immune
- High speed
- Low power consumption
- Single 5 volt supply
- Available QML Q or V processes
- Flexible package
  - 16-pin DIP
  - 16-lead flatpack
- UT54ACS85 - SMD 5962-96536
- UT54ACTS85 - SMD 5962-96537

## Description

The UT54ACS85 and the UT54ACTS85 are 4-bit magnitude comparators that perform comparison of straight binary and straight BCD (8-4-2-1) codes. Three fully decoded decisions about two 4-bit words (A, B) are made and are externally available at three outputs. Devices are fully expandable to any number of bits without external gates. The cascading paths of the devices are implemented with only a two-gate-level delay to reduce overall comparison times for long words. An alternate method of cascading which further reduces the comparison time is shown in the typical application data.

The devices are characterized over full military temperature range of -55°C to +125°C.

## Logic Symbol

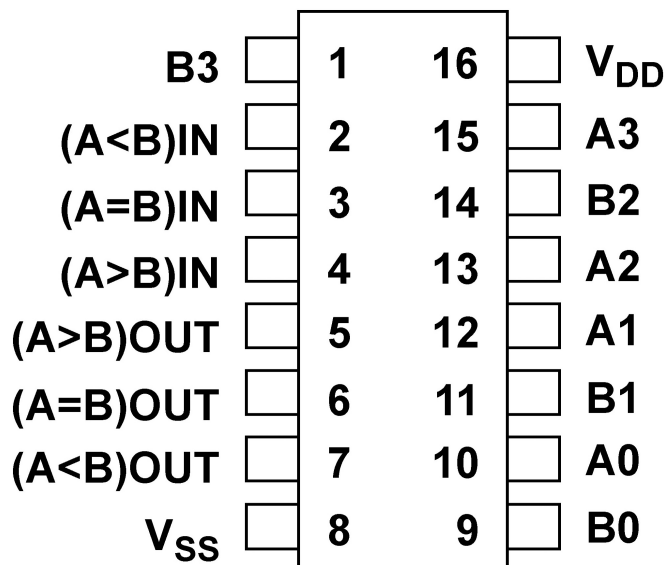


**Note:**

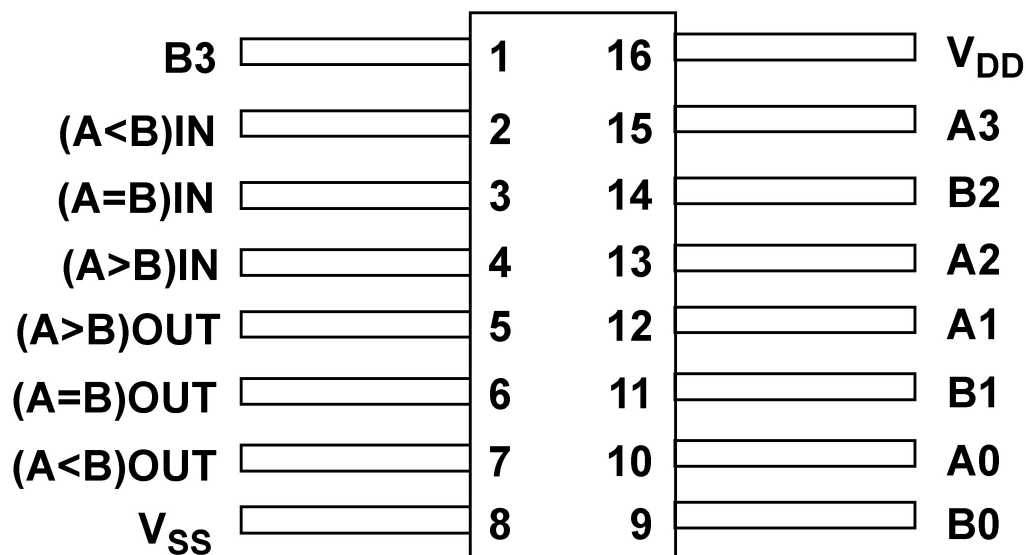
- 1) Logic symbol in accordance with ANSI/IEEE standard 91-1984 and IEC Publication 617-12.

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## Pinouts



16-Pin DIP  
Top View



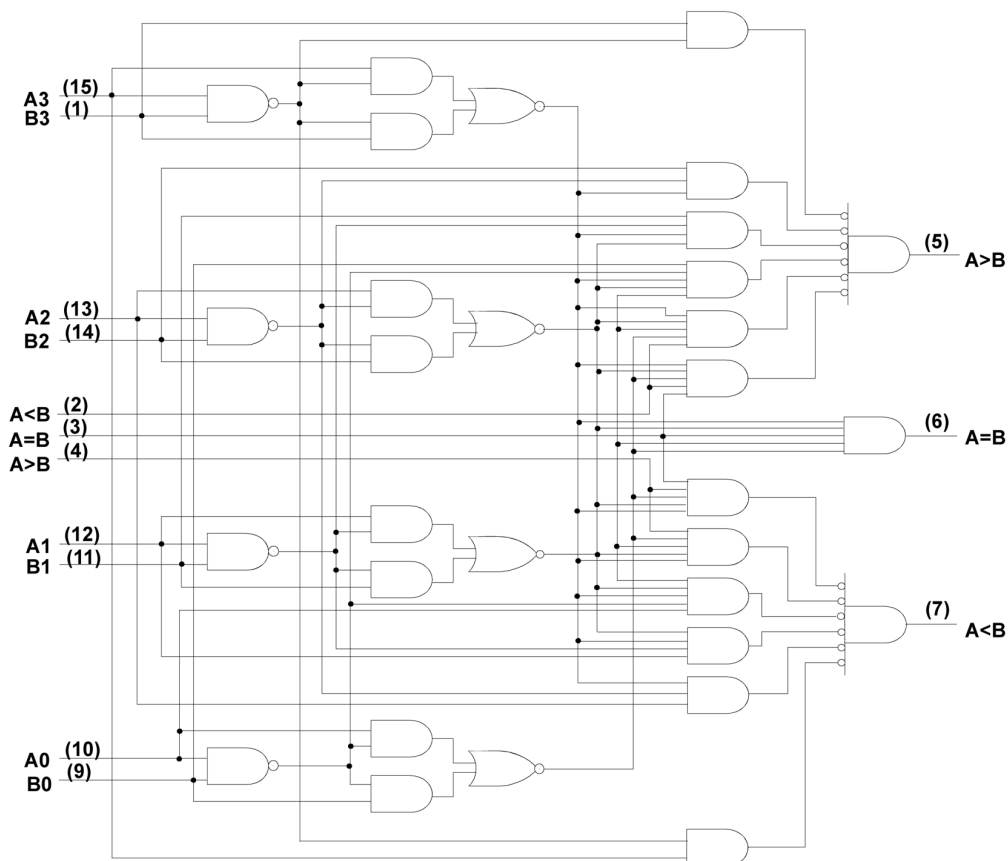
16-Lead Flatpack  
Top View

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## Function Table

Comparing Inputs				Cascading Inputs			Outputs		
A3, B3	A2, B2	A1, B1	A0, B0	A>B	A<B	A=B	A>B	A<B	A=B
A3>B3	X	X	X	X	X	X	H	L	L
A3<B3	X	X	X	X	X	X	L	H	L
A3=B3	A2>B2	X	X	X	X	X	H	L	L
A3=B3	A2<B2	X	X	X	X	X	L	H	L
A3=B3	A2=B2	A1>B1	X	X	X	X	H	L	L
A3=B3	A2=B2	A1<B1	X	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	H	L	L
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	H	L	L	H	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	H	L	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	X	X	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	H	H	L	L	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	L	H	H	L

## Logic Diagram



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## Operational Environment<sup>1</sup>

Parameter	Limit	Units
Total Dose	1.0E6	rads(Si)
SEU Threshold <sup>2</sup>	80	MeV-cm <sup>2</sup> /mg
SEL Threshold	120	MeV-cm <sup>2</sup> /mg
Neutron Fluence	1.0E14	n/cm <sup>2</sup>

**Notes:**

- 1) Logic will not latchup during radiation exposure within the limits defined in the table.
- 2) Device storage elements are immune to SEU affects.

## Absolute Maximum Ratings

Symbol	Parameter	Limit	Units
V <sub>DD</sub>	Supply voltage	-0.3 to 7.0	V
V <sub>I/O</sub>	Voltage any pin	-.3 to V <sub>DD</sub> +.3	V
T <sub>STG</sub>	Storage Temperature range	-65 to +150	°C
T <sub>J</sub>	Maximum junction temperature	+175	°C
T <sub>LS</sub>	Lead temperature (soldering 5 seconds)	+300	°C
Θ <sub>JC</sub>	Thermal resistance junction to case	20	°C/W
I <sub>I</sub>	DC input current	±10	mA
P <sub>D</sub>	Maximum power dissipation	1	W

**Note:**

- 1) Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Recommended Operating Conditions

Symbol	Parameter	Limit	Units
V <sub>DD</sub>	Supply voltage	4.5 to 5.5	V
V <sub>IN</sub>	Input voltage any pin	0 to V <sub>DD</sub>	V
T <sub>C</sub>	Temperature range	-55 to + 125	°C

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## DC Electrical Characteristics <sup>7</sup>

( $V_{DD} = 5.0V \pm 10\%$ ;  $V_{SS} = 0V$  <sup>6</sup>,  $-55^{\circ}C < T_C < +125^{\circ}C$ ); Unless otherwise noted,  $T_C$  is per the temperature range ordered.

Symbol	Parameter	Condition	MIN	MAX	Unit
$V_{IL}$	Low-level input voltage <sup>1</sup> ACTS ACS			0.8 .3 $V_{DD}$	V
$V_{IH}$	High-level input voltage <sup>1</sup> ACTS ACS		.5 $V_{DD}$ .7 $V_{DD}$		V
$I_{IN}$	Input leakage current ACTS/ACS	$V_{IN} = V_{DD}$ or $V_{SS}$	-1	1	$\mu A$
$V_{OL}$	Low-level output voltage <sup>3</sup> ACTS ACS	$I_{OL} = 8.0mA$ $I_{OL} = 100\mu A$		0.40 0.25	V
$V_{OH}$	High-level output voltage <sup>3</sup> ACTS ACS	$I_{OH} = -8.0mA$ $I_{OH} = -100\mu A$	.7 $V_{DD}$ $V_{DD} - 0.25$		V
$I_{OS}$	Short-circuit output current <sup>2,4</sup> ACTS/ACS	$V_O = V_{DD}$ and $V_{SS}$	-200	200	mA
$I_{OL}$	Output current <sup>10</sup> (Sink)	$V_{IN} = V_{DD}$ or $V_{SS}$ $V_{OL} = 0.4V$	8		mA
$I_{OH}$	Output current <sup>10</sup> (Source)	$V_{IN} = V_{DD}$ or $V_{SS}$ $V_{OH} = V_{DD} - 0.4V$	-8		mA
$P_{total}$	Power dissipation <sup>2, 8, 9</sup>	$C_L = 50pF$		2.3	mW/ MHz
$I_{DDQ}$	Quiescent Supply Current	$V_{DD} = 5.5V$		10	$\mu A$
$\Delta I_{DDQ}$	Quiescent Supply Current Delta ACTS	For input under test $V_{IN} = V_{DD} - 2.1V$ For all other inputs $V_{IN} = V_{DD}$ or $V_{SS}$ $V_{DD} = 5.5V$		1.6	mA
$C_{IN}$	Input capacitance <sup>5</sup>	$f = 1MHz @ 0V$		15	pF
$C_{OUT}$	Output capacitance <sup>5</sup>	$f = 1MHz @ 0V$		15	pF

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**Notes:**

- 1) Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions:  $V_{IH} = V_{IH(min)} + 20\%$ ,  $- 0\%$ ;  $V_{IL} = V_{IL(max)} + 0\%$ ,  $- 50\%$ , as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to  $V_{IH(min)}$  and  $V_{IL(max)}$ .
- 2) Supplied as a design limit but not guaranteed or tested.
- 3) Per MIL-PRF-38535, for current density  $\leq 5.0E5$  amps/cm<sup>2</sup>, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765 pF/MHz.
- 4) Not more than one output may be shorted at a time for maximum duration of one second.
- 5) Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and  $V_{SS}$  at frequency of 1MHz and a signal amplitude of 50mV rms maximum
- 6) All specifications valid for radiation dose  $\leq 1E6$  rads(Si).
- 7) Maximum allowable relative shift equals 50mV.
- 8) Power does not include power contribution of any TTL output sink current.
- 9) Power dissipation specified per switching output.
- 10) This value is guaranteed based on characterization data, but not tested.

## AC Electrical Characteristics <sup>2</sup>

( $V_{DD} = 5.0V \pm 10\%$ ;  $V_{SS} = 0V$  <sup>1</sup>,  $-55^{\circ}C < T_c < +125^{\circ}C$ ); unless otherwise noted,  $T_c$  is per the temperature range ordered.

Symbol	Parameter	Minimum	Maximum	Unit
$t_{PHL}$	An, Bn to (A<B) <sub>OUT</sub>	2	22	ns
$t_{PLH}$	An, Bn to (A<B) <sub>OUT</sub>	2	16	ns
$t_{PHL}$	An, Bn to (A=B) <sub>OUT</sub>	2	17	ns
$t_{PLH}$	An, Bn to (A=B) <sub>OUT</sub>	2	16	ns
$t_{PHL}$	An, Bn to (A>B) <sub>OUT</sub>	2	18	ns
$t_{PLH}$	An, Bn to (A>B) <sub>OUT</sub>	2	16	ns
$t_{PHL}$	(A<B) <sub>IN</sub> , (A=B) <sub>IN</sub> to (A>B) <sub>OUT</sub>	2	17	ns
$t_{PLH}$	(A<B) <sub>IN</sub> , (A=B) <sub>IN</sub> to (A>B) <sub>OUT</sub>	2	15	ns
$t_{PHL}$	(A=B) <sub>IN</sub> to (A=B) <sub>OUT</sub>	2	13	ns
$t_{PLH}$	(A=B) <sub>IN</sub> to (A=B) <sub>OUT</sub>	1	15	ns
$t_{PHL}$	(A>B) <sub>IN</sub> , (A=B) <sub>IN</sub> to (A<B) <sub>OUT</sub>	2	17	ns
$t_{PLH}$	(A>B) <sub>IN</sub> , (A=B) <sub>IN</sub> to (A<B) <sub>OUT</sub>	2	15	ns

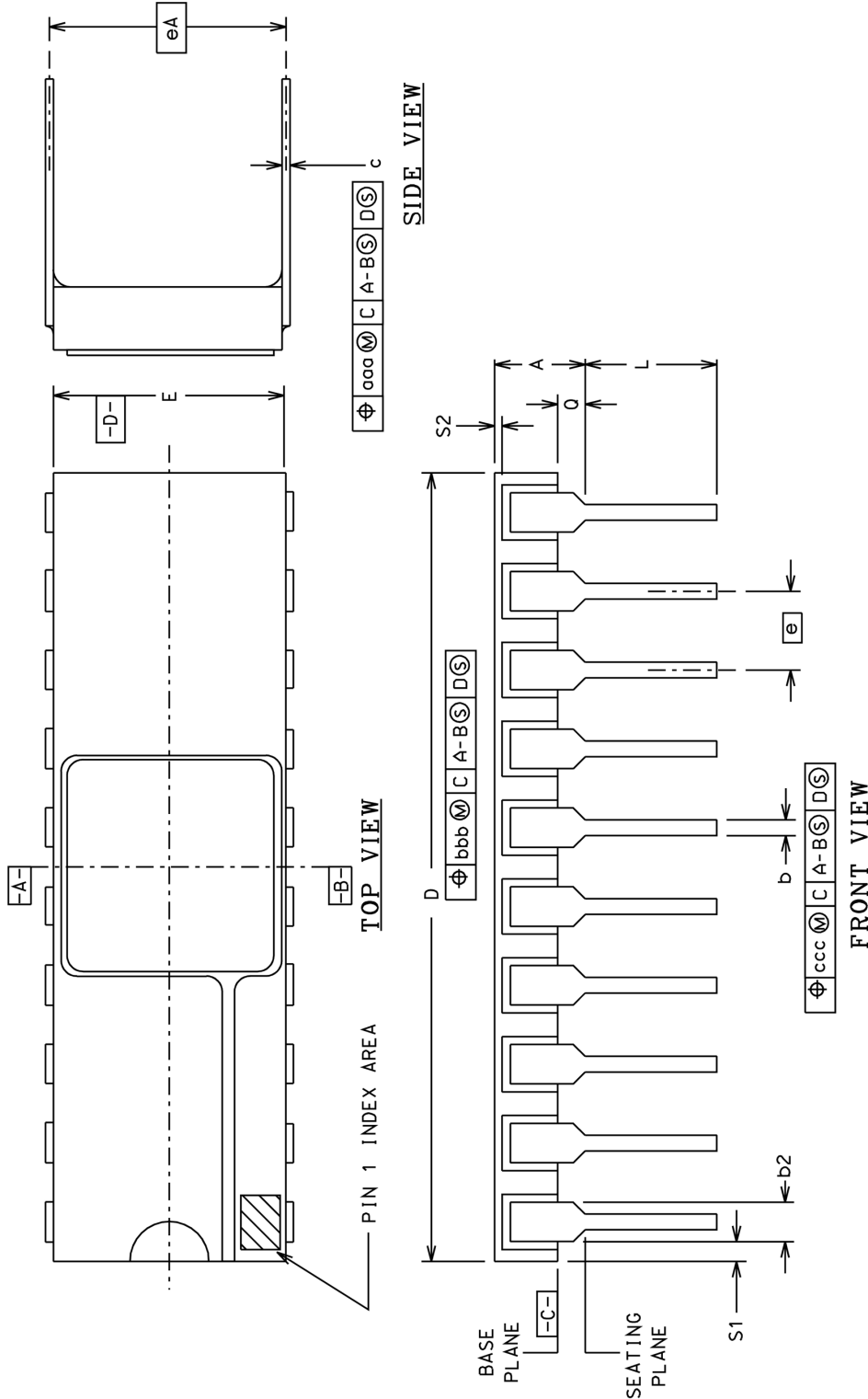
**Notes:**

- 1) Maximum allowable relative shift equals 50mV.
- 2) All specifications valid for radiation dose  $\leq 1E6$  rads(Si)

# UT54ACS85/UT54ACTS85

## Packaging

### Side-Brazed Packages

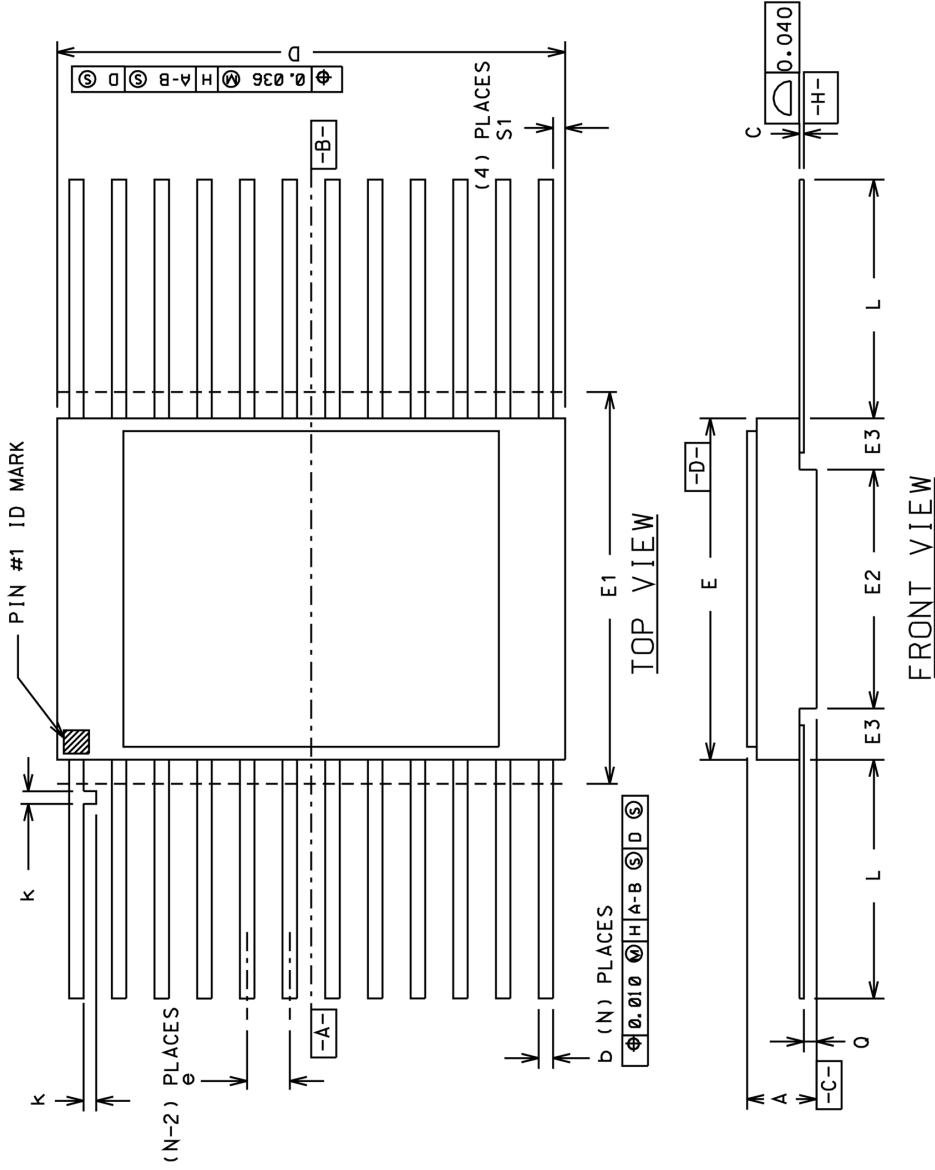


PKG. CONF IG	LEAD COUNT	MIL-STD-1835 DWG CONF C	A	b	b2	c	D	E	e	eA	L	Q	S1	S2	aaa	bbb	ccc
-01	14	D-1	0.200	0.026	0.065	0.018	0.785	0.310	0.100	0.300	0.200	0.060	0.005	0.005	0.015	0.030	0.010
-02	16	D-2	0.200	0.026	0.065	0.018	0.840	0.310	0.100	0.300	0.200	0.060	0.005	0.005	0.015	0.030	0.010
-03	20	D-8	0.200	0.026	0.065	0.018	1.060	0.310	0.100	0.300	0.200	0.070	0.005	0.005	0.015	0.030	0.010
			----	0.014	0.045	0.008	----	0.220	BSC	BSC	0.125	0.015	0.005	0.005	----	----	----

4-Bit Comparators

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Flatpack Packages

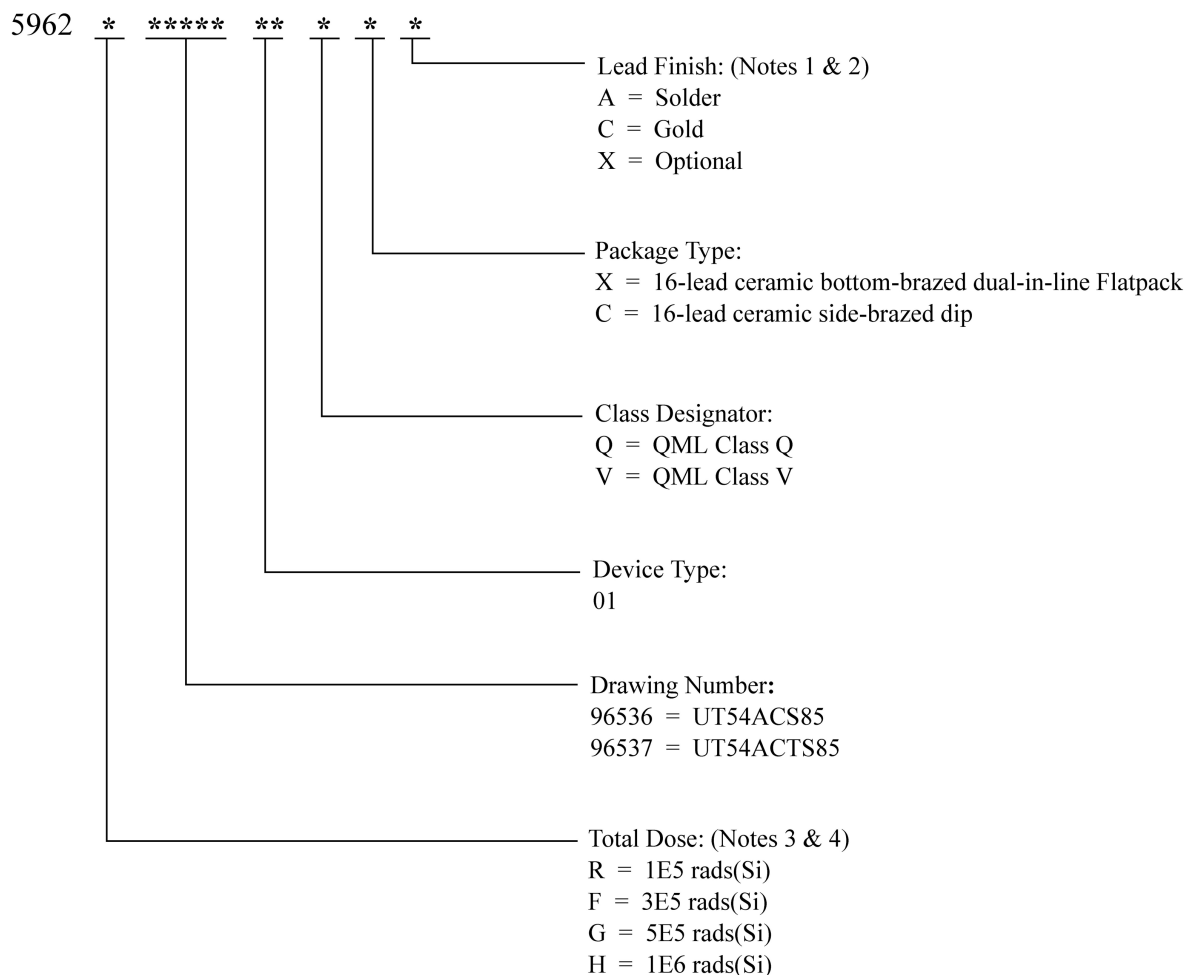


PKG CONFIG	LEAD COUNT	MIL-STD 1835 DWG CONF B	DIMENSION SYMBOLS													
			A	b	c	D	E	E1	E2	E3	e	k	L	Q	S1	
-03	14	F-2A	0.115 0.045	0.022 0.015	0.009 0.004	0.390 ---	0.260 0.235	0.290 ---	---	---	0.050 BSC	0.015 0.008	0.370 0.270	0.045 0.026	---	0.005
-04	16	F-5A	0.115 0.045	0.022 0.015	0.009 0.004	0.440 ---	0.285 0.245	0.315 ---	---	---	0.050 BSC	0.015 0.008	0.370 0.250	0.045 0.026	---	0.005
-05	20	F-9A	0.115 0.045	0.022 0.015	0.009 0.004	0.540 ---	0.300 0.245	0.330 ---	---	---	0.050 BSC	0.015 0.008	0.370 0.250	0.045 0.026	---	0.000



# UT54ACS85/UT54ACTS85

## UT54ACS85/UT54ACTS85: SMD



**Notes:**

- 1) Lead finish (A,C, or X) must be specified.
- 2) If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
- 3) Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening. For prototype inquiries, contact factory.
- 4) Device type 02 is only offered with a TID tolerance guarantee of 3E5 rads(Si) or 1E6 rads(Si) and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A and section 3.11.2. Device type 03 is only offered with a TID tolerance guarantee of 1E5 rads(Si), 3E5 rads(Si), and 5E5 rads(Si), and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A.

# UT54ACS85/UT54ACTS85

## Datasheet Definitions

	DEFINITION
Advanced Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet <b>is subject to change</b> . Specifications can be <b>TBD</b> and the part package and pinout are <b>not final</b> .
Preliminary Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

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