DATASHEET

RELEASED 12/16/11

Octal D-Flip-Flops with Clear

UT54ACS273/UT54ACTS273

Features

- Contains eight flip-flops with single-rail outputs
- Buffered clock and direct clear inputs
- Individual data input to each flip-flop
- Applications include:
  - Buffer/storage registers, shift registers, and pattern generators
- 1.2µ CMOS
  - Latchup immune
- High speed
- Low power consumption
- Single 5 volt supply
- Available QML Q or V processes
- Flexible package
  - 20-pin DIP
  - 20-lead flatpack
- UT54ACS273 - SMD 5962-96578
- UT54ACTS273 - SMD 5962-96579

Description

The UT54ACS273 and the UT54ACTS273 are positive-edge-triggered D-type flip-flops with a direct clear input.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

The devices are characterized over full military temperature range of -55°C to +125°C.

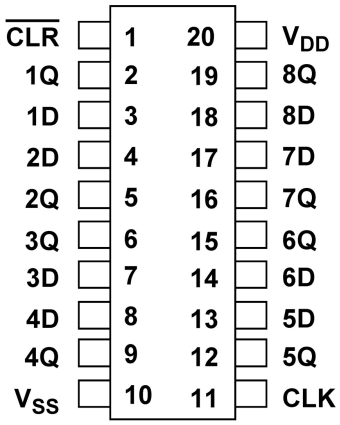
Function Table

Inputs			Outputs
$\overline{CLR}$	CLK	D_X	Q_X
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	No change

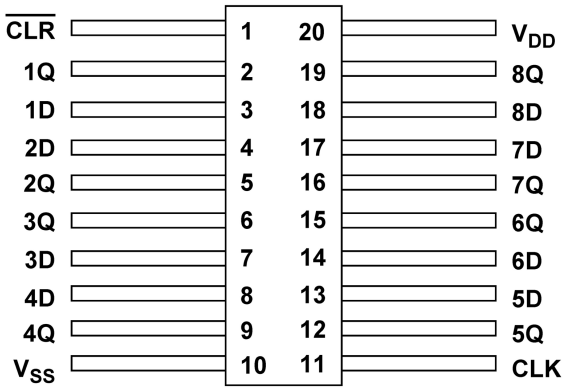
Octal D-Flip-Flops with Clear

UT54ACS273/UT54ACTS273

Pinouts

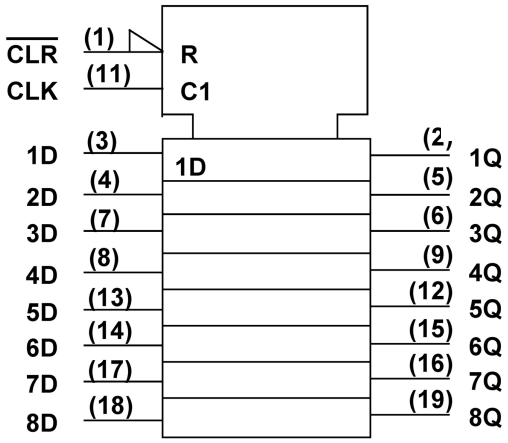


20-Pin DIP
Top View



20-Lead Flatpack
Top View

Logic Symbol



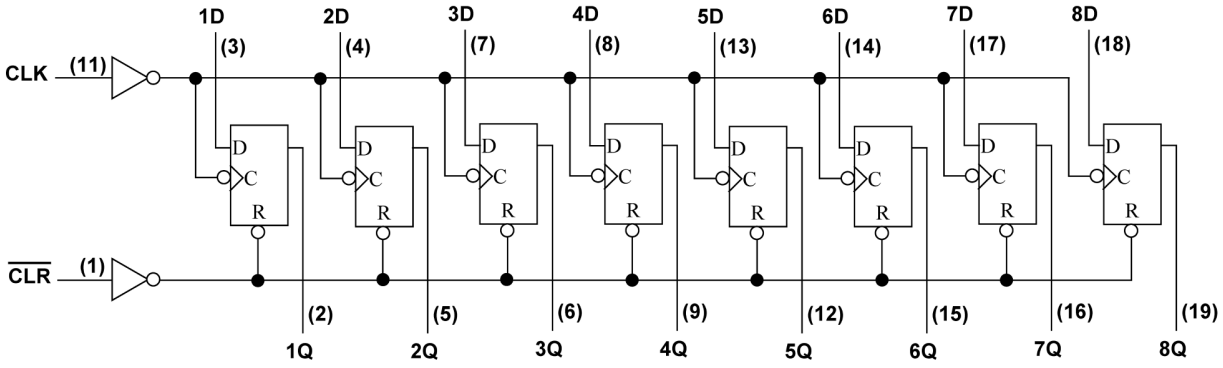
Note:

1) Logic symbol in accordance with ANSI/IEEE standard 91-1984 and IEC Publication 617-12.

Octal D-Flip-Flops with Clear

UT54ACS273/UT54ACTS273

Logic Diagram



Operational Environment [1]

Parameter	Limit	Units
Total Dose	1.0E6	rads(Si)
SEU Threshold [2]	80	MeV-cm^2/mg
SEL Threshold	120	MeV-cm^2/mg
Neutron Fluence	1.0E14	n/cm^2

Notes:

1) Logic will not latchup during radiation exposure within the limits defined in the table.
2) Device storage elements are immune to SEU affects.

Absolute Maximum Ratings

Symbol	Parameter	Limit	Units
V_{DD}	Supply voltage	-0.3 to 7.0	V
$V_{I/O}$	Voltage any pin	-.3 to V_{DD} +.3	V
T_{STG}	Storage Temperature range	-65 to +150	°C
T_J	Maximum junction temperature	+175	°C
T_{LS}	Lead temperature (soldering 5 seconds)	+300	°C
Θ_{JC}	Thermal resistance junction to case	20	°C/W
I_I	DC input current	±10	mA
P_D	Maximum power dissipation	1	W

Note:

1) Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other condition beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RELEASED 12/16/11

Octal D-Flip-Flops with Clear

UT54ACS273/UT54ACTS273

Recommended Operating Conditions

Symbol	Parameter	Limit	Units
V_{DD}	Supply voltage	4.5 to 5.5	V
V_{IN}	Input voltage any pin	0 to V_{DD}	V
T_C	Temperature range	-55 to + 125	°C

DC Electrical Characteristics [7]

(V_{DD} = 5.0V ±10%; V_{SS} = 0V [6], -55°C < T_C < +125°C); Unless otherwise noted, T_C is per the temperature range ordered.

Symbol	Parameter	Condition	MIN	MAX	Unit
V_{IL}	Low-level input voltage [1] ACTS ACS			0.8 .3V_{DD}	V
V_{IH}	High-level input voltage [1] ACTS ACS		.5V_{DD} .7V_{DD}		V
I_{IN}	Input leakage current ACTS/ACS	V_{IN} = V_{DD} or V_{SS}	-1	1	µA
V_{OL}	Low-level output voltage [3] ACTS ACS	I_{OL} = 8.0mA I_{OL} = 100µA		0.40 0.25	V
V_{OH}	High-level output voltage [3] ACTS ACS	I_{OH} = -8.0mA I_{OH} = -100 µA	.7V_{DD} V_{DD} - 0.25		V
I_{OS}	Short-circuit output current [2, 4] ACTS/ACS	V_O = V_{DD} and V_{SS}	-200	200	mA
I_{OL}	Output current [10] (Sink)	V_{IN} = V_{DD} or V_{SS} V_{OL} = 0.4V	8		mA
I_{OH}	Output current [10] (Source)	V_{IN} = V_{DD} or V_{SS} V_{OH} = V_{DD} - 0.4V	-8		mA
P_{total}	Power dissipation [2, 8, 9]	C_L = 50pF		1.9	mW/ MHz
I_{DDQ}	Quiescent Supply Current	V_{DD} = 5.5V		10	µA
ΔI_{DDQ}	Quiescent Supply Current Delta ACTS	For input under test V_{IN} = V_{DD} - 2.1V For all other inputs V_{IN} = V_{DD} or V_{SS} V_{DD} = 5.5V		1.6	mA
C_{IN}	Input capacitance [5]	f = 1MHz @ 0V		15	pF
C_{OUT}	Output capacitance [5]	f = 1MHz @ 0V		15	pF

Notes:

1) Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: $V_{IH} = V_{IH}(min) + 20\%, - 0\%$; $V_{IL} = V_{IL}(max) + 0\%, - 50\%$, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to $V_{IH}(min)$ and $V_{IL}(max)$.
2) Supplied as a design limit but not guaranteed or tested.
3) Per MIL-PRF-38535, for current density ≤ 5.0E5 amps/cm^2, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765 pF/MHz.
4) Not more than one output may be shorted at a time for maximum duration of one second.
5) Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz and signal amplitude of 50mV rms maximum.
6) Maximum allowable relative shift equals 50mV.
7) All specifications valid for radiation dose ≤ 1E6 rads(Si).
8) Power does not include power contribution of any TTL output sink current.
9) Power dissipation specified per switching output.
10) This value is guaranteed based on characterization data, but not tested.

AC Electrical Characteristics [2]

(V_{DD} = 5.0V ±10%; V_{SS} = 0V [6], -55°C < T_C < +125°C); Unless otherwise noted, T_C is per the temperature range ordered.

Symbol	Parameter	Minimum	Maximum	Unit
t_{PLH}	CLK to Q	4	17	ns
t_{PHL}	CLK to Q	4	19	ns
t_{PHL}	$\overline{CLR}$ to Q	5	19	ns
f_{MAX}	Maximum clock frequency		63	MHz
t_{SU1}	$\overline{CLR}$ inactive setup time before CLK ↑	5		ns
t_{SU2}	Data setup time before CLK ↑	5		ns
t_H	Data hold time after CLK ↑	3		ns
t_W	Minimum pulse width $\overline{CLR}$ low CLK high CLK low	8		ns

Notes:

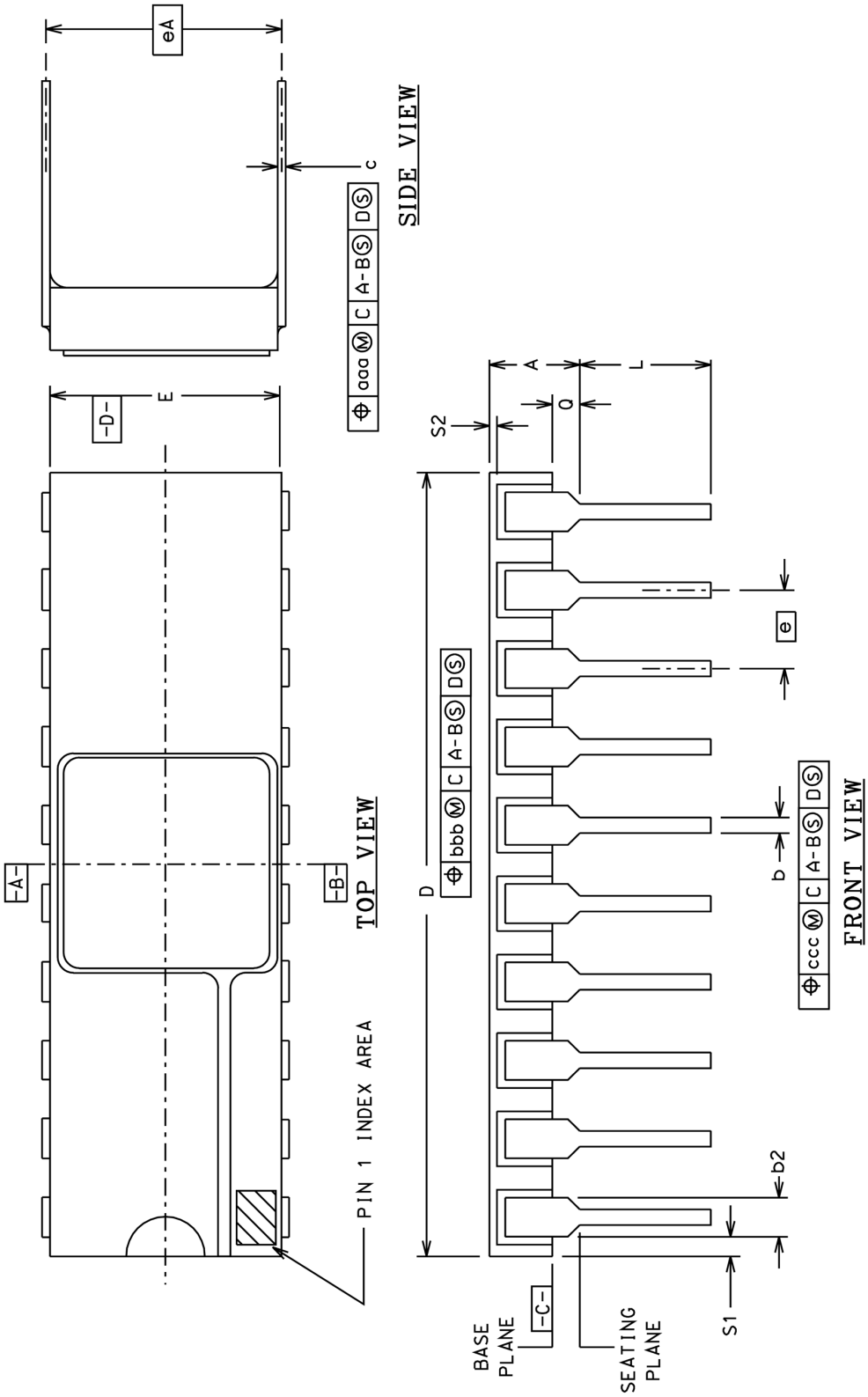
1) Maximum allowable relative shift equals 50mV.
2) All specifications valid for radiation dose ≤ 1E6 rads(Si).

Octal D-Flip-Flops with Clear

UT54ACS273/UT54ACTS273

Packaging

Side-Brazed Packages



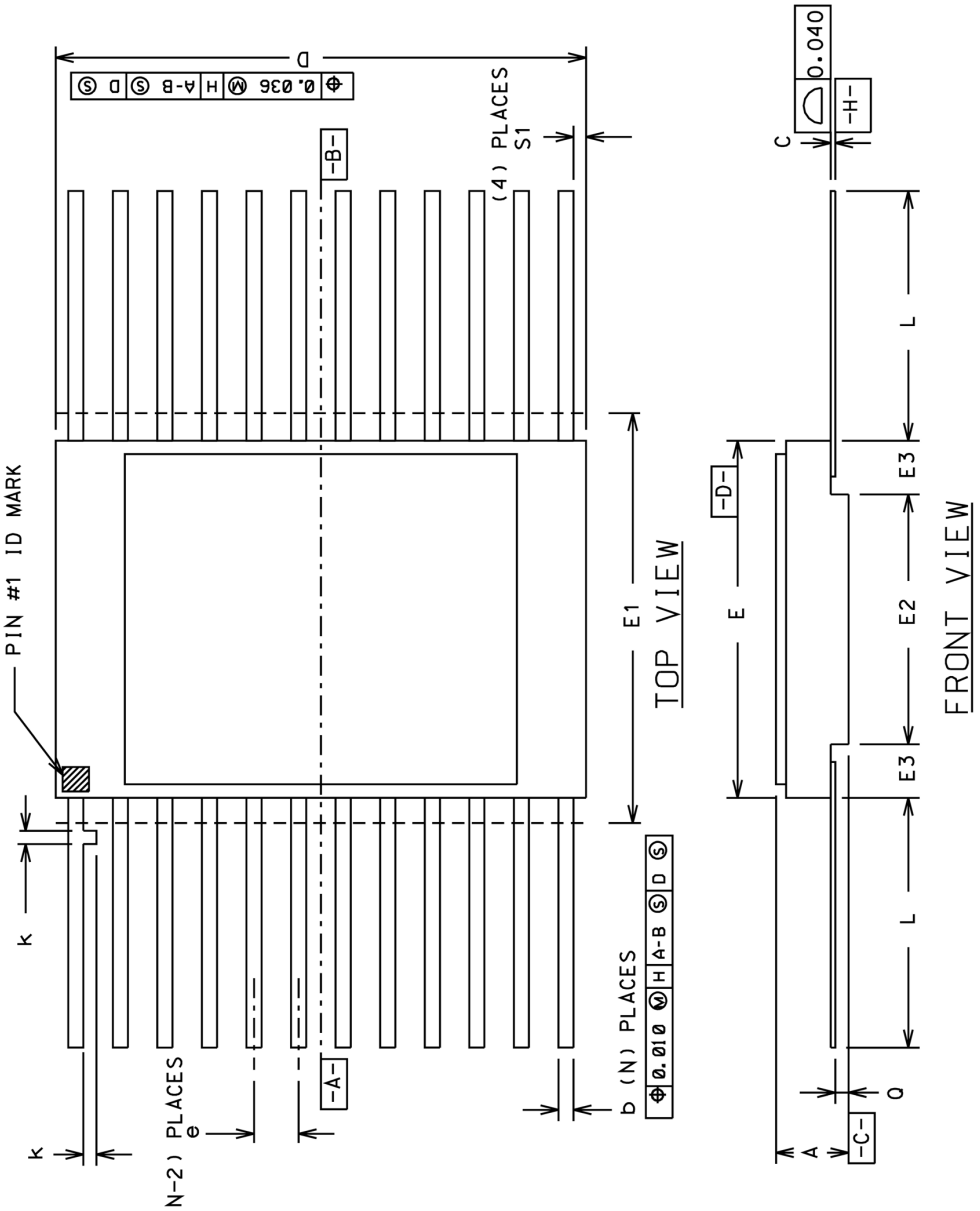
DIMENSION SYMBOLS

PKG CONFIG	LEAD COUNT	MIL-STD-1835 DWG CONF C	A	b	b2	c	D	E	e	eA	L	Q	S1	S2	aaa	bbb	ccc
-01	14	D-1	0.200 MAX	0.026 0.014	0.065 0.045	0.018 0.008	0.785 MAX	0.310 0.220	0.100 BSC	0.300 BSC	0.200 0.125	0.060 0.015	0.005 MAX	0.005 MAX	0.015 MAX	0.030 MAX	0.010 MAX
-02	16	D-2	0.200 MAX	0.026 0.014	0.065 0.045	0.018 0.008	0.840 MAX	0.310 0.220	0.100 BSC	0.300 BSC	0.200 0.125	0.060 0.015	0.005 MAX	0.005 MAX	0.015 MAX	0.030 MAX	0.010 MAX
-03	20	D-8	0.200 MAX	0.026 0.014	0.065 0.045	0.018 0.008	1.060 MAX	0.310 0.220	0.100 BSC	0.300 BSC	0.200 0.125	0.070 0.015	0.005 MAX	0.005 MAX	0.015 MAX	0.030 MAX	0.010 MAX

Octal D-Flip-Flops with Clear

UT54ACS273/UT54ACTS273

Flatpack Packages

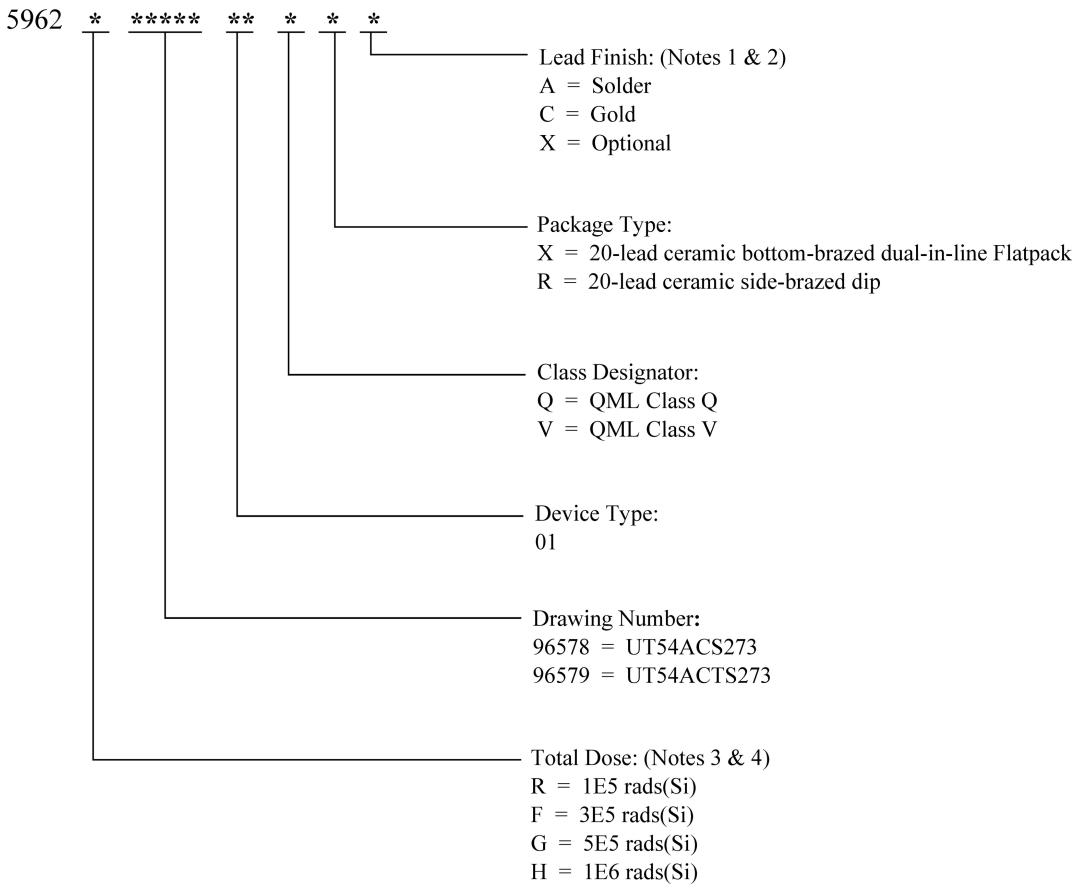


PKG CONFIG	LEAD COUNT	MIL-STD 1835 DWG CONF B	DIMENSION SYMBOLS															
			A	b	c	D	E	E1	E2	E3	e	k	L	Q	S1
-03	14	F-2A	0.115 0.045	0.022 0.015	0.009 0.004	0.390 -----	0.260 0.235	0.290 -----	----- 0.130	----- 0.030	0.050 BSC	0.015 0.008	0.370 0.270	0.045 0.026	----- 0.005
-04	16	F-5A	0.115 0.045	0.022 0.015	0.009 0.004	0.440 -----	0.285 0.245	0.315 -----	----- 0.130	----- 0.030	0.050 BSC	0.015 0.008	0.370 0.250	0.045 0.026	----- 0.005
-05	20	F-9A	0.115 0.045	0.022 0.015	0.009 0.004	0.540 -----	0.300 0.245	0.330 -----	----- 0.130	----- 0.030	0.050 BSC	0.015 0.008	0.370 0.250	0.045 0.026	----- 0.000

Octal D-Flip-Flops with Clear

UT54ACS273/UT54ACTS273

UT54ACS273/UT54ACTS273: SMD



Notes:

1) Lead finish (A,C, or X) must be specified.
2) If an "X" is specified when ordering, then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3) Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening. For prototype inquiries, contact factory.
4) Device type 02 is only offered with a TID tolerance guarantee of 3E5 rads(Si) or 1E6 rads(Si) and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A and section 3.11.2. Device type 03 is only offered with a TID tolerance guarantee of 1E5 rads(Si), 3E5 rads(Si), and 5E5 rads(Si), and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A.

DATASHEET

RELEASED 12/16/11

Octal D-Flip-Flops with Clear

UT54ACS273/UT54ACTS273

Datasheet Definitions

	DEFINITION
Advanced Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet **is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final**.
Preliminary Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

The following United States (U.S.) Department of Commerce statement shall be applicable if these commodities, technology, or software are exported from the U.S.: These commodities, technology, or software were exported from the United States in accordance with the Export Administration Regulations. Diversion contrary to U.S. law is prohibited.