DATASHEET

RELEASED 1/18

Synchronous 4-Bit Up-Down Dual Clock Counters

UT54ACS193/UT54ACTS193

Features

- Look-ahead circuitry enhances cascaded counters
- Fully synchronous in count modes
- Parallel asynchronous load for modulo-N count lengths
- Asynchronous clear
- 1.2µ CMOS (ACTS193) and.6µm CRH CMOS process (ACS193)
  - Latchup immune
- High speed
- Low power consumption
- Single 5 volt supply
- Available QML Q or V processes
- Flexible package
  - 16-pin DIP (ACTS only)
  - 16-lead flatpack
- UT54ACS193 - SMD 5962-96566
- UT54ACTS193 - SMD 5962-96567

Description

The UT54ACS193 and the UT54ACTS193 are synchronous 4-bit, binary reversible up-down binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when instructed. Synchronous operation eliminates the output counting spikes normally associated with asynchronous counters.

The outputs of the four flip-flops are triggered on a low-to-high-level transition of either count input (Up or Down). The direction of the counting is determined by which count input is pulsed while the other count input is high.

The counters are fully programmable. The outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the count pulses. Asynchronous loading allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided that forces all outputs to the low level when a high level is applied. The clear function is independent of the count and the load inputs.

The counter is designed for efficient cascading without the need for external circuitry. The borrow output ($\overline{BO}$) produces a low-level pulse while the count is zero and the down input is low. Similarly, the carry output ($\overline{CO}$) produces a low-level pulse while the count is maximum

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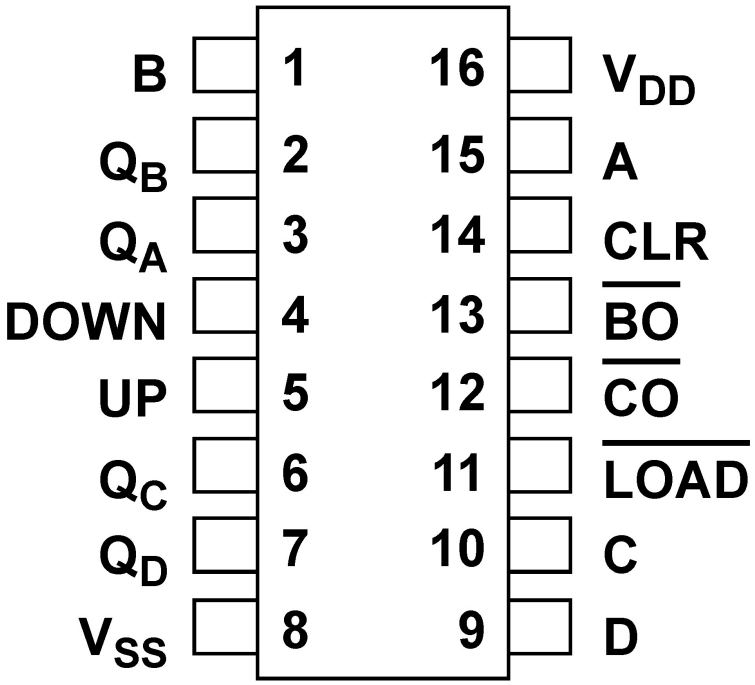
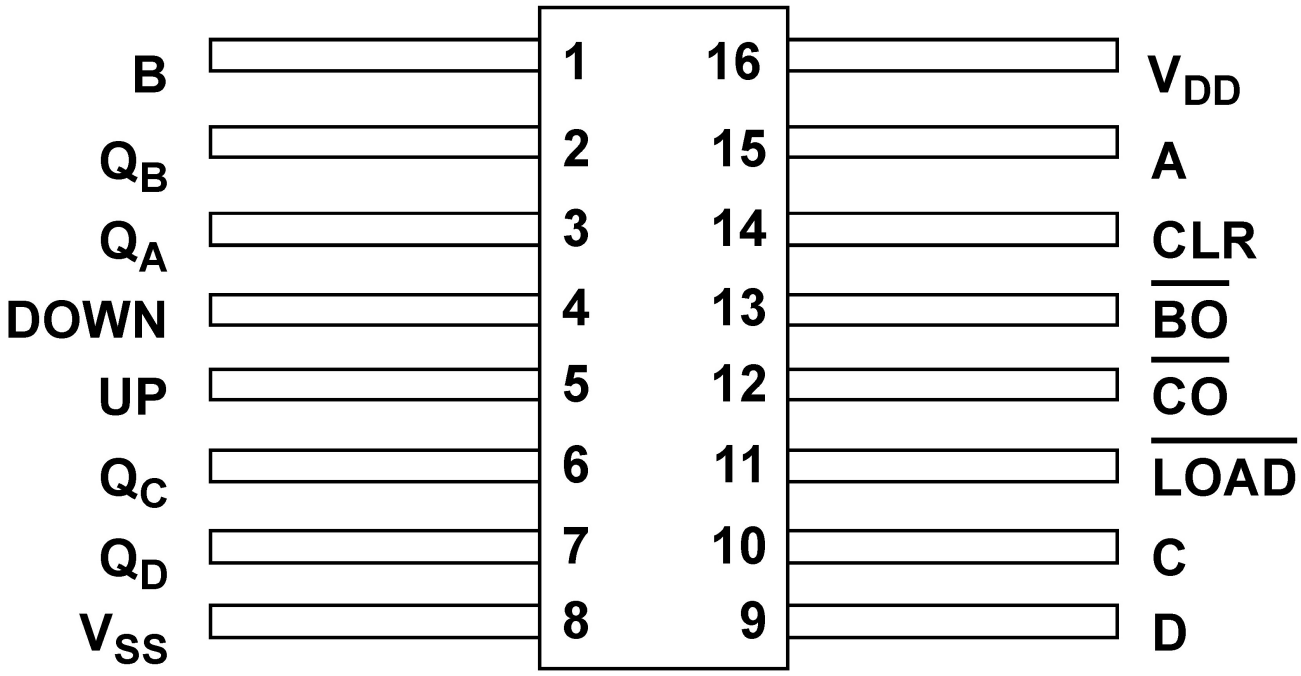
Pinout



16-Pin DIP
Top View



16-Lead Flatpack
Top View

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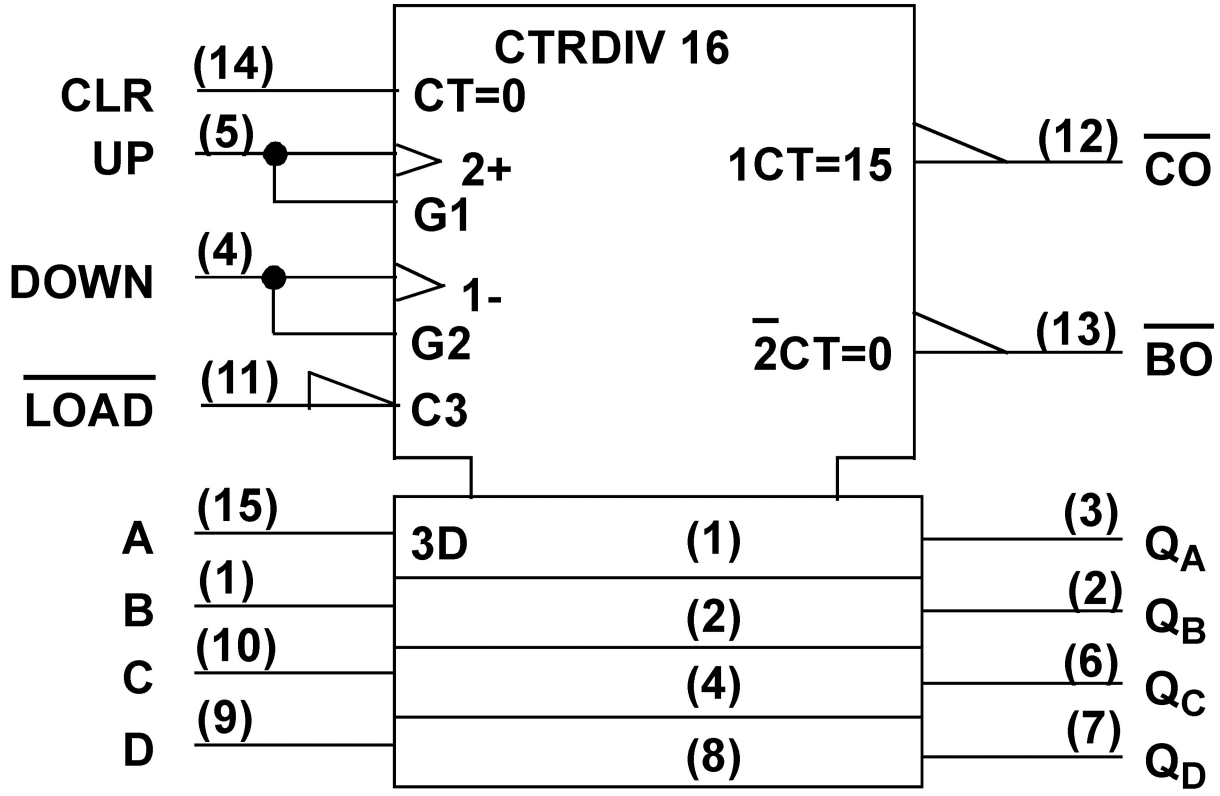
Function Table

Function	CLOCK UP	CLOCK DOWN	CLR	$\overline{\text{LOAD}}$
Count Up	↑	H	L	H
Count Down	H	↑	L	H
Reset	X	X	H	X
Load Preset Input	X	X	L	L

Logic Symbol



Note:

1) Logic symbol in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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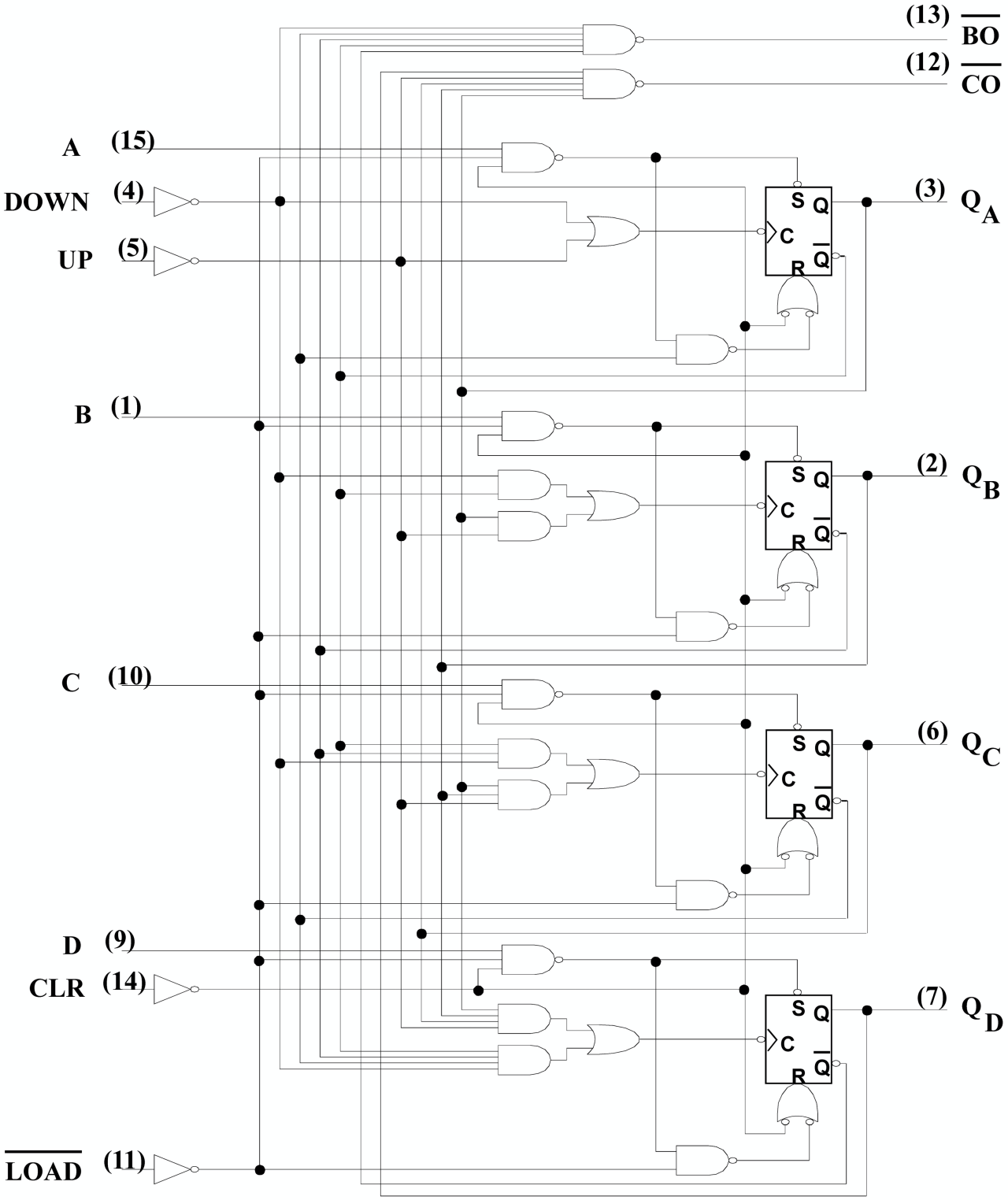
Logic Diagram



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Operational Environment[1]

Parameter	Limit	Units
Total Dose	1.0E6 (ACTS) 500K (ACS)	rads(Si)
SEU Threshold [2]	80	MeV-cm^2/mg
SEL Threshold	120	MeV-cm^2/mg
Neutron Fluence	1.0E14	n/cm^2

Notes:

1) Logic will not latchup during radiation exposure within the limits defined in the table.
2) Device storage elements are immune to SEU affects.

Absolute Maximum Ratings

Symbol	Parameter	Limit	Units
V_{DD}	Supply voltage	-0.3 to 7.0	V
$V_{I/O}$	Voltage any pin	-.3 to V_{DD} +.3	V
T_{STG}	Storage Temperature range	-65 to +150	°C
T_J	Maximum junction temperature	+175	°C
T_{LS}	Lead temperature (soldering 5 seconds)	+300	°C
Θ_{JC}	Thermal resistance junction to case	15.5	°C/W
I_I	DC input current	±10	mA
P_D	Maximum power dissipation	1	W

Note:

1) Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Limit	Units
V_{DD}	Supply voltage	4.5 to 5.5	V
V_{IN}	Input voltage any pin	0 to V_{DD}	V
T_C	Temperature range	-55 to + 125	°C

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DC Electrical Characteristics [7]

(V_{DD} = 5.0V±10%; V_{SS} = 0V [6]; -55°C < T_C < +125°C); Unless otherwise noted, Tc is per the temperature range ordered.

Symbol	Parameter		Condition	MIN	MAX	Unit
V_{IL}	Low-level input voltage [1] ACTS ACS				0.8 .3V_{DD}	V
V_{IH}	High-level input voltage [1] ACTS ACS			.5V_{DD} .7V_{DD}		V
I_{IN}	Input leakage current ACTS/ACS		V_{IN} = V_{DD} or V_{SS}	-1	1	µA
V_{OL}	Low-level output voltage [3] ACTS ACS		I_{OL} = 8.0mA I_{OL} = 100µA		0.40 0.25	V
V_{OH}	High-level output voltage [3] ACTS ACS		I_{OH} = -8.0mA I_{OH} = -100µA	.7V_{DD} V_{DD} - 0.25		V
I_{OS}	Short-circuit output current [2, 4] ACTS/ACS		V_O = V_{DD} and V_{SS}	-200	200	mA
I_{OL}	Output current [10] (Sink)		V_{IN} = V_{DD} or V_{SS} V_{OL} = 0.4V	8		mA
I_{OH}	Output current [10] (Source)		V_{IN} = V_{DD} or V_{SS} V_{OH} = V_{DD} - 0.4V	-8		mA
P_{total}	Power dissipation [2, 8, 9]		C_L = 50pF		2.1	mW/ MHz
I_{DDQ}	Quiescent Supply Current	Pre-Rad	V_{IN} = V_{DD} or V_{SS} V_{DD} = V_{DD} MAX		10	µA
		Post-Rad Device Type-01			50	
ΔI_{DDQ}	Quiescent Supply Current Delta ACTS		For input under test V_{IN} = V_{DD} - 2.1V For all other inputs V_{IN} = V_{DD} or V_{SS} V_{DD} = 5.5V		1.6	mA
C_{IN}	Input capacitance [5]		f = 1MHz @0V		15	pF
C_{OUT}	Output capacitance [5]		f = 1MHz @0V		15	pF

Notes:

1) Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: V_{IH} = V_{IH}(min) + 20%, -0%; V_{IL} = V_{IL}(max) + 0%, -50%, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to V_{IH}(min) and V_{IL}(max).
2) Supplied as a design limit but not guaranteed or tested.
3) Per MIL-PRF-38535, for current density ≤ 5.0E5 amps/cm^2, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765 pF/MHz.
4) Not more than one output may be shorted at a time for maximum duration of one second.
5) Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz and a signal amplitude of 50mV rms maximum.
6) Maximum allowable relative shift equals 50mV.
7) Device type 01 is only offered with a TID tolerance guarantee of 1E6 rads(Si) (ACTS only), 1E5 rads(Si), 3E5 rads(Si), and 5E5 rads(Si), and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A.
8) Power does not include power contribution of any TTL output sink current.

9) Power dissipation specified per switching output.
10) This value is guaranteed based on characterization data, but not tested.

AC Electrical Characteristics [2]

(V_{DD} = 5.0V ±10%; V_{SS} = 0V [6], -55°C < T_C < +125°C); Unless otherwise noted, Tc is per the temperature range ordered.

Symbol	Parameter	Minimum	Maximum	Unit
t_{PLH}	UP to Q_n	2	20	ns
t_{PHL}	UP to Q_n	2	24	ns
t_{PLH}	UP to $\overline{CO}$	2	13	ns
t_{PHL}	UP to $\overline{CO}$	2	16	ns
t_{PLH}	DOWN to $\overline{BO}$	2	13	ns
t_{PHL}	DOWN to $\overline{BO}$	2	16	ns
t_{PLH}	DOWN to Q_n	2	20	ns
t_{PHL}	DOWN to Q_n	2	24	ns
t_{PLH}	$\overline{LOAD}$ to Qn	2	22	ns
t_{PHL}	$\overline{LOAD}$ to Qn	2	23	ns
t_{PHL}	CLR to Q_n	2	22	ns
f_{MAX}	Maximum clock frequency		56	MHz
t_{SU1}	$\overline{LOAD}$ inactive setup time before UP or DOWN ↑	3		ns
t_{SU2}	CLR inactive setup time before UP or DOWN↑	3		ns
t_{SU3}	A, B, C, D setup time before $\overline{LOAD}$ ↑	6		ns
t_{H1}	UP high hold time after DOWN ↑	20		ns
t_{H2}	DOWN high hold time after UP ↑	20		ns
t_{H3} [3]	A, B, C, D hold time after $\overline{LOAD}$ ↑	2		ns
t_W	Minimum pulse width UP high or low DOWN high or low $\overline{LOAD}$ low CLR high	9		ns

Notes:

1) Maximum allowable relative shift equals 50mV.
2) Device type 01 is only offered with a TID tolerance guarantee of 1E6 rads(Si) (ACTS only), 1E5 rads(Si), 3E5 rads(Si), and 5E5 rads(Si), and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A.
3) Based on characterization, data hold time (t_{H3}) of 0ns can be assumed if data setup time (t_{SU3}) is ≥10ns. This is guaranteed, but not tested.

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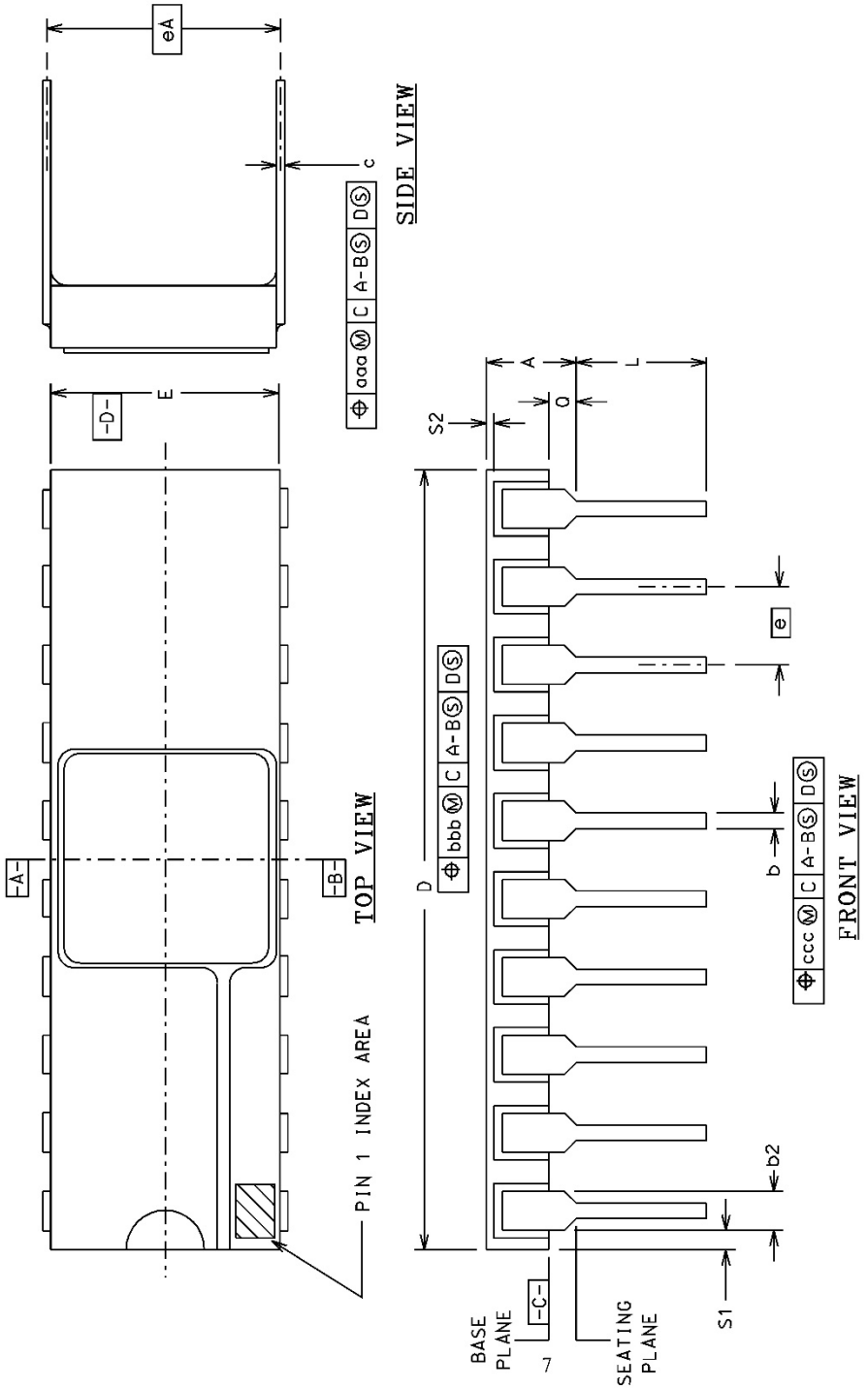
Packaging

Side-Brazed Packages



PKG CONFIG	LEAD COUNT	MIL-STD-1835 DWG CONF C	DIMENSION SYMBOLS																			
			A	b	b2	c	D	E	e	eA	L	Q	S1	S2	aaa	bbb	ccc
-01	14	D-1	0.200 MAX	0.026 0.014	0.065 0.045	0.018 0.008	0.785 MAX	0.310 0.220	0.100 BSC	0.300 BSC	0.200 0.125	0.060 0.015	MIN	MIN	0.015 MAX	0.030 MAX	0.010 MAX
-02	16	D-2	0.200 MAX	0.026 0.014	0.065 0.045	0.018 0.008	0.840 MAX	0.310 0.220	0.100 BSC	0.300 BSC	0.200 0.125	0.060 0.015	MIN	MIN	0.015 MAX	0.030 MAX	0.010 MAX
-03	20	D-8	0.200 MAX	0.026 0.014	0.065 0.045	0.018 0.008	1.060 MAX	0.310 0.220	0.100 BSC	0.300 BSC	0.200 0.125	0.070 0.015	MIN	MIN	0.015 MAX	0.030 MAX	0.010 MAX

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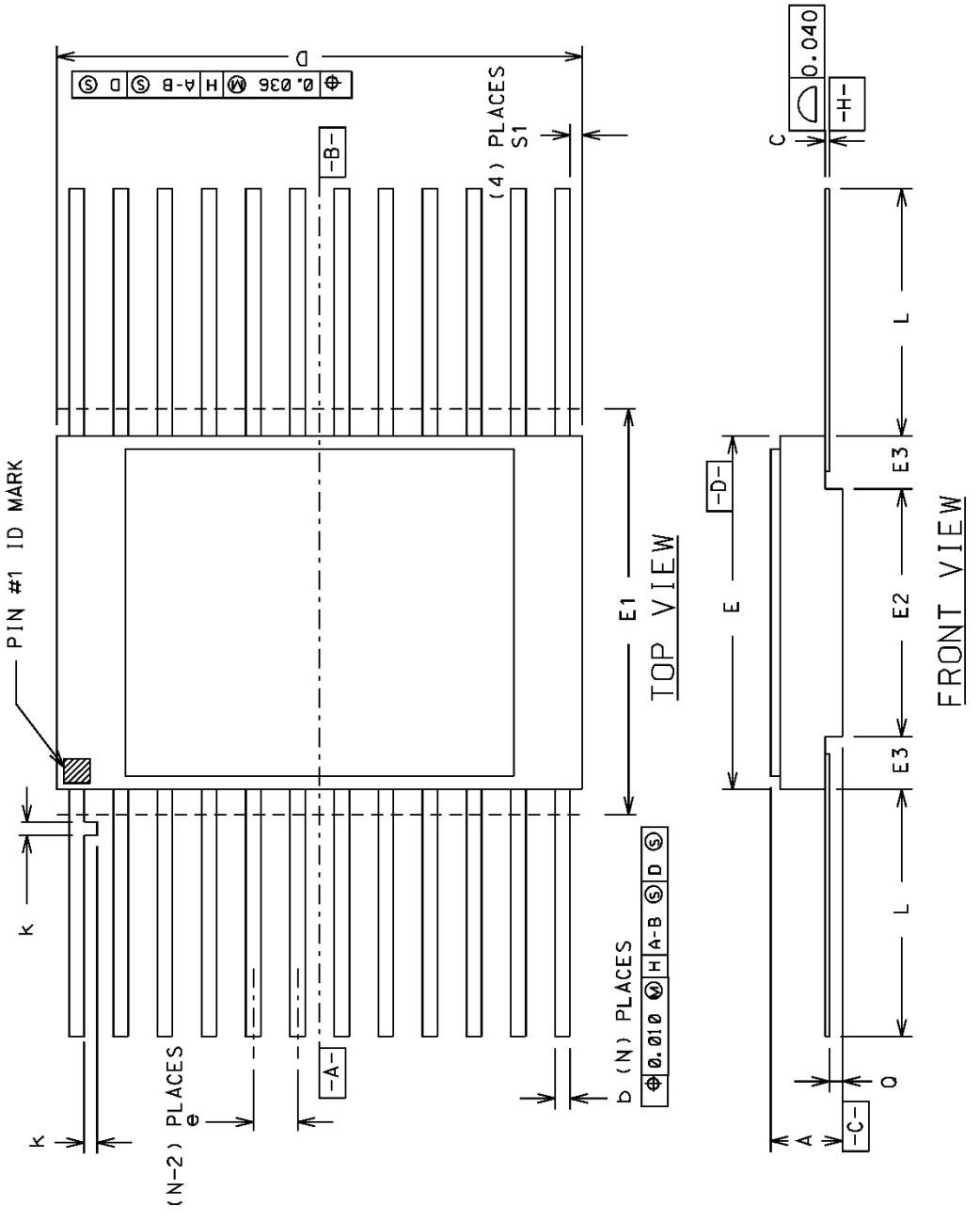
Flatpack Packages



PKG CONFIG	LEAD COUNT	MIL-STD 1835 DWG CONF B	DIMENSION SYMBOLS													
			A	b	c	D	E	E1	E2	E3	e	k	L	Q	S1
-03	14	F-2A	0.115 0.045	0.022 0.015	0.009 0.004	0.390 -----	0.260 0.235	0.290 -----	----- 0.130	----- 0.030	0.050 BSC	0.015 0.008	0.370 0.270	0.045 0.026	----- 0.005
-04	16	F-5A	0.115 0.045	0.022 0.015	0.009 0.004	0.440 -----	0.285 0.245	0.315 -----	----- 0.130	----- 0.030	0.050 BSC	0.015 0.008	0.370 0.250	0.045 0.026	----- 0.005
-05	20	F-9A	0.115 0.045	0.022 0.015	0.009 0.004	0.540 -----	0.300 0.245	0.330 -----	----- 0.130	----- 0.030	0.050 BSC	0.015 0.008	0.370 0.250	0.045 0.026	----- 0.000

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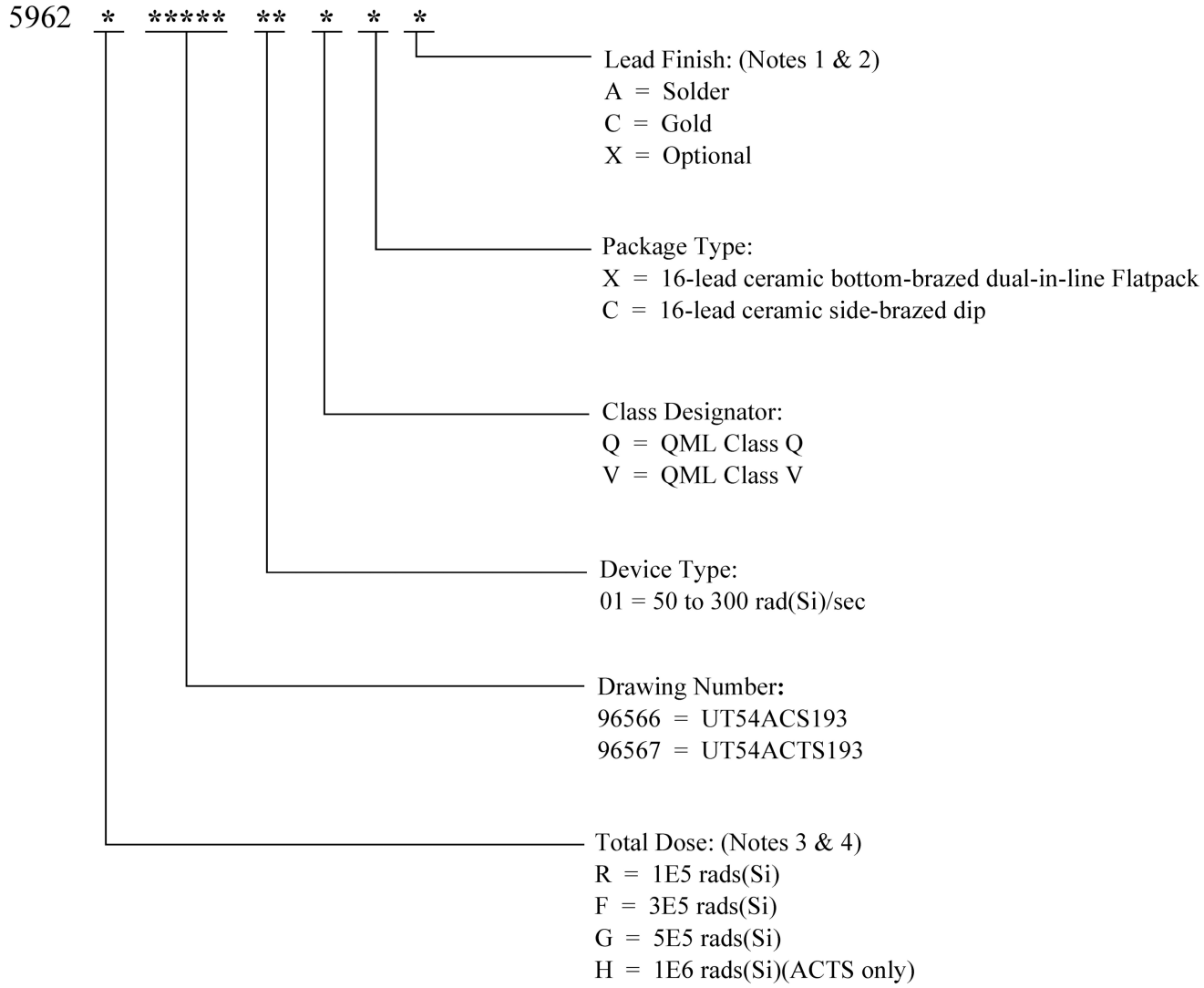
UT54ACS193/UT54ACTS193: SMD



Notes:

1) Lead finish (A,C, or X) must be specified.
2) If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3) Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening. For prototype inquiries, contact factory.
4) Device type 01 is only offered with a TID tolerance guarantee of 1E6 rads(Si) (ACTS only), 1E5 rads(Si), 3E5 rads(Si), and 5E5 rads(Si), and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A.

Data Sheet Revision History

Revision Date	Description of Change	Author
10-17	Page 6 edited IDDQ Applied new CAES Data Sheet template to the document.	RT
1-18	Updates to reflect current SMD	RT

DATASHEET

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Datasheet Definitions

	DEFINITION
Advanced Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet **is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final**.
Preliminary Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

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