

UT54ACS08/UT54ACTS08

Features

- 0.6 μ CRH CMOS
 - Latchup immune
- High speed
- Low power consumption
- Single 5 volt supply
- Available QML Q or V processes
- 14-lead flatpack
- UT54ACS08 - SMD 5962-96518
- UT54ACTS08 - SMD 5962-96519

Description

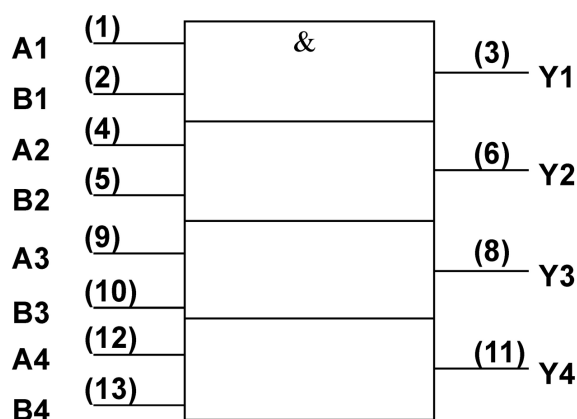
The UT54ACS08 and UT54ACTS08 are quadruple two-input AND gates. The circuits perform the Boolean functions $Y = A \cdot B$ or $Y = \overline{\overline{A} + \overline{B}}$ in positive logic.

The devices are characterized over full military temperature range of -55°C to +125°C.

Function Table

Input		Output
A	B	Y
H	H	H
L	X	L
X	L	L

Logic Symbol

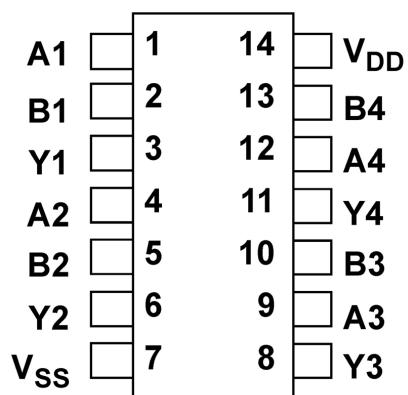


Note:

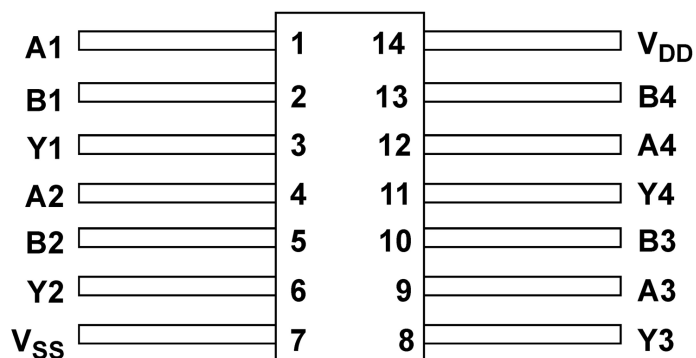
- 1) Logic symbol in accordance with ANSI/IEEE standard 91-1984 and IEC Publication 617-12.

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Pinouts

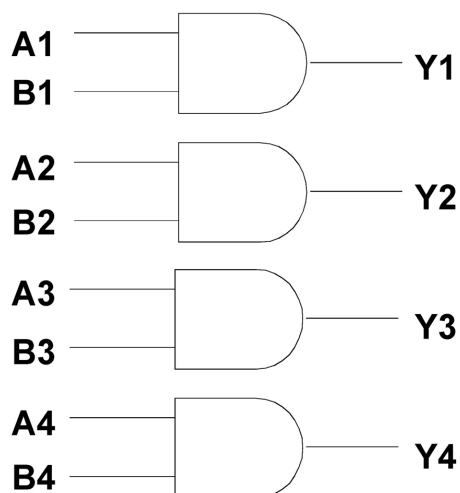


14-Pin DIP
Top View



14-Pin Flatpack
Top View

Logic Diagram



UT54ACS08/UT54ACTS08

Operational Environment ¹

Parameter	Limit	Units
Total Dose	500K	rads(Si)
SEU Threshold ²	80	MeV-cm ² /mg
SEL Threshold	120	MeV-cm ² /mg
Neutron Fluence	1.0E14	n/cm ²

Notes:

- 1) Logic will not latchup during radiation exposure within the limits defined in the table.
- 2) Device storage elements are immune to SEU affects.

Absolute Maximum Ratings

Symbol	Parameter	Limit	Units
V _{DD}	Supply voltage	-0.3 to 7.0	V
V _{I/O}	Voltage any pin	-.3 to V _{DD} +.3	V
T _{STG}	Storage Temperature range	-65 to +150	°C
T _J	Maximum junction temperature	+175	°C
T _{LS}	Lead temperature (soldering 5 seconds)	+300	°C
Θ _{JC}	Thermal resistance junction to case	15.5 (ACS) 15.0 (ACTS)	°C/W
I _I	DC input current	±10	mA
P _D	Maximum power dissipation	1	W

Note:

- 1) Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Limit	Units
V _{DD}	Supply voltage	4.5 to 5.5	V
V _{IN}	Input voltage any pin	0 to V _{DD}	V
T _C	Temperature range	-55 to + 125	°C

Quadruple 2-Input AND Gates

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DC Electrical Characteristics ⁷

($V_{DD} = 5.0V \pm 10\%$; $V_{SS} = 0V$ ⁶, $-55^{\circ}C < T_C < +125^{\circ}C$); Unless otherwise noted, T_C is per the temperature range ordered.

Symbol	Parameter	Condition	MIN	MAX	Unit
V_{IL}	Low-level input voltage ¹ ACTS ACS			0.8 .3 V_{DD}	V
V_{IH}	High-level input voltage ¹ ACTS ACS		.5 V_{DD} .7 V_{DD}		V
I_{IN}	Input leakage current ACTS/ACS	$V_{IN} = V_{DD}$ or V_{SS}	-1	1	μA
V_{OL}	Low-level output voltage ³ ACTS ACS	$I_{OL} = 8.0mA$ $I_{OL} = 100\mu A$		0.40 0.25	V
V_{OH}	High-level output voltage ³ ACTS ACS	$I_{OH} = -8.0mA$ $I_{OH} = -100\mu A$.7 V_{DD} $V_{DD} - 0.25$		V
I_{OS}	Short-circuit output current ^{2, 4} ACTS/ACS	$V_O = V_{DD}$ and V_{SS}	-200	200	mA
I_{OL}	Output current ¹⁰ (sink)	$V_{IN} = V_{DD}$ or V_{SS} $V_{OL} = 0.4V$	8		mA
I_{OH}	Output current ¹⁰ (source)	$V_{IN} = V_{DD}$ or V_{SS} $V_{OH} = V_{DD} - 0.4V$	-8		mA
P_{total}	Power dissipation ^{2, 8, 9}	$C_L = 50pF$		1.8	mW/ MHz
I_{DDQ}	Quiescent Supply Current	Pre-Rad	$V_{IN} = V_{DD}$ or V_{SS} $V_{DD} = V_{DD} MAX$	10	μA
		Post-Rad Device Type 01		50	
ΔI_{DDQ}	Quiescent Supply Current Delta ACTS	For input under test $V_{IN} = V_{DD} - 2.1V$ For all other inputs $V_{IN} = V_{DD}$ or V_{SS} $V_{DD} = 5.5V$		1.6	mA
C_{IN}	Input capacitance ⁵	$f = 1MHz @ 0V$		15	pF
C_{OUT}	Output capacitance ⁵	$f = 1MHz @ 0V$		15	pF

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Notes:

- 1) Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: $V_{IH} = V_{IH(min)} + 20\%$, $- 0\%$; $V_{IL} = V_{IL(max)} + 0\%$, $- 50\%$, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to $V_{IH(min)}$ and $V_{IL(max)}$.
- 2) Supplied as a design limit but not guaranteed or tested.
- 3) Per MIL-PRF-38535, for current density $\leq 5.0E5$ amps/cm², the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765 pF/MHz.
- 4) Not more than one output may be shorted at a time for maximum duration of one second.
- 5) Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz and a signal amplitude of 50mV rms maximum.
- 6) Maximum allowable relative shift equals 50mV.
- 7) Device type 01 is only offered with a TID tolerance guarantee of 1E5 rads(Si), 3E5 rads(Si), and 5E5 rads(Si), and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A.
- 8) Power does not include power contribution of any TTL output sink current.
- 9) Power dissipation specified per switching output.
- 10) This value is guaranteed based on characterization data, but not tested.

AC Electrical Characteristics ²

($V_{DD} = 5.0V \pm 10\%$; $V_{SS} = 0V$ ¹, $-55^{\circ}C < T_C < +125^{\circ}C$); Unless otherwise noted, T_C is per the temperature range ordered.

Symbol	Parameter	Minimum	Maximum	Unit
t_{PHL}	Input to Y_n	1	13	ns
t_{PLH}	Input to Y_n	1	10	ns

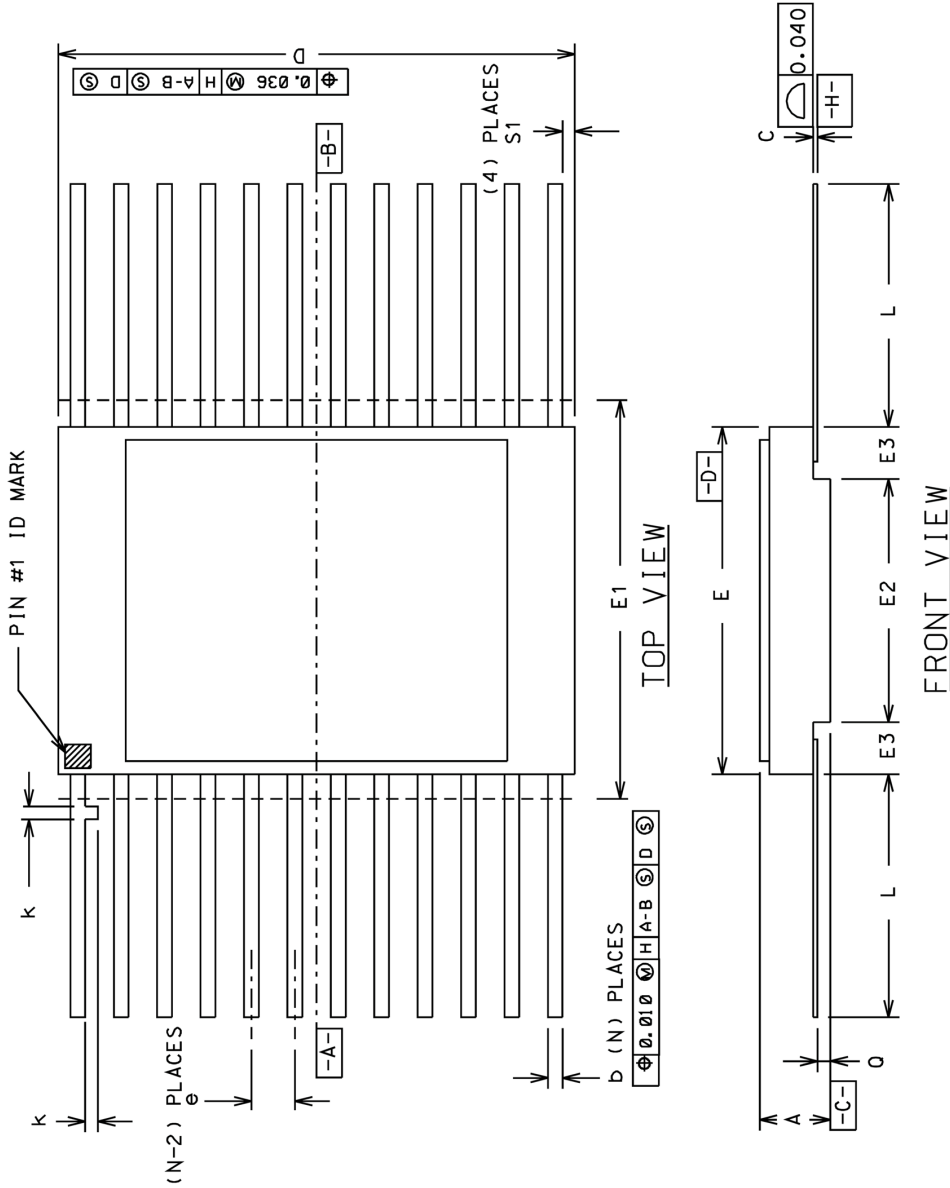
Notes:

- 1) Maximum allowable relative shift equals 50mV.
- 2) Device type 01 is only offered with a TID tolerance guarantee of 1E5 rads(Si), 3E5 rads(Si), and 5E5 rads(Si), and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A.

Quadruple 2-Input AND Gates

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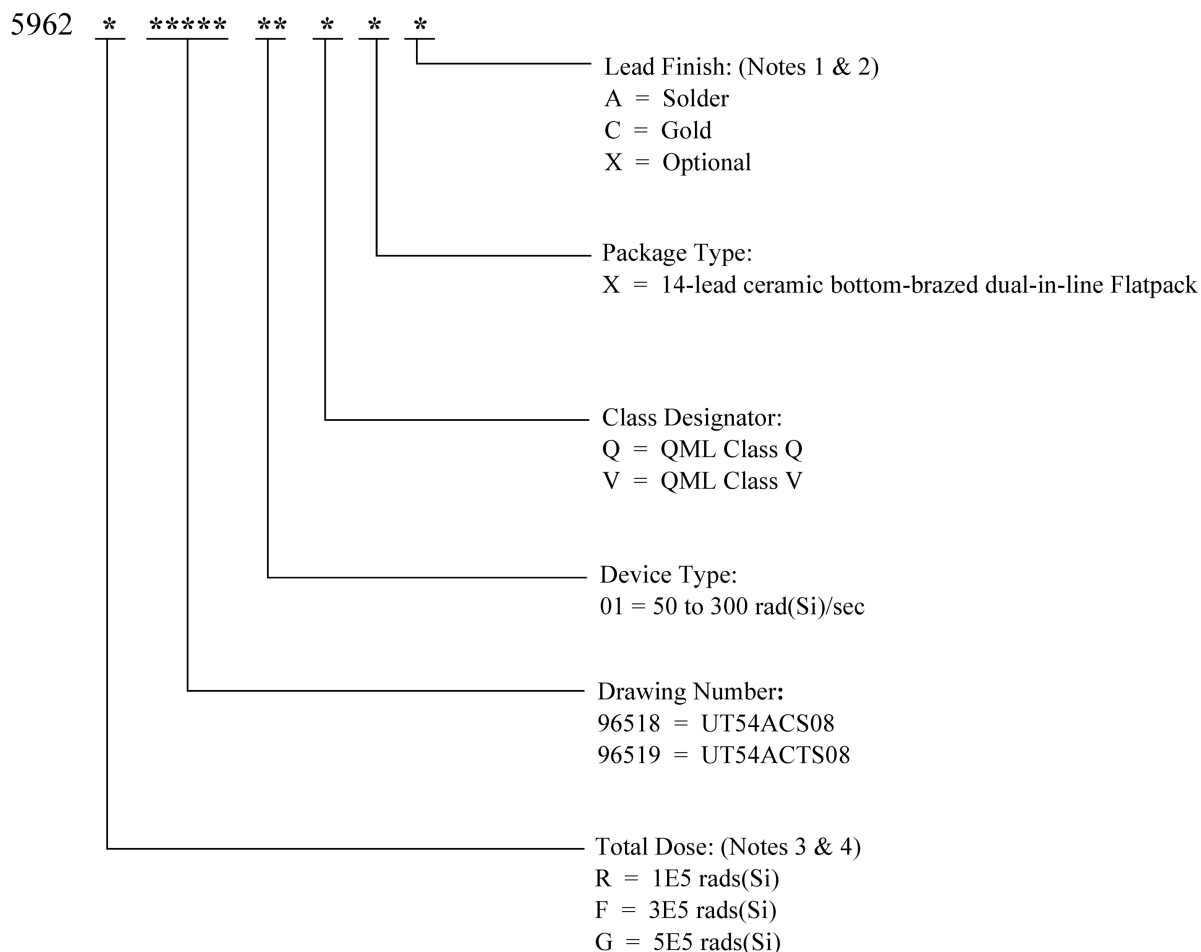
Packages



PKG CONFIG	LEAD COUNT	ML-STD 1835 DWG CONF B	DIMENSION SYMBOLS												
			A	b	c	D	E	E1	E2	E3	e	k	L	0	S1
-03	14	F-2A	0.115	0.022	0.009	0.390	0.260	0.290	0.130	0.050	0.015	0.370	0.045	0.045	0.005
-04	16	F-5A	0.045	0.015	0.009	0.440	0.285	0.315	0.130	0.050	0.015	0.370	0.045	0.045	0.005
-05	20	F-9A	0.115	0.022	0.009	0.540	0.300	0.330	0.130	0.050	0.015	0.370	0.045	0.045	0.005
			0.045	0.015	0.004	0.245	0.245	0.130	0.030	BSC	0.008	0.250	0.026	0.026	0.000

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UT54ACS08/UT54ACTS08: SMD



Notes:

- 1) Lead finish (A,C, or X) must be specified.
- 2) If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
- 3) Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening. For prototype inquiries, contact factory.
- 4) Device type 01 is only offered with a TID tolerance guarantee of 1E5 rads(Si), 3E5 rads(Si), and 5E5 rads(Si), and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A.

Datasheet Revision History

Revision Date	Description of Change	Author
10-17	Page 4 edited IDDQ Applied new CAES Data Sheet template to the document.	RT
1-18	Updates to reflect current SMD	RT

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Datasheet Definitions

	DEFINITION
Advanced Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet is subject to change . Specifications can be TBD and the part package and pinout are not final .
Preliminary Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

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