DATASHEET

RELEASED 7/13

Dual D Flip-Flops with Clear & Preset

UT54ACTS74E

Features

- 0.6µm CRH CMOS process
  - Latchup immune
- High speed
- Low power consumption
- Wide power supply operating range from 3.0V to 5.5V
- Available QML Q or V processes
- 14-lead flatpack
- UT54ACTS74E-SMD- 5962-96535

Description

The UT54ACTS74E contains two independent D-type positive triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the D input meeting the setup time requirement is transferred to the outputs on the positive-going edge of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

The device is characterized over full HiRel temperature range of -55°C to +125°C.

Function Table

Inputs				Output	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H [1]	H [1]
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q_0}$

Note:

1) The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at preset and clear are near V_{IL} maximum. In addition, this configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

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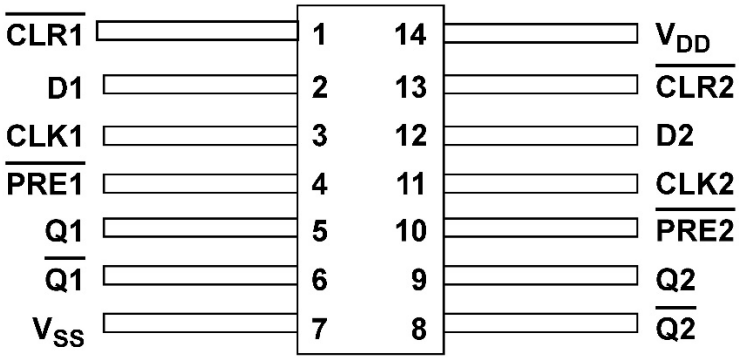
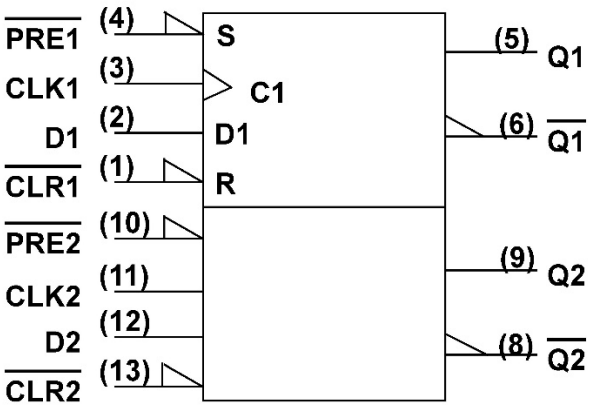
Pinouts



14-Lead Flatpack
Top View

Logic Symbol



Note:

1) Logic symbol in accordance with ANSI/IEEE standard 91-1984 and IEC Publication 617-12.

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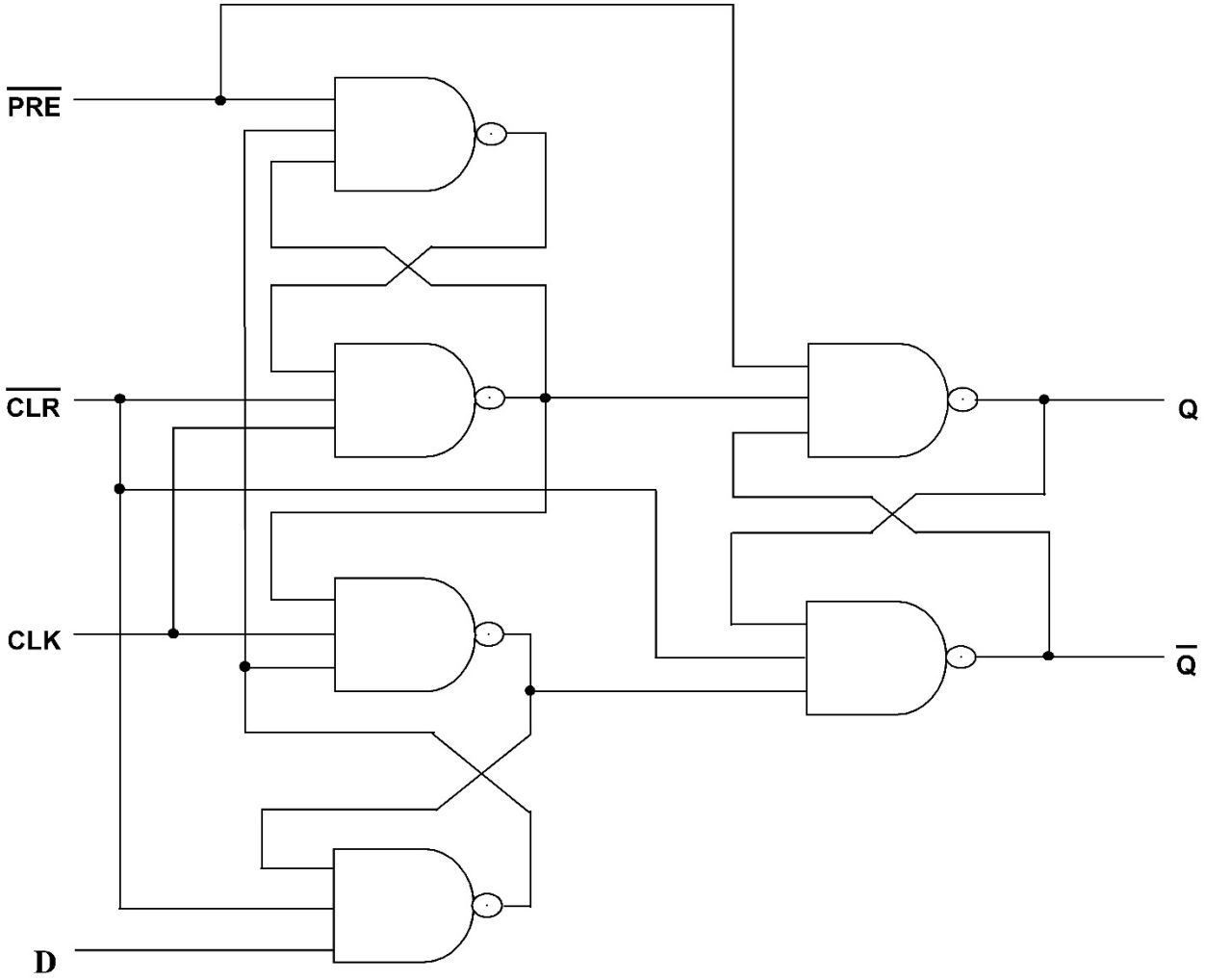
Logic Diagram



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Operational Environment[1]

Parameter	Limit	Units
Total Dose	1.0E6	rads(Si)
SEU Threshold [2]	80	MeV-cm^2/mg
SEL Threshold	120	MeV-cm^2/mg
Neutron Fluence	1.0E14	n/cm^2

Notes:

1) Logic will not latchup during radiation exposure within the limits defined in the table.
2) Device storage elements are immune to SEU affects.

Absolute Maximum Ratings

Symbol	Parameter	Limit	Units
V_{DD}	Supply voltage	-0.3 to 7.0	V
$V_{I/O}$	Voltage any pin	-.3 to V_{DD} +.3	V
T_{STG}	Storage Temperature range	-65 to +150	°C
T_J	Maximum junction temperature	+175	°C
T_{LS}	Lead temperature (soldering 5 seconds)	+300	°C
Θ_{JC}	Thermal resistance junction to case	15.5	°C/W
I_I	DC input current	±10	mA
P_D	Maximum power dissipation permitted @ T_C = +125°C	3.2	W

Notes:

1) Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2) Per MIL-STD-883, method 1012.1, Section 3.4.1, $P_D = (T_{J(max)} - T_{C(max)}) / \Theta_{JC}$

Recommended Operating Conditions

Symbol	Parameter	Limits	Units
V_{DD}	Supply voltage	3.0 to 5.5	V
V_{IN}	Input voltage any pin	0 to V_{DD}	V
T_C	Temperature range	-55 to +125	°C

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DC Electrical Characteristics [7]

(V_{DD} = 3.0V to 5.5V; V_{SS} = 0V[6]; -55°C < T_C < +125°C)

Symbol	Description	Condition	MIN	MAX	Unit
V_{IL1}	Low-level input voltage [1]	V_{DD} from 4.5V to 5.5V		0.8	V
V_{IL2}	Low-level input voltage [1]	V_{DD} from 3.0V to 5.5V		0.8	V
V_{IH1}	High-level input voltage [1]	V_{DD} from 4.5V to 5.5V	.5V_{DD}		V
V_{IH2}	High-level input voltage [1]	V_{DD} from 3.0V to 5.5V	2.0		V
I_{IN}	Input leakage current	V_{IN} = V_{DD} or V_{SS}	-1	1	µA
V_{OL1}	Low-level output voltage [3]	I_{OL} = 8mA V_{DD} = 4.5V to 5.5V		0.4	V
V_{OL2}	Low-level output voltage [3]	I_{OL} = 6mA V_{DD} = 4.5V to 5.5V		0.4	V
V_{OH1}	High-level output voltage [3]	I_{OH} = -8mA V_{DD} from 4.5V to 5.5V	0.7V_{DD}		V
V_{OH2}	High-level output voltage [3]	I_{OH} = -6mA V_{DD} from 3.0V to 3.6V	2.4		V
I_{OS1}	Short-circuit output current [2,4]	V_O = V_{DD} and V_{SS} V_{DD} from 4.5V to 5.5V	-200	200	mA
I_{OS2}	Short-circuit output current [2,4]	V_O = V_{DD} and V_{SS} V_{DD} from 3.0V to 3.6V	-100	100	mA
I_{OL1}	Low level output current [9]	V_{IN} = V_{DD} or V_{SS} V_{OL} = 0.4V V_{DD} from 4.5V to 5.5V	8		mA
I_{OL2}	Low level output current [9]	V_{IN} = V_{DD} or V_{SS} V_{OL} = 0.4V V_{DD} from 3.0V to 3.6V	6		mA
I_{OH1}	High level output current [9]	V_{IN} = V_{DD} or V_{SS} V_{OH} = V_{DD}-0.4V V_{DD} from 4.5V to 5.5V	-8		mA
I_{OH2}	High level output current [9]	V_{IN} = V_{DD} or V_{SS} V_{OH} = V_{DD}-0.4V V_{DD} from 3.0V to 3.6V	-6		mA
P_{total1}	Power dissipation [2,8]	C_L = 50pF V_{DD} = 4.5V to 5.5V		1.0	mW/ MHz
P_{total2}	Power dissipation [2,8]	C_L = 50pF V_{DD} = 3.0V to 3.6V		0.5	mW/ MHz
I_{DDQ}	Quiescent Supply Current	V_{IN} = V_{DD} or V_{SS} V_{DD} from 3.0V to 5.5V		10	µA
ΔI_{DDQ}	Quiescent Supply Current Delta	For input under test V_{IN} = V_{DD} - 2.1V For all other inputs V_{IN} = V_{DD} or V_{SS} V_{DD} = 5.5V		1.6	mA
C_{IN}	Input capacitance [5]	f = 1MHz V_{DD} = 0V		15	pF
C_{OUT}	Output capacitance [5]	f = 1MHz V_{DD} = 0V		15	pF

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Notes:

1) Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: $V_{IH} = V_{IH}(min) + 20\%, - 0\%$; $V_{IL} = V_{IL}(max) + 0\%, - 50\%$, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to $V_{IH}(min)$ and $V_{IL}(max)$.
2) Supplied as a design limit but not guaranteed or tested.
3) Per MIL-PRF-38535, for current density ≤ 5.0E5 amps/cm^2, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765 pF/MHz.
4) Not more than one output may be shorted at a time for maximum duration of one second.
5) Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at a frequency of 1MHz and a signal amplitude of 50mV rms maximum.
6) Maximum allowable relative shift equals 50mV.
7) All specifications valid for radiation dose ≤ 1E6 rads(Si) per MIL-STD-883 Method 1019.
8) Power dissipation specified per switching output.
9) Guaranteed based on characterization, but not tested.

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AC Electrical Characteristics [2]

(V_{DD} = 5.0V ±10%; V_{SS} = 0V [1], -55°C < T_C < +125°C); Unless otherwise noted, Tc is per the temperature range ordered.

Symbol	Parameter	Condition	V_{DD}	Minimum	Maximum	Unit
t_{PHL1}	CLK ↑ to Q, $\overline{Q}$	C_L = 50pF	3.0V to 3.6V	3	30	ns
			4.5V to 5.5V	3	14	
t_{PLH1}	CLK ↑ to Q, $\overline{Q}$	C_L = 50pF	3.0V to 3.6V	3	20	ns
			4.5V to 5.5V	2	11	
t_{PLH2}	$\overline{PRE}$ to $\overline{Q}$	C_L = 50pF	3.0V to 3.6V	4	30	ns
			4.5V to 5.5V	3	15	
t_{PHL2}	$\overline{PRE}$ to Q	C_L = 50pF	3.0V to 3.6V	3	20	ns
			4.5V to 5.5V	3	12	
t_{PHL3}	CLR to Q	C_L = 50pF	3.0V to 3.6V	4	30	ns
			4.5V to 5.5V	3	15	
t_{PLH3}	CLR to $\overline{Q}$	C_L = 50pF	3.0V to 3.6V	3	21	ns
			4.5V to 5.5V	2	12	
f_{MAX}	Maximum clock frequency	C_L = 50pF	3.0V to 3.6V		100	MHz
			4.5V to 5.5V		125	
t_{SU1}	Data setup time before CLK ↑	C_L = 50pF	3.0V to 3.6V	4		ns
			4.5V to 5.5V	3		
t_{SU2}	$\overline{PRE}$ or $\overline{CLR}$ inactive Data setup time before CLK ↑	C_L = 50pF	3.0V to 3.6V	1		ns
			4.5V to 5.5V	1		
t_H [3]	Data hold time after CLK ↑	C_L = 50pF	3.0V to 3.6V	0		ns
			4.5V to 5.5V	0		
t_{W1}	Minimum pulse width CLK high or low	C_L = 50pF	3.0V to 3.6V	5		ns
			4.5V to 5.5V	4		
t_{W2}	Minimum pulse width $\overline{PRE}$ or $\overline{CLR}$ low	C_L = 50pF	3.0V to 3.6V	5		ns
			4.5V to 5.5V	4		

Notes:

1) Maximum allowable relative shift equals 50mV.
2) All specifications valid for radiation dose ≤ 1E6 rads(Si) per MIL-STD-883 Method 1019.

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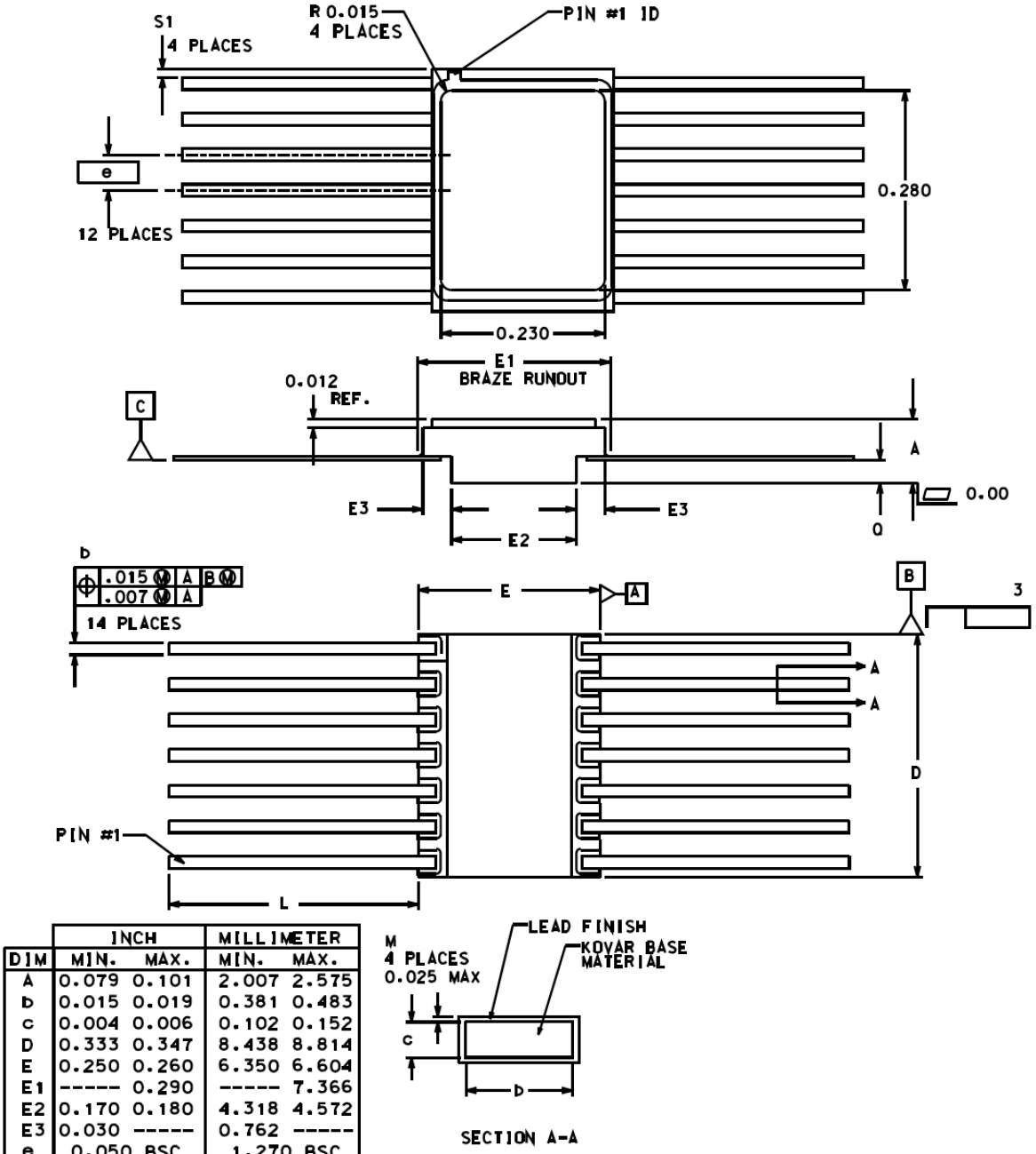
Packaging



DIM	INCH MIN.	INCH MAX.	MILLIMETER MIN.	MILLIMETER MAX.
A	0.079	0.101	2.007	2.575
b	0.015	0.019	0.381	0.483
c	0.004	0.006	0.102	0.152
D	0.333	0.347	8.438	8.814
E	0.250	0.260	6.350	6.604
E1	-----	0.290	-----	7.366
E2	0.170	0.180	4.318	4.572
E3	0.030	-----	0.762	-----
e	0.050 BSC		1.270 BSC	
L	0.340	0.360	8.636	9.144
Q	0.026	-----	0.660	-----
S1	0.005	-----	0.127	-----

Figure 1. 14-lead Flatpack

Notes:

1) All exposed metallized areas are gold plated over electroplated nickel per MIL-PRF-38535.
2) The lid is electrically connected to VSS.
3) Lead finishes are in accordance with MIL-PRF-38535.
4) Dimension symbol is in accordance with MILPRF-8533.
5) Lead position and colanarity are not measured.

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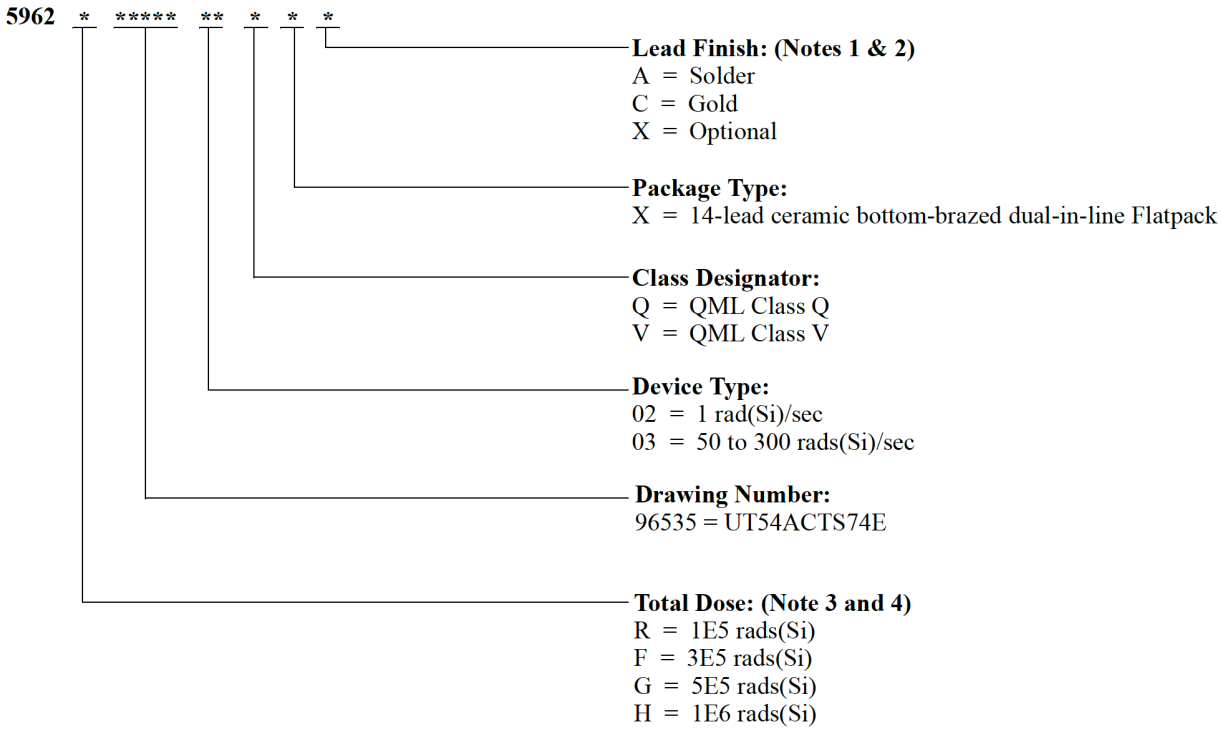
Ordering Information: UT54ACTS74E: SMD



Notes:

1) Lead finish (A,C, or X) must be specified.
2) If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3) Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening. For prototype inquiries, contact factory.
4) Device type 02 is only offered with a TID tolerance guarantee of 3E5 rads(Si) or 1E6 rads(Si) and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A and section 3.11.2. Device type 03 is only offered with a TID tolerance guarantee of 1E5 rads(Si), 3E5 rads(Si), and 5E5 rads(Si), and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A.

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Datasheet Definitions

	DEFINITION
Advanced Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet **is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final**.
Preliminary Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

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