Quadruple 2 to 1 Multiplexers

UT54ACTS157E

Features

- 0.6μm CRH CMOS process
  - Latchup immune
- High speed
- Low power consumption
- Wide power supply operating range of 3.0V to 5.5V
- Available QML Q or V processes
- 16-lead flatpack
- UT54ACTS157E-SMD-5962-96553

Description

The UT54ACTS157E is a monolithic data selector/multiplexer. A 4-bit word is selected from one of two sources and is routed to the four outputs. A separate strobe input, $\overline{G}$, is provided.

The device is characterized over full HiRel temperature range of -55°C to +125°C.

Function Table

Inputs				Output
Strobe $\overline{G}$	Select $\overline{A}/B$	Data A	Data B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

Pinouts

$\overline{A}/B$ — 1   16 — V_{DD}
1A — 2   15 — $\overline{G}$
1B — 3   14 — 4A
1Y — 4   13 — 4B
2A — 5   12 — 4Y
2B — 6   11 — 3A
2Y — 7   10 — 3B
V_{SS} — 8   9 — 3Y
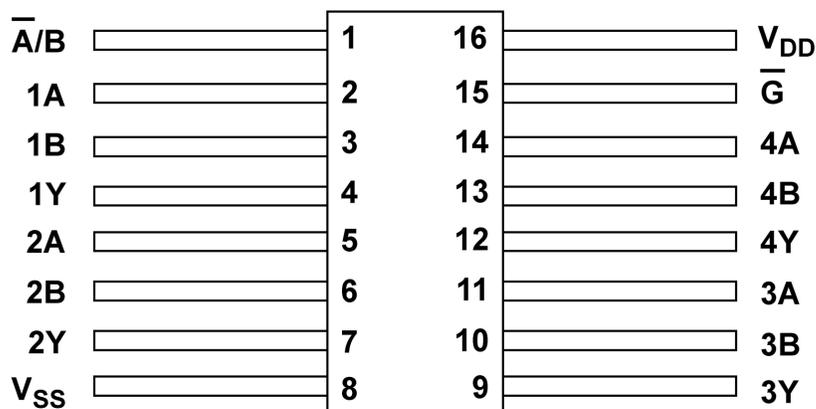
16-Lead Flatpack
Top View

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Logic Symbol
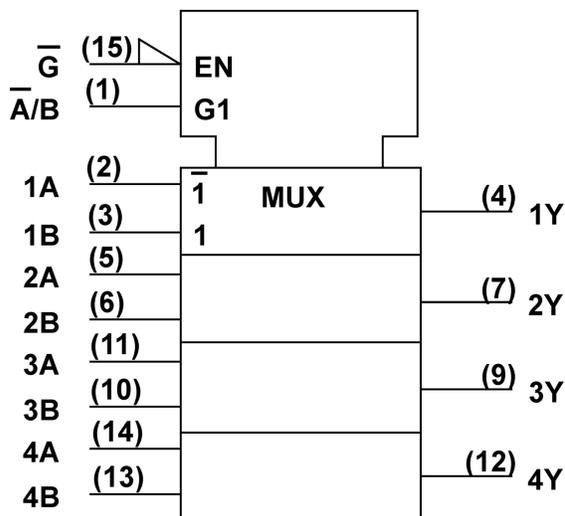
Note:

1) Logic symbol in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Logic Diagram

Quadruple 2 to 1 Multiplexers
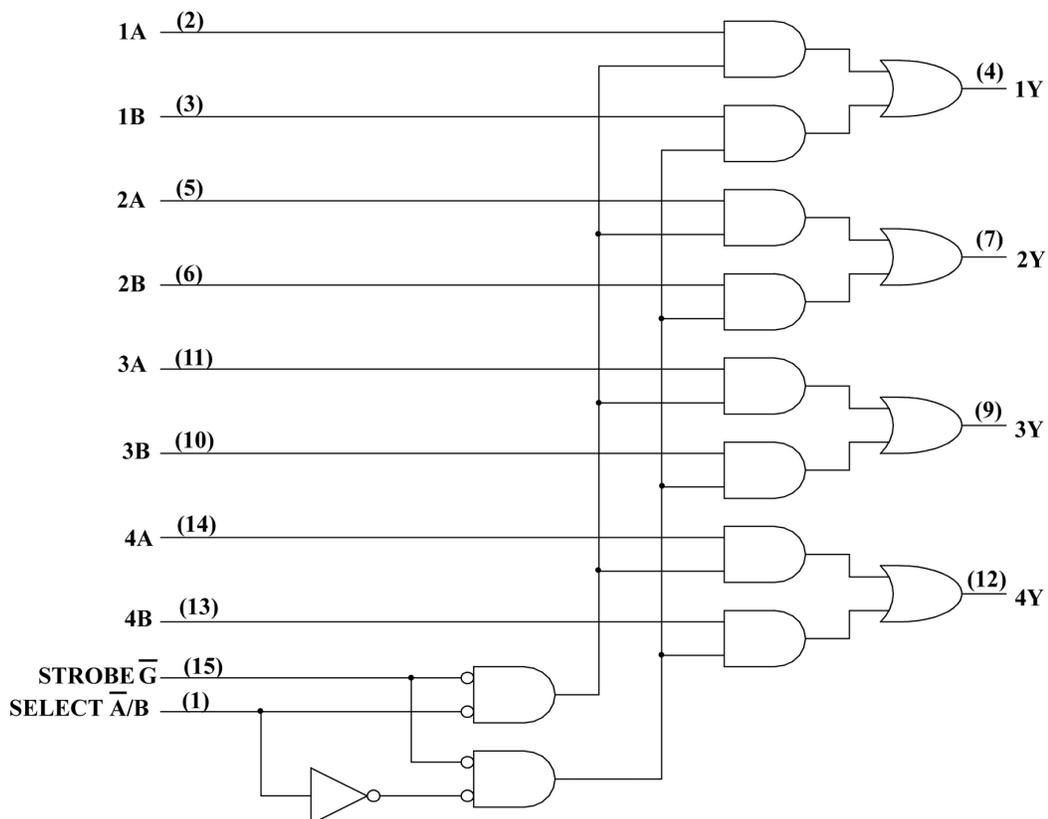
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Operational Environment [1]

Parameter	Limit	Units
Total Dose	1.0E6	rads(Si)
SEU Threshold [2]	108	MeV-cm^2/mg
SEL Threshold	120	MeV-cm^2/mg
Neutron Fluence	1.0E14	n/cm^2

Notes:

1) Logic will not latchup during radiation exposure within the limits defined in the table
2) Device storage elements are immune to SEU affects.

Absolute Maximum Ratings [1]

Symbol	Parameter	Limit	Units
V_{DD}	Supply voltage	-0.3 to 7.0	V
$V_{I/O}$	Voltage any pin	-0.3 to V_{DD} +0.3	V
T_{STG}	Storage Temperature range	-65 to +150	°C
T_J	Maximum junction temperature	+175	°C
T_{LS}	Lead temperature (soldering 5 seconds)	+300	°C
Θ_{JC}	Thermal resistance junction to case	15	°C/W
I_I	DC input current	±10	mA
P_D [2]	Maximum package power dissipation permitted @ T_C= +125°C	3.3	W

Notes:

1) Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2) Per MIL-STD-883, method 1012.1, Section 3.4.1, $P_D = (T_{j(max)} - T_{C(max)}) / \Theta_{jc}$

Recommended Operating Conditions

Symbol	Parameter	Limit	Units
V_{DD}	Supply voltage	3.0 to 5.5	V
V_{IN}	Input voltage any pin	0 to V_{DD}	V
Tc	Temperature range	-55 to + 125	°C

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DC Electrical Characteristics for the UT54ACTS157E [7]

(V_{DD} = 3.0V to 5.5V; V_{SS} = 0V [6]; -55°C < T_C < +125°C)

Symbol	Description	Condition	MIN	MAX	Unit
V_{IL1}	Low-level input voltage [1]	V_{DD} from 4.5V to 5.5V		0.8	V
V_{IL2}	Low-level input voltage [1]	V_{DD} from 3.0V to 3.6V		0.8	V
V_{IH1}	High-level input voltage [1]	V_{DD} from 4.5V to 5.5V	0.5 V_{DD}		V
V_{IH2}	High-level input voltage [1]	V_{DD} from 3.0V to 3.6V	2.0		V
I_{IN}	Input leakage current	V_{IN} = V_{DD} or V_{SS}	-1	1	µA
V_{OL1}	Low-level output voltage [3]	I_{OL} = 8mA V_{DD} = 4.5V to 5.5V		0.4	V
V_{OL2}	Low-level output voltage [3]	I_{OL} = 6mA V_{DD} = 3.0V to 3.6V		0.4	V
V_{OH1}	High-level output voltage [3]	I_{OH} = -8mA V_{DD} from 4.5V to 5.5V	0.7 V_{DD}		V
V_{OH2}	High-level output voltage [3]	I_{OH} = -6mA V_{DD} from 3.0V to 3.6V	2.4		V
I_{OS1}	Short-circuit output current [2, 4]	V_O = V_{DD} and V_{SS} V_{DD} from 3.0V to 3.6V	-200	200	mA
I_{OS2}	Short-circuit output current [2, 4]	V_O = V_{DD} and V_{SS} V_{DD} from 3.0V to 3.6V	-100	100	mA
I_{OL1}	Low level Output current [9]	V_{IN} = V_{DD} or V_{SS} V_{OL} = 0.4V V_{DD} from 4.5V to 5.5V	8		mA
I_{OL2}	Low level Output current [9]	V_{IN} = V_{DD} or V_{SS} V_{OL} = 0.4V V_{DD} from 3.0V to 3.6V	6		mA
I_{OH1}	High level Output current [9]	V_{IN} = V_{DD} or V_{SS} V_{OH} = V_{DD}-0.4V V_{DD} from 4.5V to 5.5V	-8		mA
I_{OH2} [9]	High level Output current	V_{IN} = V_{DD} or V_{SS} V_{OH} = V_{DD}-0.4V V_{DD} from 3.0V to 3.6V	-6		mA
P_{total1}	Power dissipation [2, 8]	C_L= 50pF V_{DD} from 4.5V to 5.5V		1.3	mW/ MHz
P_{total2}	Power dissipation [2, 8]	C_L = 50pF V_{DD} from 3.0V to 3.6V		0.75	mW/ MHz
I_{DDQ}	Quiescent Supply Current	V_{IN} = V_{DD} or V_{SS} V_{DD} from 3.0V to 5.5V		10	µA
ΔI_{DDQ}	Quiescent Supply Current Delta	For input under test V_{IN} = V_{DD} -2.1V For all other inputs V_{IN} = V_{DD} or V_{SS} V_{DD} = 5.5V		1.6	mA
C_{IN}	Input capacitance [5]	f = 1MHz, V_{DD} =0V		15	pF
C_{OUT}	Output capacitance [5]	f = 1MHz, V_{DD} =0V		15	pF

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Notes:

1) Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: $V_{IH} = V_{IH}(min) +$ 20%, - 0%; $V_{IL} = V_{IL}(max) + 0\%, -50\%$, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to $V_{IH}(min)$ and $V_{IL}(max)$.
2) Supplied as a design limit but not guaranteed or tested.
3) Per MIL-PRF-38535, for current density $\leq$ 5.0E5 amps/cm^2, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765pF/MHz.
4) Not more than one output may be shorted at a time for maximum duration of one second.
5) Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at a frequency of 1MHz and a signal amplitude of 50mV rms maximum.
6) Maximum allowable relative shift equals 50mV.
7) All specifications valid for the maximum radiation dose available for the respective device types.
8) Power dissipation specified per switching output.
9) Guaranteed by characterization, but not tested.

AC Electrical Characteristics for UT54ACTS157E [2]

(V_{DD}=5.0V ± 10%; V_{SS} = 0V [1], -55°C < T_C < +125°C)

| Symbol	Parameter	Condition	V_{DD}	Minimum	Maximum	Unit
t_{PHL1}	mA or mB to mY	C_L=50pF	3.0V to 3.6V	3	20	ns
			4.5V to 5.5V	2	11	
t_{PLH1}	mA or mB to mY	C_L=50pF	3.0V to 3.6V	3	18	ns
			4.5V to 5.5V	2	10	
t_{PHL2}	$\overline{G}$ to mY	C_L=50pF	3.0V to 3.6V	3	18	ns
			4.5V to 5.5V	2	10	
t_{PLH2}	$\overline{G}$ to mY	C_L=50pF	3.0V to 3.6V	3	18	ns
			4.5V to 5.5V	2	10	
t_{PHL3}	$\overline{A}$/B to mY	C_L=50pF	3.0V to 3.6V	3	19	ns
			4.5V to 5.5V	2	11	
t_{PLH3}	$\overline{A}$/B to mY	C_L=50pF	3.0V to 3.6V	3	17	ns
			4.5V to 5.5V	2	10	

Notes:

1) Maximum allowable relative shift equals 50mV.
2) All specifications valid for the maximum radiation dose available for the respective device types.

Quadruple 2 to 1 Multiplexers

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Packaging

TOP VIEW

FRONT VIEW

SECTION A-A

| c1	0.008 +/- 0.002
b1	0.020 +/- 0.002
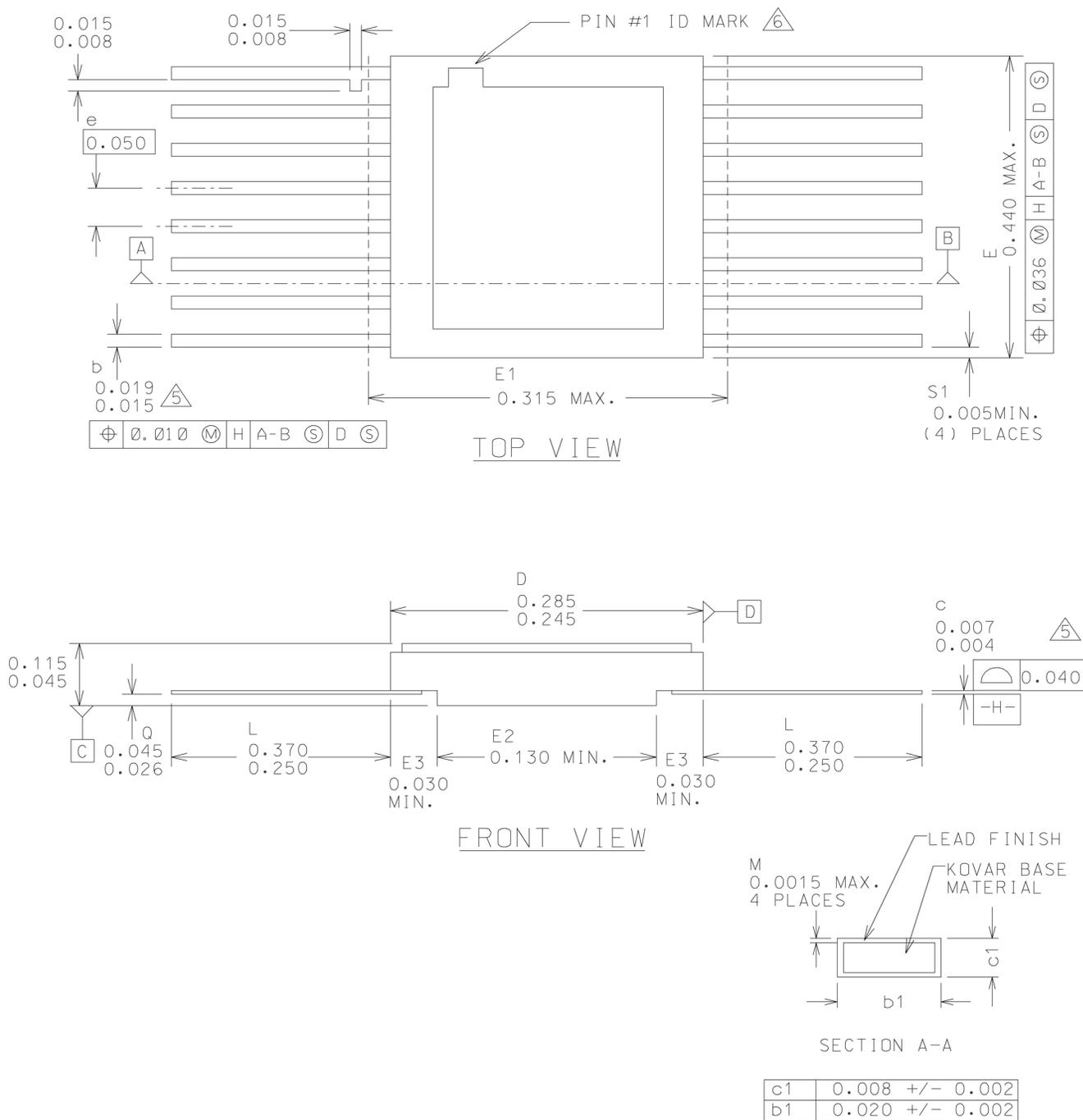
Notes:

1) All exposed metalized areas are gold plated over electroplated nickel per MIL-M-38510.

2) The lid is electrically connected to VSS.

3) Lead finishes are in accordance to MIL-PRF-38535.

4) Packaged dimensions and symbols are similar to MIL-STD-1835 variation F-5A.

5) Lead position and coplanarity are not measured.

6) ID mark symbol is vendor option.

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Ordering Information: UT54ACTS157E: SMD

5962   *   ***   **   *   *   ***

Lead Finish: (Notes 1 & 2)
A = Solder
C = Gold
X = Optional

Package Type:
X = 16-lead ceramic bottom-brazed dual-in-line Flatpack

Class Designator:
Q = QML Class Q
V = QML Class V

Device Type:
02 = 1 rad(Si)/sec
03 = 50 to 300 rads(Si)/sec

Drawing Number:
96553 = UT54ACTS157E

Total Dose: (Note 3 and 4)
R = 1E5 rads(Si)
F = 3E5 rads(Si)
G = 5E5 rads(Si)
H = 1E6 rads(Si)

Notes:
1) Lead finish (A,C, or X) must be specified.
2) If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3) Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening. For prototype inquiries, contact factory.
4) Device type 02 is only offered with a TID tolerance guarantee of 3E5 rads(Si) or 1E6 rads(Si) and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A and section 3.11.2. Device type 03 is only offered with a TID tolerance guarantee of 1E5 rads(Si), 3E5 rads(Si), and 5E5 rads(Si), and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A.

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Datasheet Definitions

	DEFINITION
Advanced Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet **is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final**.
Preliminary Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

The following United States (U.S.) Department of Commerce statement shall be applicable if these commodities, technology, or software are exported from the U.S.: These commodities, technology, or software were exported from the United States in accordance with the Export Administration Regulations. Diversion contrary to U.S. law is prohibited.