DATASHEET

RELEASED 5/16/12

RadHard EDAC

UT54ACS630

Features

- DC operating voltage range 4.5V to 5.5V
- Input logic levels
  - V_{IL} = 30% of V_{CC}
  - V_{IH} = 70% of V_{CC}
- Fast propagation delay 11ns (max)
- 0.6µm Commercial RadHard™ CMOS
  - Total dose: 100K rad(Si)
  - Single Event Latchup immune
  - SEU Onset LET: >108 MeV-cm^2/mg
- Standard Microcircuit Drawing 5962-06239
  - QML Q and V
- Package:
  - 28-lead flatpack

Description

The UT54ACS630 is a RadHard 16-bit parallel error detection and correction circuit. It uses a modified Hamming code to generate a 6-bit check word from each 16-bit data word. The check word is stored with the data word during a memory write cycle; during a memory read cycle a 22-bit word is taken from memory and checked for errors. Single bit errors in the data words are flagged and corrected. Single bit errors in the checkword are flagged, but not corrected. The position of the incorrect bit is pinpointed, in both cases, by the 6-bit error syndrome code which is output during the error correction cycle.

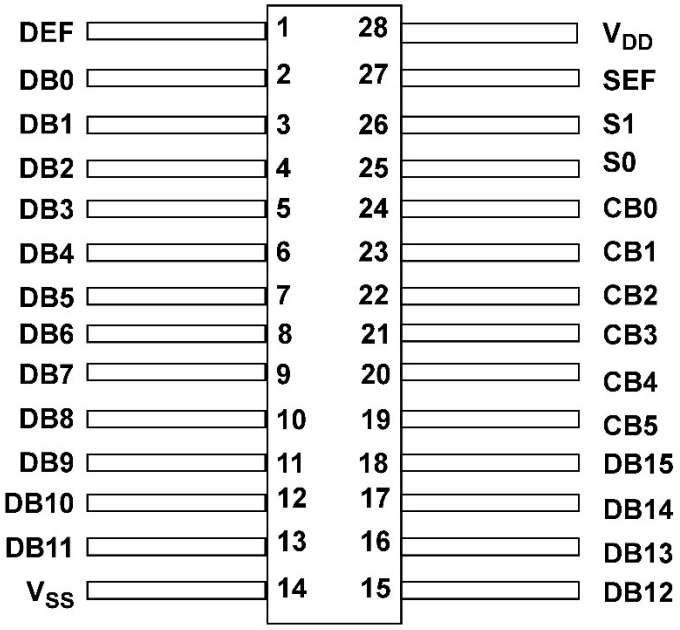
PIN Description

Pin Names	Description
S0, S1	Mode Control Inputs
DBn	Bidirectional Data Bus
CBn	Bidirectional Check bit Bus
SEF	Single Error Flag Output
DEF	Double Error Flag Output

RadHard EDAC

UT54ACS630

28-Lead Flatpack
Top View



Function Table

Control Functions

Memory Cycle	Control		EDAC Function	Data I/O	Checkword	Error Flags	
	S1	S0				SEF	DEF
WRITE	Low	Low	Generates Checkword	Input Data	Output Checkword	Low	Low
READ	Low	High	Read Data and Checkword	Input Data	Input Checkword	Low	Low
READ	High	High	Latch and Flag Error	Latch Data	Latch Checkword	Enabled	Enabled
READ	High	Low	Correct Data Word and Generate Syndrome Bits	Output Correction Data	Output Syndrome Bits	Enabled	Enabled

Checkword Generation

Check word Bit	16-bit Data Word															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CB0	X	X		X	X				X	X	X			X		
CB1	X		X	X		X	X		X			X			X	
CB2		X	X		X	X		X		X			X			X
CB3	X	X	X				X	X			X	X	X			
CB4				X	X	X	X	X						X	X	X
CB5									X	X	X	X	X	X	X	X

RadHard EDAC

UT54ACS630

Error Syndrome Codes

Syndrome Error Code	Error Locations																						
	DB																CB						No Error
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	
CB0	L	L	H	L	L	H	H	H	L	L	L	H	H	L	H	H	L	H	H	H	H	H	H
CB1	L	H	L	L	H	L	L	H	L	H	H	L	H	H	L	H	H	L	H	H	H	H	H
CB2	H	L	L	H	L	L	H	L	H	L	H	H	L	H	H	L	H	H	L	H	H	H	H
CB3	L	L	L	H	H	H	L	L	H	H	L	L	L	H	H	H	H	H	H	L	H	H	H
CB4	H	H	H	L	L	L	L	L	H	H	H	H	H	L	L	L	H	H	H	H	L	H	H
CB5	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	H	H	H	H	H	L	H

Error Functions

Total Number of Errors		Error Flags		Data Correction
16-Bit Data	6-Bit Check Word	SEF	DEF	
0	0	L	L	Not applicable
1	0	H	L	Correction
0	1	H	L	Correction
1	1	H	H	Interrupt
2	0	H	H	Interrupt
0	2	H	H	Interrupt

Radiation Hardness Specifications [1]

Parameter	Limit	Units
Total Dose	1.0E5	rad(Si)
SEL Immune	>108	MeV-cm^2/mg
SEU Onset LET	>108	MeV-cm^2/mg
Neutron Fluence [2]	1.0E14	n/cm^2

Notes:

1) Logic will not latch up during radiation exposure within the limits defined in the table.
2) Not tested, inherent of CMOS technology.

Absolute Maximum Ratings [1]

Symbol	Parameter	Limit	Units
V_{DD}	Supply voltage	-0.3 to 6.0	V
$V_{I/O}$	Voltage any pin	-0.3 to V_{DD} +0.3	V
T_{STG}	Storage Temperature range	-65 to +150	°C
T_J	Maximum junction temperature	+175	°C
Θ_{JC}	Thermal resistance junction to case	20	°C/W
I_I	DC input current	±10	mA
P_D	Maximum power dissipation	350	mW

DATASHEET

RELEASED 5/16/12

Notes:

1) Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.

Recommended Operating Conditions

Symbol	Parameter	Limit	Units
V_{DD}	Supply voltage	4.5 to 5.5	V
V_{IN}	Input voltage any pin	0 to V_{DD}	V
T_C	Temperature range	-55 to + 125	°C
t_{INRISE} t_{INFALL}	Max input rise or fall time (V_{IN} transitions between V_{IL} (max) and V_{IH} (min))	20	ns

RadHard EDAC

UT54ACS630

DC Electrical Characteristics [1]

(V_{DD} = 5.0V±10%; V_{SS} = 0V, -55°C < T_C < +125°C)

Symbol	Parameter	Condition	MIN	MAX	UNIT
V_{IL}	Low level input voltage[2]			0.3 V_{DD}	V
V_{IH}	High level input voltage[2]		0.7 V_{DD}		V
I_{IN}	Input leakage current	V_{DD} from 4.5V to 5.5V V_{IN} = V_{DD} or V_{SS}	-5	+5	µA
I_{OS}	Short-circuit output current[3,4]	V_O = V_{DD} or V_{SS} V_{DD} from 4.5V to 5.5V	300	300	mA
I_{OZ}	Three-state output leakage current	V_{IN} = V_{DD} or V_{SS}, V_{DD} from 4.5V to 5.5V	-10	+10	µA
V_{OL1}	Low-level output voltage (except DEF and SEF)[5]	I_{OL} = 16mA		0.4	V
		I_{OL} = 100µA V_{IN} = V_{IH} min or V_{IL} max V_{DD} from 4.5V to 5.5V		0.2	
V_{OH1}	High-level output voltage (except DEF and SEF)[5]	I_{OL} = -16mA	V_{DD}-0.8		V
		I_{OL} = -100µA V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$ V_{DD} from 4.5V to 5.5V	V_{DD}-0.2		
V_{OL2}	Low-level output voltage (DEF and SEF only)[3,4]	I_{OL} = 8mA		0.4	V
		I_{OL} = 100µA V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$ V_{DD} from 4.5V to 5.5V		0.2	
V_{OH2}	High-level output voltage (DEF and SEF only)[5]	I_{OL} = -8mA	V_{DD}-0.8		V
		I_{OL} = -100µA V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$ V_{DD} from 4.5V to 5.5V	V_{DD}-0.2		
I_{DDQ}	Quiescent supply current Pre-Rad -55°C to +125°C Post-Rad 25°C	V_{DD} = 5.5V V_{IN} = V_{DD} or V_{SS}		100	µA
$I_{DD\ (OP)}$	V_{DD} supply current operating	V_{IH} = 5.0V C_L=20pF V_{IL} = 0.0V V_{DD} = 5.0V		2	mA/ MHz
C_{IN}	Input capacitance[6]	f= 1MHz @ 0V V_{DD} from 4.5V to 5.5V		24	pF
C_{OUT}	Output capacitance[6]	f= 1MHz @ 0V V_{DD} from 4.5V to 5.5V		24	pF
V_{IC}^+	Positive input clamp voltage	For input under test, I_{IN} = 18mA V_{DD} = 0.0V	0.4	1.5	V
V_{IC}-	Negative input clamp voltage	For input under test, I_{IN} = -18mA V_{DD} = open	-1.5	-0.4	V
P_{TOTAL}	Power dissipation [7, 8, 9]	C_L = 20pf V_{DD} from 4.5V to 5.5V		400	µW/ MHz

Note:

1) All Specifications valid for radiation dose ≤1E5 rad(Si) per MIL-STD-883, method 1019.
2) Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: V_{IH}= V_{IH} (min) + 20%, - 0%; V_{IL} = V_{IL} (max) + 0%, - 50%, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to V_{IH}(min) and V_{IL}(max).
3) Not more than one output may be shorted at a time for maximum duration of one second.
4) Supplied as a design limit, but not guaranteed or tested.
5) Per MIL-PRF-38535, for current density ≤5.0E5 amps/cm^2, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765 pF-MHz.
6) Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz and a signal amplitude of 50mV rms maximum.
7) This value is guaranteed based on characterization data, but not tested.
8) Power does not include power contribution of any CMOS output sink current.
9) Power dissipation specified per switching output.

AC Electrical Characteristics[2]

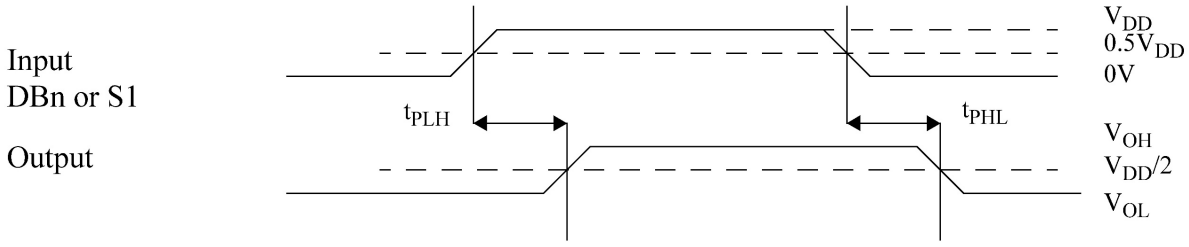
(V_{DD} = 5.0V +/- 10%; V_{SS} = 0V[1], -55°C< T_C < +125°C)

Symbol	Parameter	MIN	MAX	Unit
t_{PLH1}	Propagation delay time, DB to CBn	5.5	11	ns
t_{PHL1}	Propagation delay time, DBn to CBn	5.5	11	ns
t_{PLH2}	Propagation delay time, S1 to DEF	3	8	ns
t_{PLH3}	Propagation delay time, S1 to SEF	3	8	ns
t_{PZH}	Output enable time, S0 to DBn or CBn	2	9.5	ns
t_{PZL}	Output enable time, S0 to DBn or CBn	2	9.5	ns
t_{PHZ}	Output disable time, S0 to DBn or CBn	3.5	8	ns
t_{PLZ}	Output disable time, S0 to DBn or CBn	3.5	8	ns
t_S	Setup time, high or low, DBn or CBn to S1	0.5		ns
t_H	Hold time, high or low, DBn or CBn from S1	3.5		ns

Note:

1) Maximum allowable relative shift equals 50mV.
2) All specifications are valid for radiation dose >1E6rad(Si).

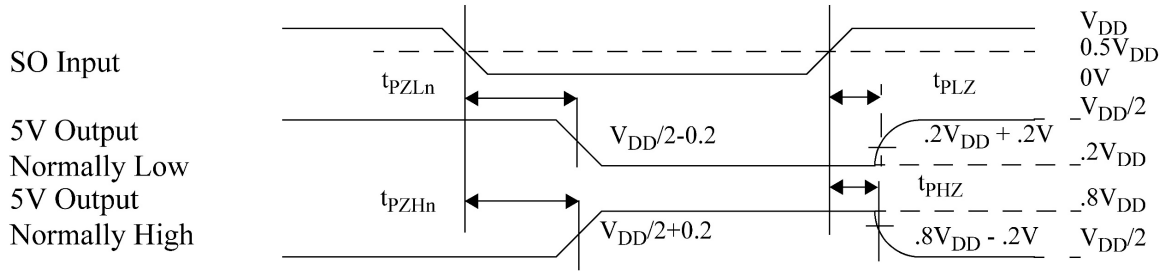
Propagation Delay



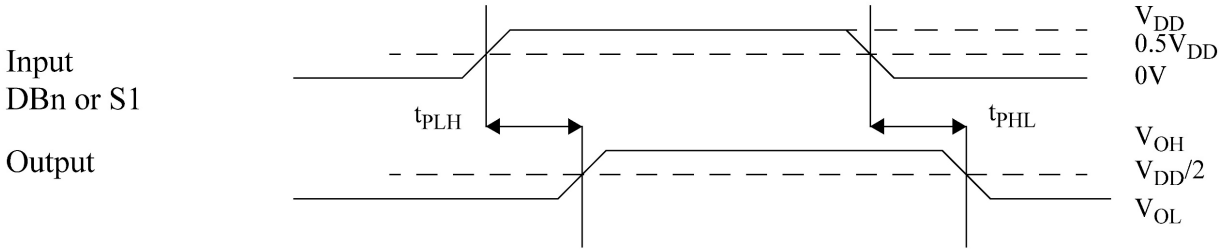
RadHard EDAC

UT54ACS630

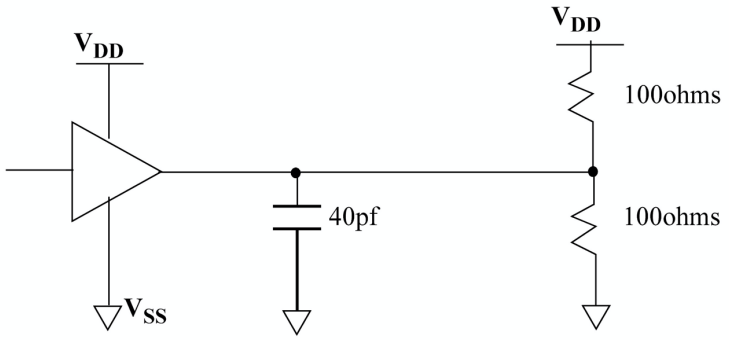
Enable Disable Times



Set up / Hold Waveforms



Test Load Or Equivalent[1]



Note:

1) Equivalent test circuit means that DUT performance will be correlated and remain guaranteed to the applicable test circuit, above, whenever a test platform change necessitates a deviation from the applicable test circuit.

RadHard EDAC

UT54ACS630

Package

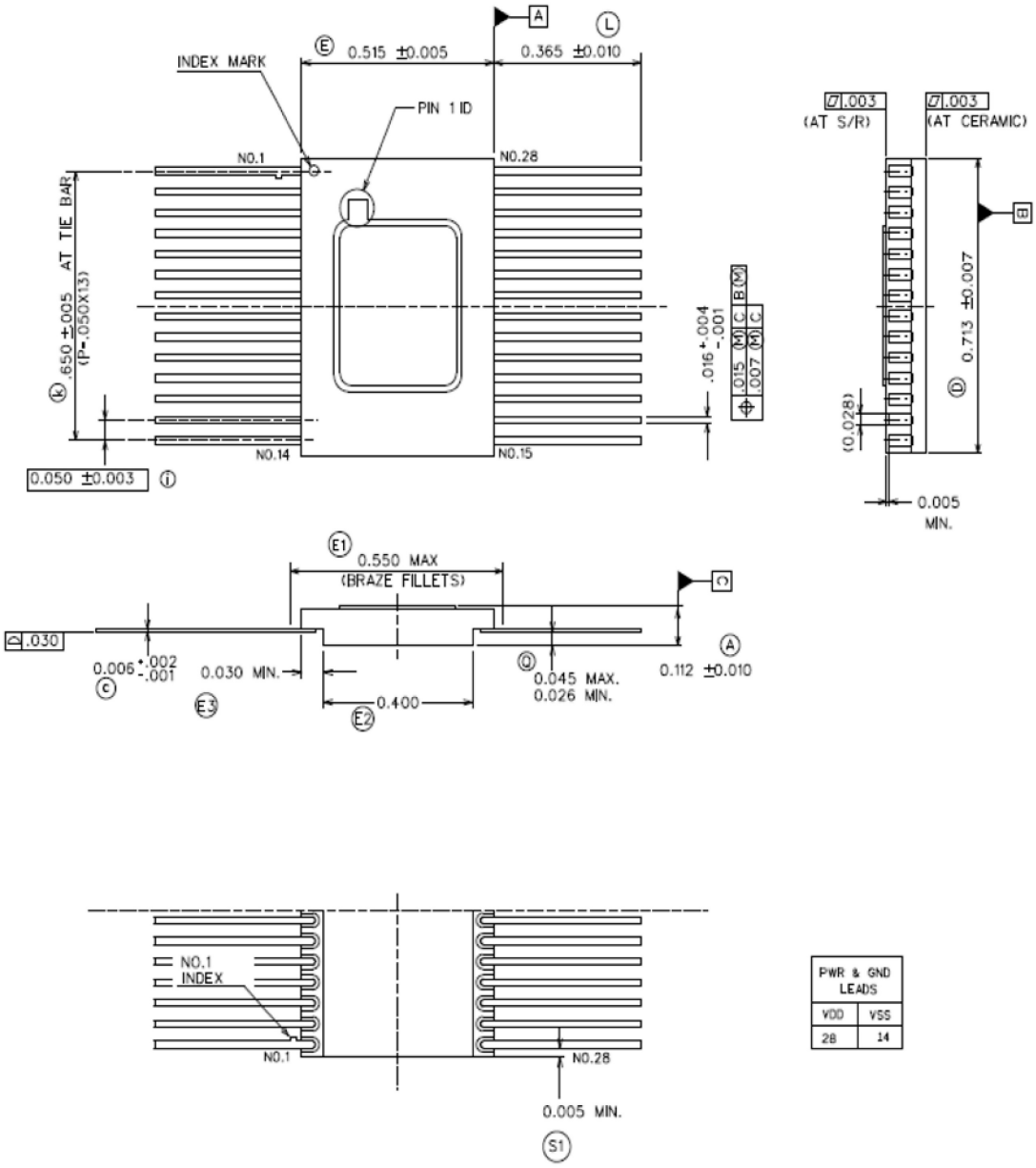


Figure 1: 28-pin Ceramic Flat pack

Note:

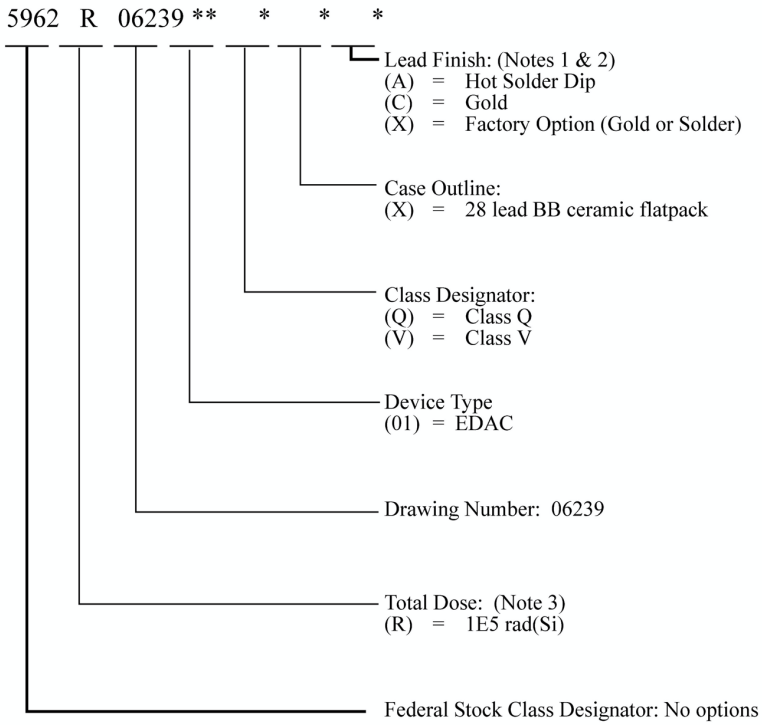
1) Seal ring is connected to VSS.
2) Units are in inches.
3) All exposed metalized areas must be gold plated 100 to 225 microinches thick and all bottom side exposed metalized areas must be gold plated to 60 microinches thick nominal. Both side shall be over electroplated nicked undercoating 100 to 350 microinches per MIL-PRF-38535.

RadHard EDAC

UT54ACS630

Ordering Information

UT54ACS630: SMD



Note:

1) Lead finish (A, C, or X) must be specified.
2) If an "X" is specified when ordering, then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3) Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation Hardening. For prototype inquiries, contact factory.

RadHard EDAC

UT54ACS630

Datasheet Definitions

	DEFINITION
Advanced Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet **is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final**.
Preliminary Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

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