DATASHEET

RELEASED 4/16

Triple ManyGate Configurable Logic Gate

UT54ACS3G99S

Features

- Voltage Supply: 3.0V to 5.5V
- Advanced CMOS technology
- Schmitt Trigger Inputs
- Tri-State Outputs
- ESD rating HBM: 2000V, Class 2
- Operational environment:
  - Total dose: 1 Mrad(Si)
  - Latchup immune (LET <= 100 MeV-cm^2/mg)
- Packaging:
  - 20-lead flatpack
- Standard Microelectronics Drawing (SMD) - 5962-15238
- QML Q, V

Introduction

The UT54ACS3G99S is CAES Triple, Combinatorial, ManyGate Configurable Logic Gate with Schmitt Trigger inputs and Tri-State outputs. The output-enable pin /OEn is active LOW. The sixteen possible combinations of the four inputs An-Dn determine one of sixteen Yn output states when /OEn is LOW=VSS. The outputs Yn are disabled when /OEn is HIGH=VDD.

The ManyGate device logic functions are pin configurable by applying either a logic HIGH (VDD) or LOW (VSS) to the logic input pins as noted. Three identical, independently configurable combinatorial logic blocks are included in the UT54ACS3G99S, as shown in the logic diagram of Figure 1. The nine basic Boolean logic functions in each logic block are listed here as follows: AND, NAND, OR, NOR, XOR, XNOR, MUX, inverter, and buffer. All sixteen logic functions are described in Tables 2-9.

The UT54ACS3G99S triple, configurable, combinatorial logic gate is available in a small form factor, 20-lead ceramic flatpack and operates on a power supply range of 3.0V to 5.5V.

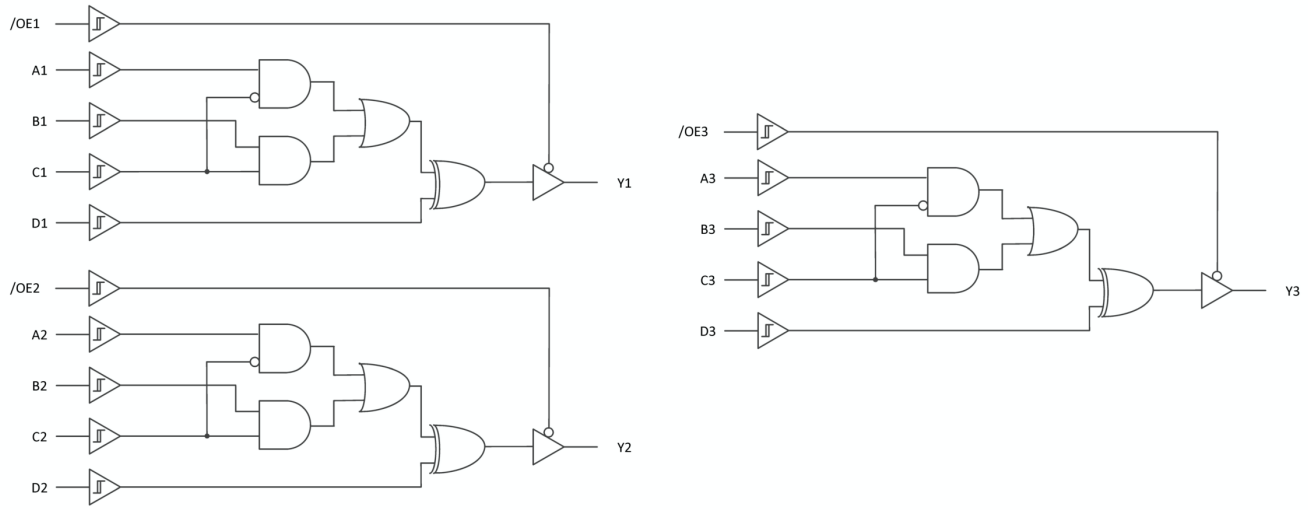

Figure 1: UT54ACS3G99S Logic Diagram

Triple ManyGate Configurable Logic Gate

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1 Pin Definition/Description

Table 1. Pin Naming

Pin No.	Name	Description
7, 8, 9	/OEn	Active LOW output enable
2, 11, 16	An	A input
3, 12, 17	Bn	B input
4, 13, 18	Cn	C input
5, 14, 19	Dn	D input
1, 6, 15	Yn	3-State Output
20	V_{DD}	Power supply pin
10	V_{SS}	Ground pin

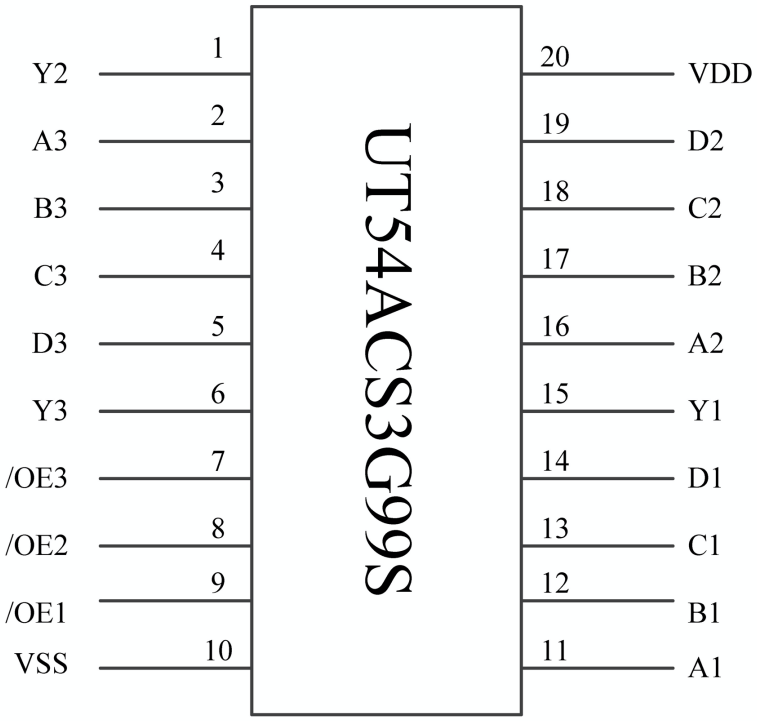

Figure 2: UT54ACS3G99S Pinout Diagram

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2 Functional Truth Tables and Operational Modes

Table 2. Combinatorial Truth Table An, Bn, Cn, Dn to n=1,2,3 of Storage Element Yn Output

Dn	Cn	Bn	An	Output to D_{IN}
L	L	L	L	L
L	L	L	H	H
L	L	H	L	L
L	L	H	H	H
L	H	L	L	L
L	H	L	H	L
L	H	H	L	H
L	H	H	H	H
H	L	L	L	H
H	L	L	H	L
H	L	H	L	H
H	L	H	H	L
H	H	L	L	H
H	H	L	H	H
H	H	H	L	L
H	H	H	H	L

3 Applications Information

Table 3. Equivalent Logic Functions Created from Table 2

Primary Logic Function	Complementary Logic Function	Table
3-state buffer		4
3-state inverter		5
3-state 2-in-1 data selector MUX		6
3-state 2-in-1 data selector MUX, inverted out		6
3-state 2-input AND	3-state 2-input NOR, both inputs inverted	7
3-state 2-input AND, one input inverted	3-state 2-input NOR, one input inverted	7
3-state 2-input AND, both inputs inverted	3-state 2-input NOR	7
3-state 2-input NAND	3-state 2-input OR, both inputs inverted	8
3-state 2-input NAND, one input inverted	3-state 2-input OR, one input inverted	8
3-state 2-input NAND, both inputs inverted	3-state 2-input OR	8
3-state 2-input XOR, both inputs inverted		9

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Table 4. 3-State Buffer Functions

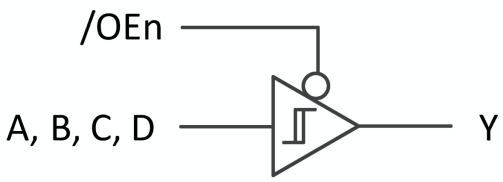
Function	A	B	C	D
3-State Buffer 	Input	X	L	L
	X	Input	H	L
	L	H	Input	L
	H	L	Input	H
	H	X	L	Input
	X	L	H	Input
	L	L	X	Input

Table 5. 3-State Inverter Buffer Functions

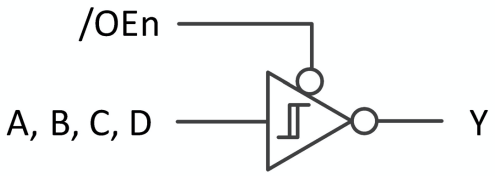
Function	A	B	C	D
3-State inverter buffer 	Input	X	L	H
	X	Input	H	H
	L	H	Input	H
	H	L	Input	L
	H	X	L	Input
	X	H	H	Input
	H	H	X	Input

Table 6. 3-State MUX Functions

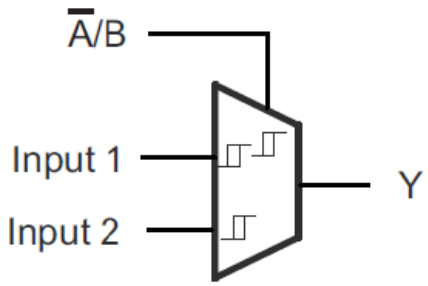
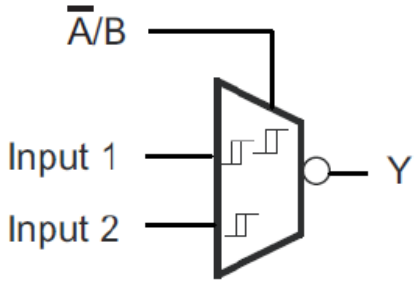
Function	A	B	C	D
3-State 2-to-1, Data Selector Mux 	Input 1 or Input 2	Input 1 or Input 2	Input 1 or Input 2	L
3-State 2-to-1, Data Selector Mux, Inverted Out 	Input 1 or Input 2	Input 1 or Input 2	Input 1 or Input 2	H

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Table 7. 3-State AND/NOR Functions

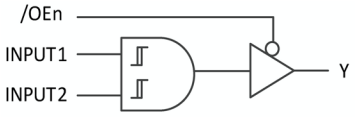
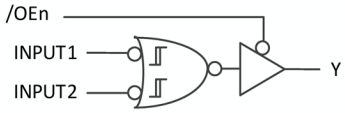
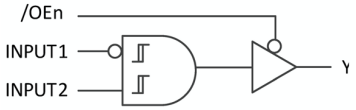
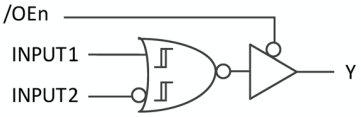
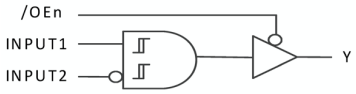
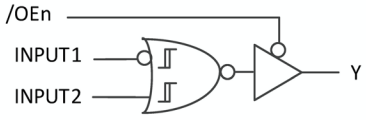
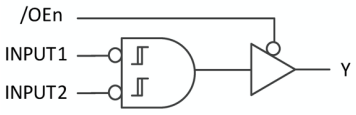
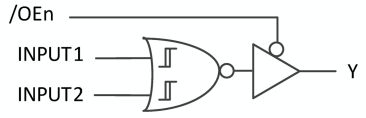
#IN	AND	NOR	A	B	C	D
2			L L	Input 1 Input 2	Input 2 Input 1	L L
2		 Or	Input 2 H	L Input 1	Input 1 Input 2	L H
2			Input 1 H	L Input 2	Input 2 Input 1	L H
2			Input 1 Input 2	H H	Input 2 Input 1	H H

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Table 8. 3-State NAND/OR Functions

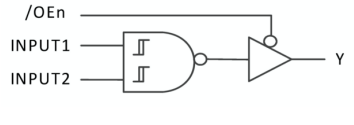
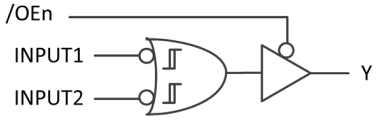
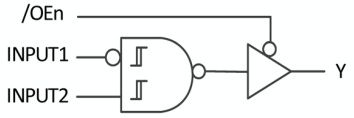
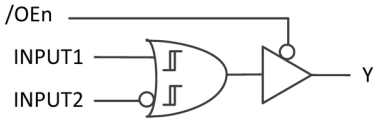
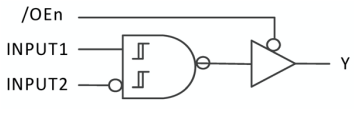
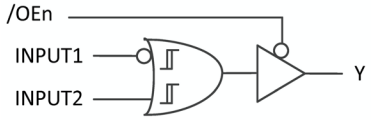
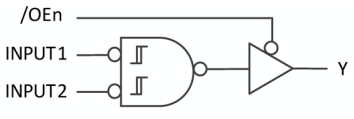
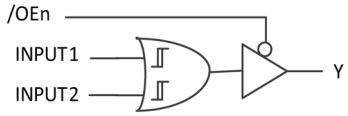
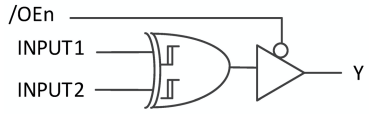
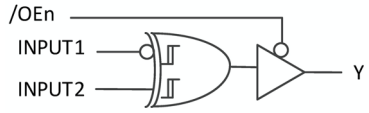
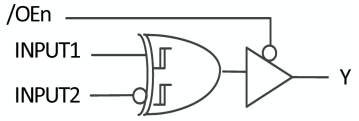
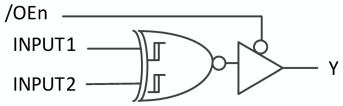
#IN	NAND	OR	A	B	C	D
2			L L	Input 1 Input 2	Input 2 Input 1	H H
2			Input 2 H	L Input 1	Input 1 Input 2	H L
2			Input 1 H	L Input 2	Input 2 Input 1	H L
2			Input 1 Input 2	H H	Input 2 Input 1	L L

Table 9. 3-State XOR/XNOR Functions

#IN	XOR/XNOR Function	A	B	C	D
2		Input 1 Input 2	X X	L L	Input 2 Input 1
		X X	Input 1 Input 2	H H	Input 2 Input 1
		L L	H H	Input 1 Input 2	Input 2 Input 1
2		H	L	Input 1	Input 2
2		H	L	Input 1	Input 2
2		H H	L L	Input 1 Input 2	Input 2 Input 1

4 Operational Environment

Table 10. Radiation

Parameter	Limit	Units
Total Ionizing Dose (TID)	1.0E6	rad(Si)
Single Event Latchup (SEL)	>100	MeV-cm^2/mg
Neutron Fluence[1]	1.0E13	n/cm^2

Note:

1) Guaranteed by Characterization

5 Absolute Maximum Ratings

Table 11. Absolute Maximum Ratings Table[1]

Symbol	Parameter	Limit	Unit
V_{DD}	Positive Output Supply Voltage	-0.3 to 7.0	V
V_{IO}	Voltage on an Input pin during operation	-0.3 to (V_{DD}+ 0.3V)	V
$I_{I/O}$	DC input/output Current	+/-10	mA
Θ_{JC}	Thermal resistance, junction-to-case	15	°C/W
T_J	Junction Temperature[2]	+175°C	°C
T_{STG}	Storage Temperature	-65°C to+150°C	°C
P_D[3]	Maximum package power dissipation permitted at Tc=125°C	1	W

Notes:

1) Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2) Maximum junction temperature may be increased to +175°C during burn-in and life test.
3) Test per MIL-STD-883, Method 1012.

6 Recommended Operating Conditions

Table 12. Recommended Operating Conditions

Symbol	Parameter	Limit	Unit
V_{DD}	Positive Output Supply Voltage	3.0 to 5.5	V
V_{IN}	Input Voltage on any pin	0.0 to V_{DD}	V
Tc	Case Temperature Range	-55 to +125	°C
t_R, t_F	Input Rise/Fall time (20%/80%)	<1	sec

7 3.3V DC Characteristics

(V_{DD}= 3.3V ± 0.3V, -55°C < Tc < +125°C); Unless otherwise noted, Tc is per the temperature range ordered

For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured

Table 13. 3.3V DC Electrical Characteristics Table[1,3,4]

Symbol	Parameter	Condition	MIN	MAX	Unit
V_{T+}	Positive going input voltage threshold[1]			0.7*V_{DD}	V
V_{T-}	Negative going input voltage threshold[1]		0.3*V_{DD}		V
V_H	Hysteresis Voltage		0.3		V
V_{OL}[2]	Low-level output voltage	I_{OL} = 100µA V_{DD} from 3.0V to 3.6V		0.25	V
V_{OH}[2]	High-level output voltage	I_{OH} = -100µA V_{DD} from 3.0V to 3.6V	V_{DD} – 0.25		V
I_{IN}	Input leakage current	V_{IN} = V_{DD} or GND, V_{DD} = 0.0V to 3.6V	-1	+1	µA
I_{OS}[3, 4]	Output Short Circuit Current	V_{OUT} = V_{DD} + V_{SS}	-200	+200	mA
I_{OL}[5]	Low level output current (sink)	V_{IN} = V_{DD} or V_{SS} V_{OL} = 0.4V V_{DD} from 3.0V to 3.6V	8		mA
I_{OH}[5]	High level output current (source)	V_{IN} = V_{DD} or V_{SS} V_{OH} = V_{DD} - 0.4V V_{DD} from 3.0V to 3.6V	-8		mA
I_{OZ}	Output Three-State Current	Device Enabled, V_{OUT} = 0V or V_{DD}, V_{DD} = 3.6V	-5	+5	µA
I_{DDQ}	Quiescent Supply Current Pre-Rad (Device Type 01 & 02)	V_{IN} = V_{DD} or V_{SS} V_{DD} = V_{DD} MAX		10	µA
	Quiescent Supply Current Post-Rad (Device Type 01)			25	µA
	Quiescent Supply Current Post-Rad (Device Type 02)			130	µA
Ptotal[5,6]	Power dissipation	C_L = 78pF		3.0	mW/MHz
C_{IN}[6]	Input capacitance			15	pF
C_{OUT}[7]	Output capacitance			15	pF

Notes:

1) Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: VIH = VIH(min) + 20%, -0%; VIL = VIL(max) + 0%, - 50%, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to VIH(min) and VIL(max).
2) Per MIL-PRF-38535, for current density <=5.0E5 amps/cm^2, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765pF/MHz.
3) Supplied as a design limit but not guaranteed or tested.
4) Not more than one output may be shorted at a time for maximum duration of one second.
5) Guaranteed by characterization but not tested.
6) Power dissipation specified per switching output.
7) Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz and a signal amplitude of 50mV rms maximum.

8 5.0V DC Characteristics

(V_{DD}= 5.0V ± 0.5V, -55°C < TC < +125°C); Unless otherwise noted, Tc is per the temperature range ordered

Table 14. 5V DC Electrical Characteristics Table[1,3,4]

Symbol	Parameter	Condition	MIN	MAX	Unit
V_{T+}	Positive going input voltage threshold[1]			0.7*V_{DD}	V
V_{T-}	Negative going input voltage threshold[1]		0.3*V_{DD}		V
V_H	Hysteresis Voltage		0.3		V
V_{OL}[2]	Low-level output voltage	I_{OL} = 100µA; V_{DD} from 5.0V to 5.5V		0.25	V
V_{OH}[2]	High-level output voltage	I_{OH} = -100µA; V_{DD} from 5.0V to 5.5V	V_{DD} – 0.25		V
I_{IN}	Input leakage current	V_{IN} = V_{DD} or GND; V_{DD} = 5.0V to 5.5V	-1	+1	µA
I_{OS}[3, 4]	Output Short Circuit Current	V_{OUT} = V_{DD} + VSS	-300	+300	mA
I_{OL}[5]	Low level output current (sink)	V_{IN} = V_{DD} or V_{SS}; V_{OL} = 0.4V; V_{DD} from 5.0V to 5.5V	-12		mA
I_{OH}[5]	High level output current (source)	Device Enabled; V_{OUT} = 0V or V_{DD}; V_{DD} = 5.5V V_{OH} = V_{DD} - 0.4V	12		mA
I_{OZ}	Output Three-State Current	V_{IN} = V_{DD} or V_{SS}; V_{DD} from 5.0V to 5.5V	-5	+5	µA
I_{DDQ}	Quiescent Supply Current Pre-Rad (Device Type 01 & 02)	V_{IN} = V_{DD} or V_{SS} V_{DD} = V_{DD} MAX		10	µA
	Quiescent Supply Current Post-Rad (Device Type 01)			25	µA
	Quiescent Supply Current Post-Rad (Device Type 02)			130	µA
Ptotal[5,6]	Power dissipation [5, 6]	C_L = 78pF		3.0	mW/MHz
C_{IN}[6]	Input capacitance			15	pF
C_{OUT}[7]	Output capacitance			15	pF

Notes:

1) Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: VIH = VIH(min) + 20%, - 0%; VIL = VIL(max) + 0%, - 50%, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to VIH(min) and VIL(max).
2) Per MIL-PRF-38535, for current density <=5.0E5 amps/cm2, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765pF/MHz.
3) Supplied as a design limit but not guaranteed or tested.
4) Not more than one output may be shorted at a time for maximum duration of one second.
5) Guaranteed by characterization but not tested.
6) Power dissipation specified per switching output.
7) Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and VSS at frequency of 1MHz and a signal amplitude of 50mV rms maximum.

9 AC Electrical Characteristics

(V_{DD}= 3.0V to 5.5V, -55°C < Tc < +125°C); Unless otherwise noted, Tc is per the temperature range ordered

Table 15. AC Electrical Table for the 3G99S

Symbol	Parameter	Condition	Minimum	Maximum	Unit
t_{PLH}	A, B, C, Dn to Yn	3.0V to 3.6V		18.5	ns
		4.5V to 5.5V		13	ns
t_{PHL}	A, B, C, Dn to Yn	3.0V to 3.6V		20.5	ns
		4.5V to 5.5V		15	ns
t_{PZL}	/OEn low to Yn	3.0V to 3.6V		13.5	ns
		4.5V to 5.5V		9.5	ns
t_{PZH}	/OEn low to Yn	3.0V to 3.6V		14.5	ns
		4.5V to 5.5V		10.5	ns
t_{PLZ}	/OEn high to Yn three-state	3.0V to 3.6V		12	ns
		4.5V to 5.5V		10	ns
t_{PHZ}	/OEn high to Yn three-state	3.0V to 3.6V		16	ns
		4.5V to 5.5V		13	ns

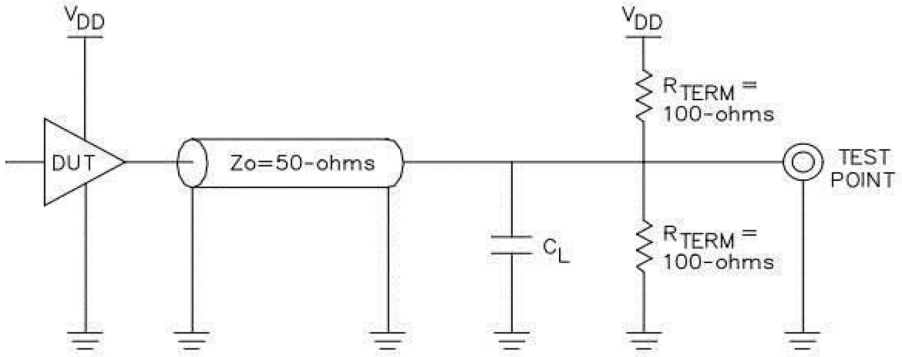


Figure 3. Test Load

Note:

1) CL = 78 pF minimum or equivalent (includes scope probe and test socket). Measurement of data output occurs at the low to high or high to low transition mid-point, typically VDD/2.

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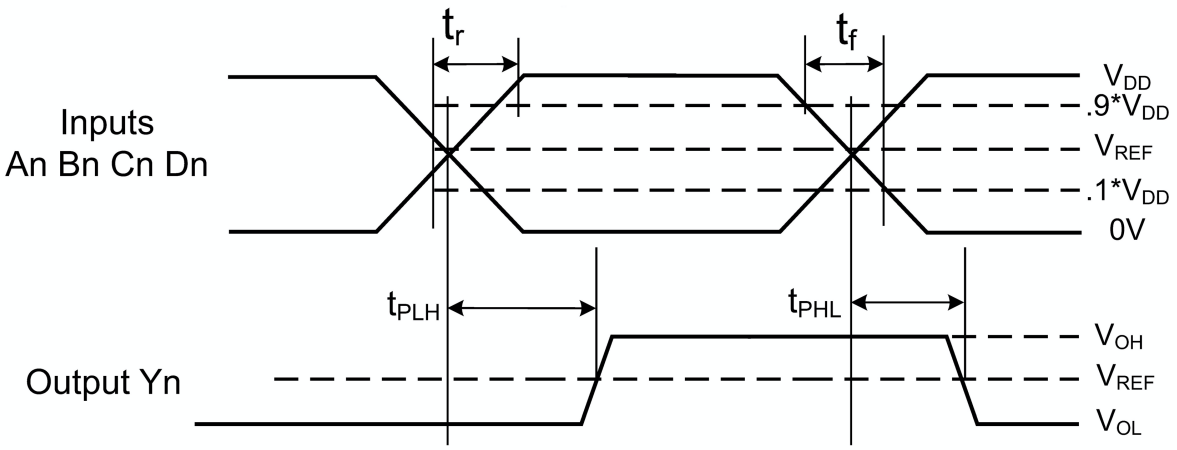
Propagation Delay



Enable/Disable Times

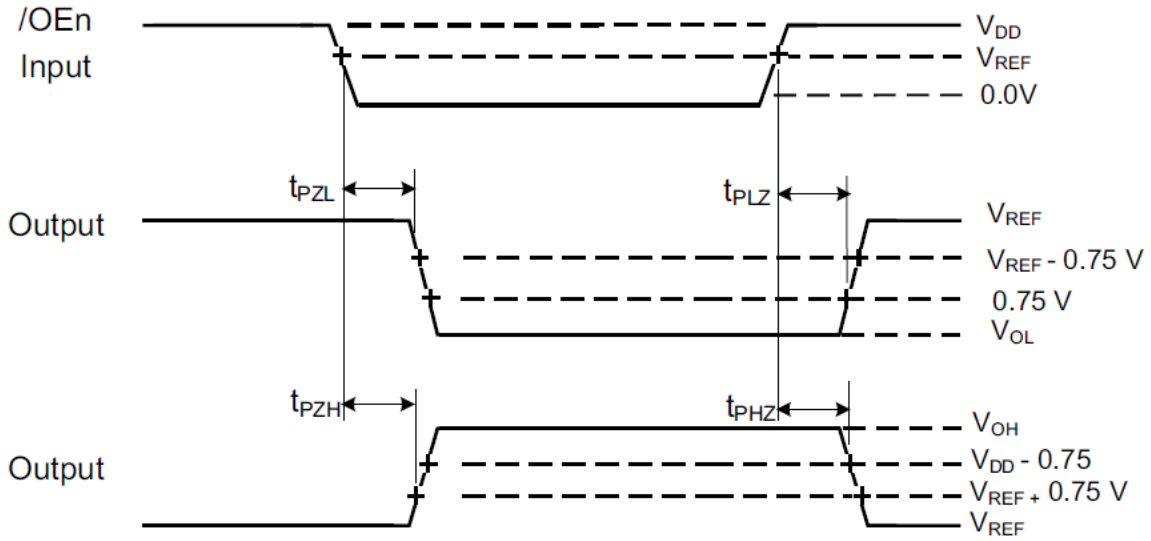


Figure 4. Timing Diagram

Notes:

1) $V_{REF} = V_{DD}/2$
2) C_L = 78 pF or equivalent (includes probe and jig capacitance).
3) I_{SRC} is set to -1 mA and I_{SNK} is set to +1 mA for t_{PHL} and t_{PLH} measurements.
4) Input signal from pulse generator: V_{IN} = 0.0V to V_{DD}; f ≤ 10 MHz; tr = 1.0 ns/V ±0.3 ns/V ±0.3 ns/V; tr and tf shall be measured from0.1 V_{DD} to 0.9 V_{DD} and from 0.9 V_{DD} to 0.1 V_{DD}, respectively.
5) Equivalent tst circuit means that DUT performance will be correlated and remain guaranteed to the applicable test circuit, above, whenever a test platform change necessitates a deviation from the applicable test circuit.

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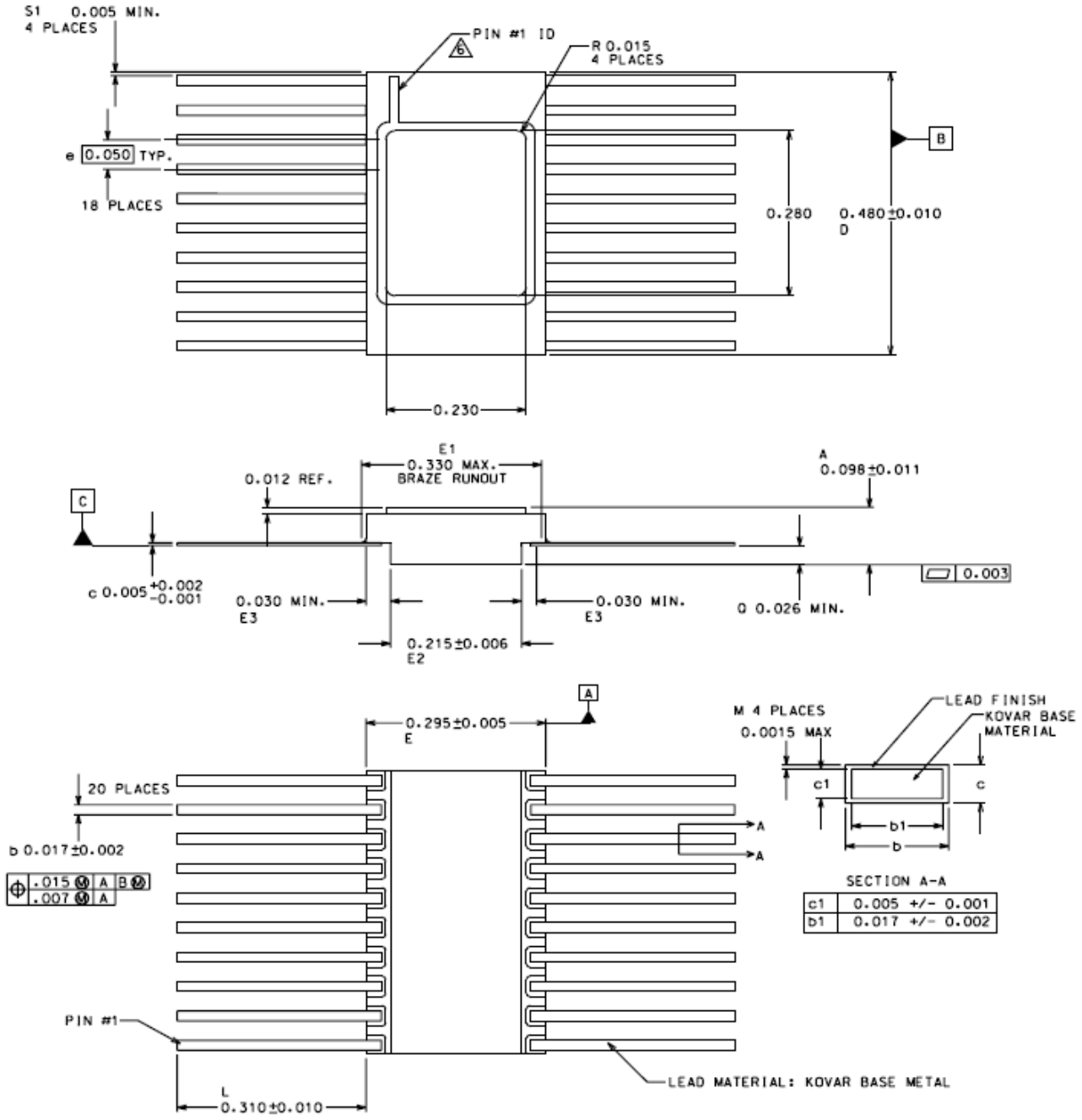

Figure 5. 20-lead Ceramic Flatpack

Notes:

1) All exposed metalized areas must be gold plated over electrically plated nickel per MIL-PRF-38535.
2) The lid is electrically connected to VSS.
3) Lead finishes are in accordance with MIL-PRF-38535.
4) Dimensions symbology is in accordance with MIL-PRF-38535.
5) Lead position and coplanarity are not measured
6) ID mark symbol is vendor option: No Alphanumerics.

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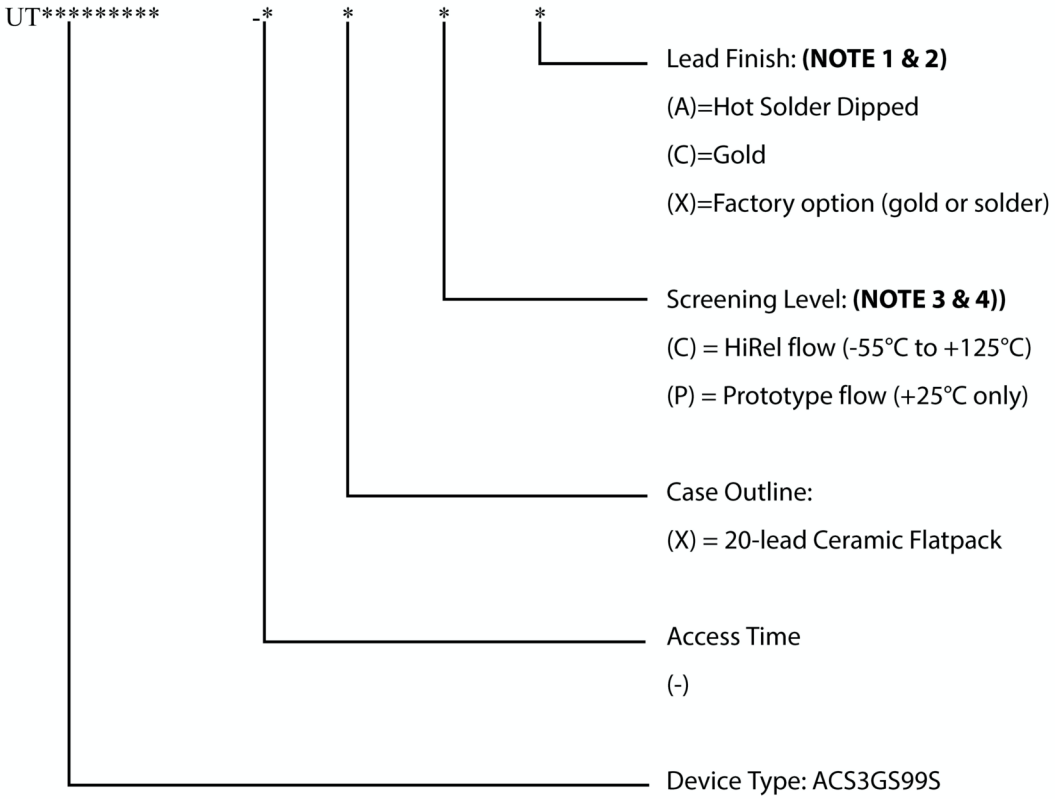

Notes:

1) Lead finish (A, C, or X) must be specified.
2) If an "X" is specified when ordering, then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3) Prototype flow per CAES Manufacturing Flows Document. Tested at 25°C only. Lead finish is GOLD ONLY. Radiation neither tested nor guaranteed.
4) HiRel Temperature Range flow per CAES Manufacturing Flows Document. Devices are tested at -55°C, room temp, and +125°C. Radiation neither tested nor guaranteed.

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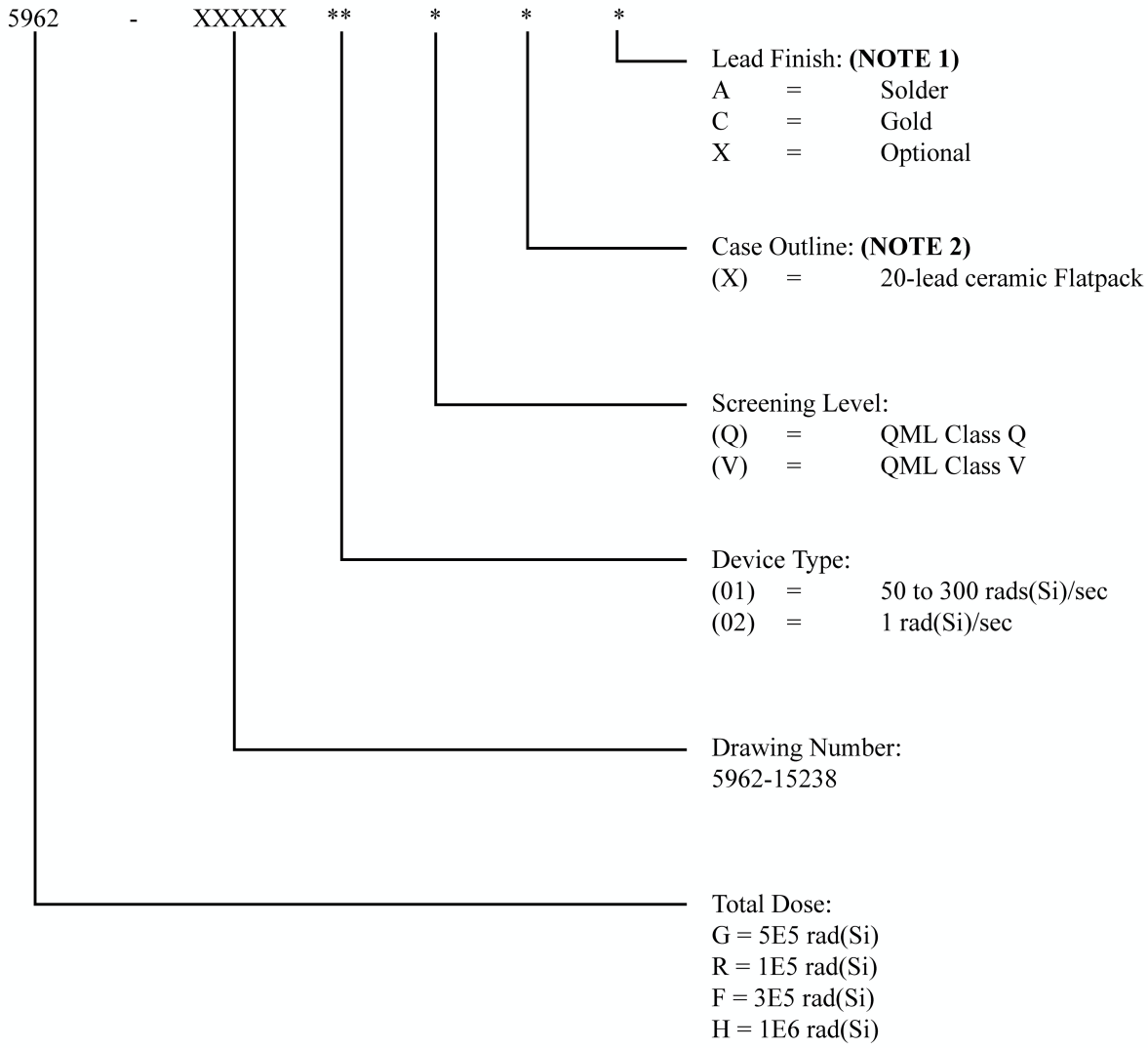

Notes:

1) Lead finish (A, C, or X) must be specified.
2) If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3) Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening. For prototype inquiries, contact factory.
4) Device Type 02 is only offered with a TID tolerance guarantee of 1E6 rads(Si) and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A and section 3.11.2. Device type 01 is only offered with a TID tolerance guarantee of 1E5 rads(Si), 3E5 rads(Si), and 5E5 rads(Si), and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A.

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Data Sheet Revision History

REV	Revision Date	Description of Change	Page(s)	Author
0.1.0	7/15	Posted Advanced Datasheet		Massey
0.2.0	10/15	Table 7-8-9 edits to existing logic diagrams. Added to Introduction.	1-6-7-8	Massey
0.3.0	12/15	Added Device Type 02 to the DC Characteristics table and order information	10-11-12-16	Massey
0.4.0	1/16	Replaced Figure 3	12	Massey
1.0.0	4/16	QML Q&V qualified	1	Massey

DATASHEET

RELEASED 4/16

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Datasheet Definitions

	DEFINITION
Advanced Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet **is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final**.
Preliminary Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

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