Dual, Sequential, ManyGate Configurable Logic Gate

UT54ACS2S99S

Features

- Voltage Supply: 3.0V to 5.5V
- Advanced CMOS technology
- Schmitt Trigger Inputs
- Tri-State Outputs
- ESD rating HBM: 2000V, Class 2
- Operational environment:
  - Total dose: 1 Mrad(Si)
  - Latchup immune (LET <= 100 MeV-cm2/mg)
- Packaging:
  - 20-lead flatpack
- Standard Microelectronics Drawing (SMD) - 5962-15239
  - QML Q, V

Introduction

The UT54ACS2S99S is CAES Dual, Sequential, ManyGate Configurable Logic Gate with Schmitt Trigger inputs and Tri-State outputs. The output-enable pin /OE1(2) is active LOW. The logic state of the 4 inputs determines the output state when /OE1(2) is LOW. When /OE1(2) is HIGH, the outputs are disabled. Setting /CLR1(2) to LOW drives output Y1(2) LOW. Setting /PRE1(2) to LOW drives the output on Y1(2) HIGH.

The ManyGate device logic functions are pin configurable by applying either a logic HIGH (VDD) or LOW (VSS) to the logic input pins as noted. The combinatorial logic function for each block, as shown in Figure 1, is determined by the input logic configuration as per Tables 2-11. The D-Flip Flop D input is transferred to the Q output (Y1) on the positive-going CLK1 edge (1F99S). The D-Transparent Latch D input is latched at the Q output (Y2) when CLK2 is LOW (1L99S). The Latch is transparent when CLK2 is HIGH.

Configuring the respective combinatorial logic blocks as a non-inverting buffer provides either a single D-Flip flop (1F99S), or transparent latch (1L99S).

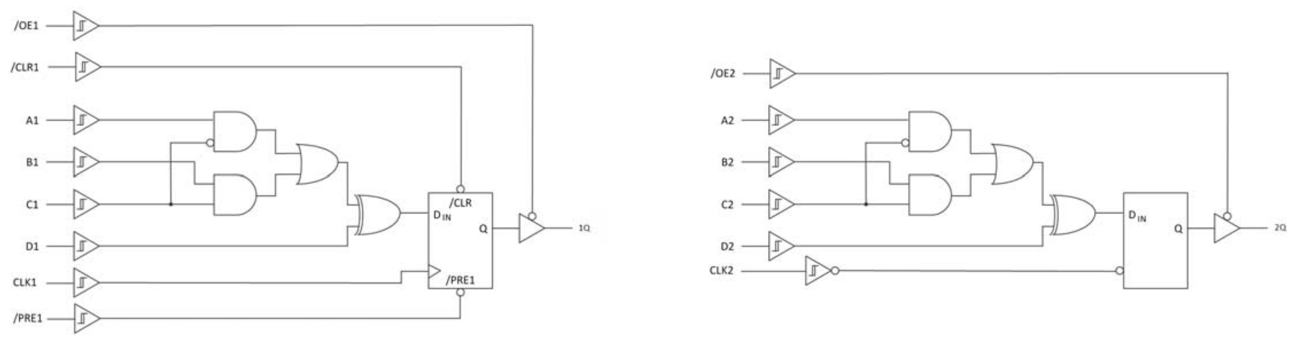


Figure 1. UT54ACS2S99S Options Block Diagrams; Left: 1F99
D-Flip Flop Gate1; Right: 1L99 Transparent Latch Gate2

Dual, Sequential, ManyGate Configurable Logic Gate

UT54ACS2S99S

1 Pin Definition/Description

Table 1. Pin Naming

Pin No.	Name	Description
3, 13	/OEn	Active LOW output enable
5, 15	An	A input
6, 16	Bn	B input
7, 17	Cn	C input
8, 18	Dn	D input
9, 19	nQ	3-State Output
1	/CLRn	Clear active LOW
2	/PREn	Preset active LOW
4, 14	CLKn	Clock
20	V_{DD}	Power supply pin
10	V_{SS}	Ground pin
11, 12	NC	Electrically unconnected on package

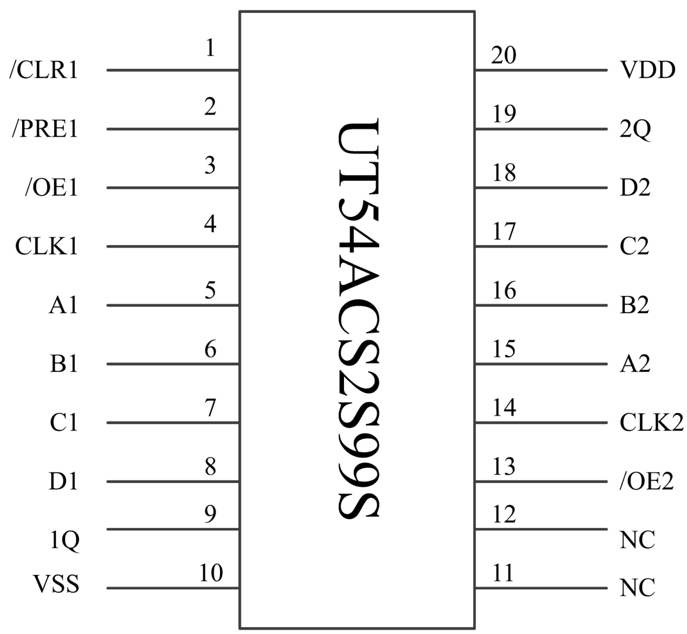


Figure 2. UT54ACS2S99S Pinout Diagram

2 Functional Truth Tables and Operational Modes

Table 2. Combinatorial Truth Table An, Bn, Cn, Dn to input (D_{IN}) of Storage Element

Dn	Cn	Bn	An	Output to D_{IN}
L	L	L	L	L
L	L	L	H	H
L	L	H	L	L
L	L	H	H	H
L	H	L	L	L
L	H	L	H	L
L	H	H	L	H
L	H	H	H	H
H	L	L	L	H
H	L	L	H	L
H	L	H	L	H
H	L	H	H	L
H	H	L	L	H
H	H	L	H	H
H	H	H	L	L
H	H	H	H	L

Table 3. Functional State Table for 1F99S D-Flip Flop

Inputs					Output
/OE1	/PRE	/CLR	CLK	A1, B1, C1, D1	1Q
L	L	H	X	X	H
L	H	L	X	X	L
L	L	L	X	X	H[1]
L	H	H	↑	Per Table 2	D_{IN}
L	H	H	L	X	Q_0
H	X	X	X	X	Z

Note:

1) The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at preset and clear are near V_{IL} maximum. In addition, this configuration is non-stable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

Table 4. Functional State Table for 1L99S Transparent Latch

Combination of Inputs			Output
/OE2	CLK2	(A2, B2, C2, D2)	2Q
L	H	Per Table 2	D_{IN}
L	L	X	Q_0
H	X	X	Z

3 Applications Info For 1F99 and 1L99 Options

Table 5. Equivalent Logic Functions Created from Table 2

Primary Logic Function	Complementary Logic Function	Table
3-state buffer		6
3-state inverter		7
3-state 2-in-1 data selector MUX		8
3-state 2-in-1 data selector MUX, inverted out		8
3-state 2-input AND	3-state 2-input NOR, both inputs inverted	9
3-state 2-input AND, one input inverted	3-state 2-input NOR, one input inverted	9
3-state 2-input AND, both inputs inverted	3-state 2-input NOR	9
3-state 2-input NAND		12
3-state 2-input NAND, one input inverted	3-state 2-input OR, one input inverted	13
3-state 2-input NAND, both inputs inverted	3-state 2-input OR	14
3-state 2-input XOR		15

Table 6. 3-State Buffer Functions

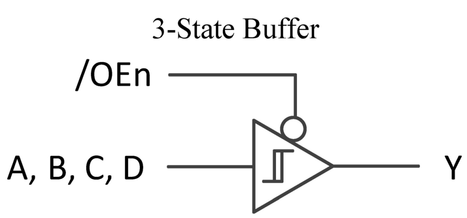
Function	A	B	C	D
	Input	X	L	L
	X	Input	H	L
	L	H	Input	L
	H	L	Input	H
	H	X	L	Input
	X	L	H	Input
	L	L	X	Input

Table 7. 3-State Inverter Buffer Functions

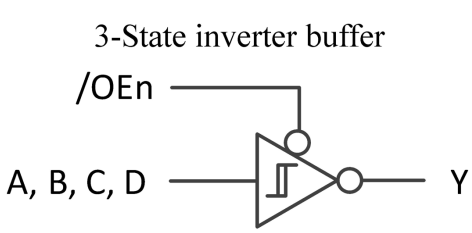
Function	A	B	C	D
	Input	X	L	H
	X	Input	H	H
	L	H	Input	H
	H	L	Input	L
	H	X	L	Input
	X	H	H	Input
	H	H	X	Input

Table 8. 3-State MUX Functions

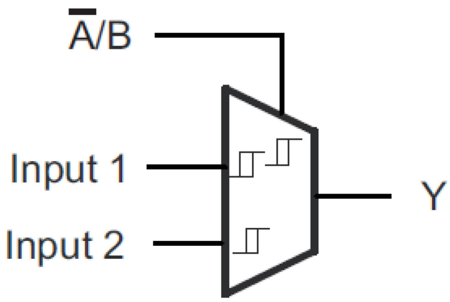
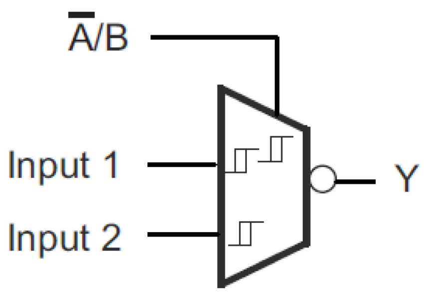
Function	A	B	C	D
3-State 2-to-1, Data Selector Mux 	Input 1 or Input 2	Input 1 or Input 2	Input 1 or Input 2	L
3-State 2-to-1, Data Selector Mux, Inverted Out 	Input 1 or Input 2	Input 1 or Input 2	Input 1 or Input 2	H

Table 9. 3-State AND/NOR Functions

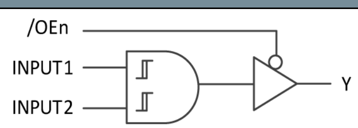
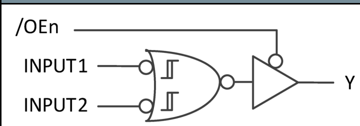
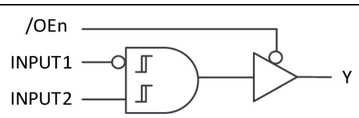
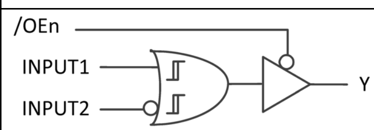
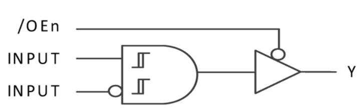
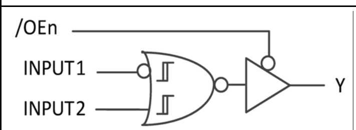
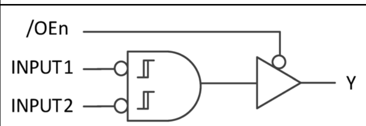
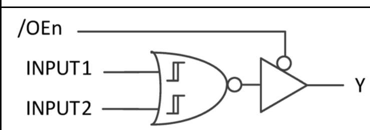
#IN	AND	NOR	A	B	C	D
2			L L	Input 1 Input 2	Input 2 Input 1	LL
2			Input 2 H	L Input 1	Input 1 Input 2	LH
2			Input 1 H	L Input 2	Input 2 Input 1	LH
2			Input 1 Input 2	H H	Input 2 Input 1	HH

Table 10. 3-state AND/NAND Functions

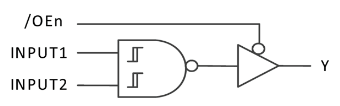
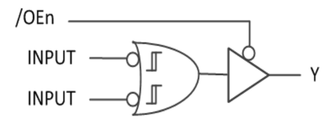
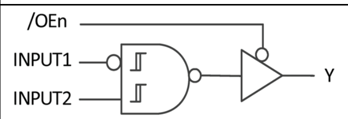
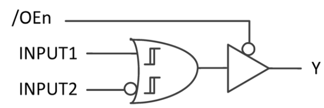
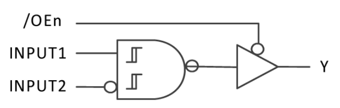
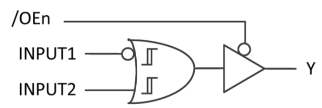
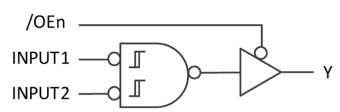
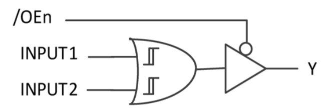
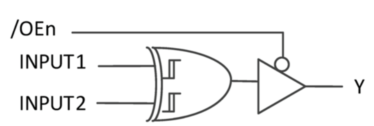
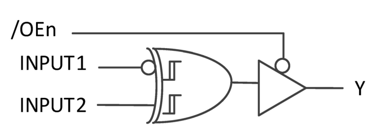
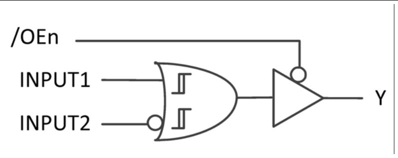
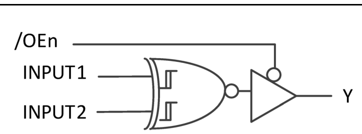
#IN	NAND	OR	A	B	C	D
2			L L	Input 1 Input 2	Input 2 Input 1	H H
2			Input 2 H	L Input 1	Input 1 Input 2	H L
2			Input 1 H	L Input 2	Input 2 Input 1	H L
2			Input 1 Input 2	H H	Input 2 Input 1	L L

Table 11. 3-State XOR/XNOR Functions

#IN	XOR/XNOR Function	A	B	C	D
2		Input 1 Input 2	X X	L L	Input 2 Input 1
		X X	Input 1 Input 2	H H	Input 2 Input 1
		L L	H H	Input 1 Input 2	Input 2 Input 1
2		H	L	Input 1	Input 2
2		H	L	Input 1	Input 2
2		H H	L L	Input 1 Input 2	Input 2 Input 1

4 Operational Environment

Table 12. Radiation

Parameter	Limit	Units
Total Ionizing Dose (TID)	1.0E6	rad(Si)
Single Event Latchup (SEL)	>100	MeV-cm^2/mg
Neutron Fluence [1]	1.0E13	n/cm^2

Note:

1) Guaranteed By Characterization

5 Absolute Maximum Ratings

Table 13. Absolute Maximum Ratings Table [1]

Symbol	Parameter	Limit	Unit
V_{DD}	Positive Output Supply Voltage	-0.3 to 7.0	V
V_{IO}	Voltage on an Input pin during operation	-0.3 to (V_{DD}+ 0.3V)	V
$I_{I/O}$	DC input/output Current	+/-10	mA
Θ_{JC}	Thermal resistance, junction-to-case	15	°C/W
T_J	Junction Temperature [2]	+175°C	°C
T_{STG}	Storage Temperature	-65°C to+150°C	°C
P_D [3]	Maximum package power dissipation permitted at T_C=125°C	1	W

Notes:

1) Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2) Maximum junction temperature may be increased to +175°C during burn-in and life test.
3) Test per MIL-STD-883, Method 1012.

6. Recommended Operating Conditions

Table 14. Recommended Operating Conditions Table

Symbol	Parameter	Limit	Unit
V_{DD}	Positive Output Supply Voltage	3.0 to 5.5	V
V_{IN}	Input Voltage on any pin	0.0 to VDD	V
T_C	Case Temperature Range	-55 to +125	°C
t_R, t_F	Input Rise/Fall time (0.1 V_{DD}-0.9 V_{DD})	<1	sec

7 3.3V DC Characteristics

(V_{DD}= 3.3V ± 0.3V, -55°C < T_C < +125°C); Unless otherwise noted, T_C is per the temperature range ordered

For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

Table 15. 3.3V DC Electrical Characteristics Table,,

Symbol	Parameter	Condition	MIN	MAX	Unit
V_{T+}	Positive going input voltage threshold [1]			0.7*V_{DD}	V
V_{T-}	Negative going input voltage threshold [1]		0.3*V_{DD}		V
V_H	Hysteresis Voltage		0.3		V
V_{OL}	Low-level output voltage [2]	I_{OL} = 100μA		0.25	V
V_{OH}	High-level output voltage [2]	I_{OH} = -100μA	V_{DD} – 0.25		V
I_{IN}	Input leakage current	V_{IN} = V_{DD} or V_{SS}	-1	+1	μA
I_{OS}	Output Short Circuit Current [3, 4]	V_{OUT} = V_{DD} and V_{SS}	-200	+200	mA
I_{OL}	Low level output current (sink) [5]	V_{IN} = V_{DD} or V_{SS} V_{OL} = 0.4V	8		mA
I_{OH}	High level output current (source) [5]	V_{IN} = V_{DD} or V_{SS} V_{OH} = V_{DD} - 0.4V	-8		mA
I_{OZ}	Output Three-State Current	V_{OUT} = V_{DD} and V_{SS}	-5	+5	μA
I_{DDQ}	Quiescent Supply Current Pre-Rad (Device Type 01 & 02)	V_{IN} = V_{DD} or V_{SS} V_{DD} = V_{DD} MAX		10	μA
	Quiescent Supply Current Post-Rad (Device Type 01)			25	μA
	Quiescent Supply Current Post-Rad (Device Type 02)			130	μA
P_{total}	Power dissipation [5, 6]	C_L = 78pF		3.5	mW/MHz
C_{IN}	Input capacitance [7]			15	pF
C_{OUT}	Output capacitance [7]			15	pF

Notes:

1) Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: VIH = VIH(min) + 20%, - 0%; VIL = VIL(max) + 0%, - 50%, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to VIH(min) and VIL(max).
2) Per MIL-PRF-38535, for current density <=5.0E5 amps/cm2, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765pF/MHz.
3) Supplied as a design limit but not guaranteed or tested.
4) Not more than one output may be shorted at a time for maximum duration of one second.
5) Guaranteed by characterization but not tested.
6) Power dissipation specified per switching output.
7) Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and VSS at frequency of 1MHz and a signal amplitude of 50mV rms maximum.

8 5.0V DC Characteristics

(V_{DD}= 5.0V ± 0.5V, -55°C < T_C < +125°C); Unless otherwise noted, T_C is per the temperature range ordered

Table 16. 5V DC Electrical Characteristics Table

Symbol	Parameter	Condition	MIN	MAX	Unit
V_{T+}	Positive going input voltage threshold [1]			0.7*V_{DD}	V
V_{T-}	Negative going input voltage threshold [1]		0.3*V_{DD}		V
V_H	Hysteresis Voltage Range		0.3		V
V_{OL}	Low-level output voltage [2]	I_{OL} = 100μA		0.25	
V_{OH}	High-level output voltage [2]	I_{OH} = -100μA	V_{DD} – 0.25		V
I_{IN}	Input leakage current	V_{IN} = V_{DD} or GND	-1	+1	μA
I_{OS}	Output Short Circuit Current [3, 4]	V_{OUT} = V_{DD} and V_{SS}	-300	+300	mA
I_{OL}	Low level output current (sink) [5]	V_{IN} = V_{DD} or V_{SS} V_{OL} = 0.4V	12		mA
I_{OH}	High level output current (source) [5]	V_{IN} = V_{DD} or V_{SS} V_{OH} = V_{DD} - 0.4V	-12		mA
I_{OZ}	Output Three-State Current	V_{OUT} = V_{DD} and V_{SS}	-5	+5	μA
I_{DDQ}	Quiescent Supply Current Pre-Rad (Device Type 01 & 02)	V_{IN} = V_{DD} or V_{SS} V_{DD} = V_{DD} MAX		10	μA
	Quiescent Supply Current Post-Rad (Device Type 01)			25	μA
	Quiescent Supply Current Post-Rad (Device Type 02)			130	μA
P_{total}	Power dissipation [5, 6]	C_L = 78pF		3.5	mW/MHz
C_{IN}	Input capacitance [7]			15	pF
C_{OUT}	Output capacitance [7]			15	pF

Notes:

1) Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: VIH = VIH(min) + 20%, - 0%; VIL = VIL(max) + 0%, - 50%, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to VIH(min) and VIL(max).
2) Per MIL-PRF-38535, for current density <=5.0E5 amps/cm2, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765pF/MHz.
3) Supplied as a design limit but not guaranteed or tested.
4) Not more than one output may be shorted at a time for maximum duration of one second.
5) Guaranteed by characterization but not tested.
6) Power dissipation specified per switching output.
7) Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz and a signal amplitude of 50mV rms maximum.

9 AC Electrical Characteristics

(V_{DD}= 3.0V to 5.5V, -55°C < T_C < +125°C); Unless otherwise noted, T_C is per the temperature range ordered

For Devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

Table 17. AC Electrical Table for the 1F99S D-Flip Flop

Symbol	Parameter	V_{DD}	Minimum	Maximum	Unit
t_{PHL1}	CLK1↑ - to 1Q	3.0V to 3.6V		21.5	ns
		4.5V to 5.5V		16	ns
t_{PLH1}	CLK1↑- to 1Q	3.0V to 3.6V		19.5	ns
		4.5V to 5.5V		14	ns
t_{PLH2}	/PRE1↓ to 1Q	3.0V to 3.6V		20	ns
		4.5V to 5.5V		14	ns
t_{PHL2}	/CLR1↓ to 1Q	3.0V to 3.6V		23	ns
		4.5V to 5.5V		17	ns
f_{MAX}	Maximum clock frequency	3.0V to 3.6V		46	MHz
		4.5V to 5.5V		62	MHz
t_{SU1}	A1-D1 setup time before CLK1 ↑	3.0V to 3.6V	7		ns
		4.5V to 5.5V	5		ns
t_{SU2}	/PRE1 or /CLR1 inactive Setup time before CLK1 ↑	3.0V to 3.6V	2		ns
		4.5V to 5.5V	2		ns
t_H	Data hold time after CLK1 ↑	3.0V to 3.6V	0		ns
		4.5V to 5.5V	0		ns
t_{W1}	Minimum pulse width CLK1 high or low	3.0V to 3.6V	6		ns
		4.5V to 5.5V	4.5		ns
t_{W2}	Minimum pulse width /PRE1 or /CLR1 low	3.0V to 3.6V	5		ns
		4.5V to 5.5V	4.5		ns

(V_{DD}= 3.0V to 5.5V, -55°C < T_C < +125°C); Unless otherwise noted, T_C is per the temperature range ordered

Table 18. AC Electrical Table for the 1L99S Transparent Latch

Symbol	Parameter	Condition	Minimum	Maximum	Unit
t_{PLH1}	CLK2=H; A2 - D2 TO 2Q	3.0V to 3.6V		21.5	ns
		4.5V to 5.5V		16	ns
t_{PHL1}	CLK2=H A2 - D2 TO 2Q	3.0V to 3.6V		24.5	ns
		4.5V to 5.5V		17.5	ns
t_{PLH2}	CLK2 ↑ TO 2Q	3.0V to 3.6V		19	ns
		4.5V to 5.5V		14	ns
t_{PHL2}	CLK2 ↑ TO 2Q	3.0V to 3.6V		21.5	ns
		4.5V to 5.5V		16	ns
f_{MAX}	Maximum clock frequency	3.0V to 3.6V		46	ns
		4.5V to 5.5V		62	ns
t_{SU}	Data setup time before CLK2 ↓	3.0V to 3.6V	8		ns
		4.5V to 5.5V	5.5		ns
t_H	Data hold time after CLK2 ↓	3.0V to 3.6V	0		ns
		4.5V to 5.5V	0		ns
t_W	Minimum pulse width CLK2 ↑	3.0V to 3.6V	6		ns
		4.5V to 5.5V	5		ns

Table 19. AC Electrical Table for both the1L99S Transparent Latch and the 1F99S D-Flip Flop

Symbol	Parameter	Condition	Minimum	Maximum	Unit
t_{PZL}	/OEn low to nQ	3.0V to 3.6V		12.5	ns
		4.5V to 5.5V		9	ns
t_{PZH}	/OEn low to nQ	3.0V to 3.6V		14	ns
		4.5V to 5.5V		10	ns
tP_{LZ}	/OEn high to nQ three-state	3.0V to 3.6V		12	ns
		4.5V to 5.5V		10	ns
t_{PHZ}	/OEn high to nQ three-state	3.0V to 3.6V		16.5	ns
		4.5V to 5.5V		13	ns

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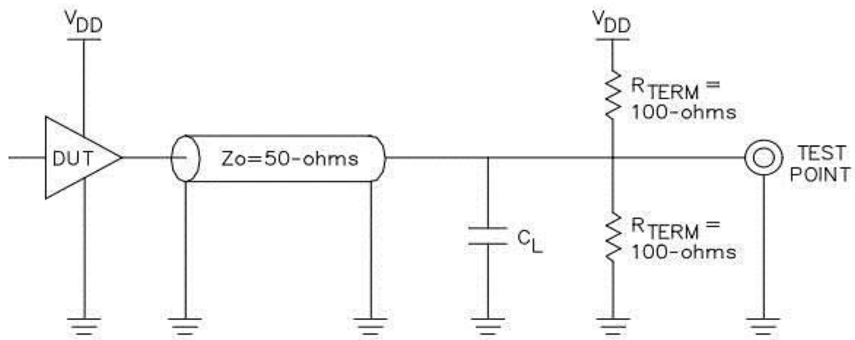
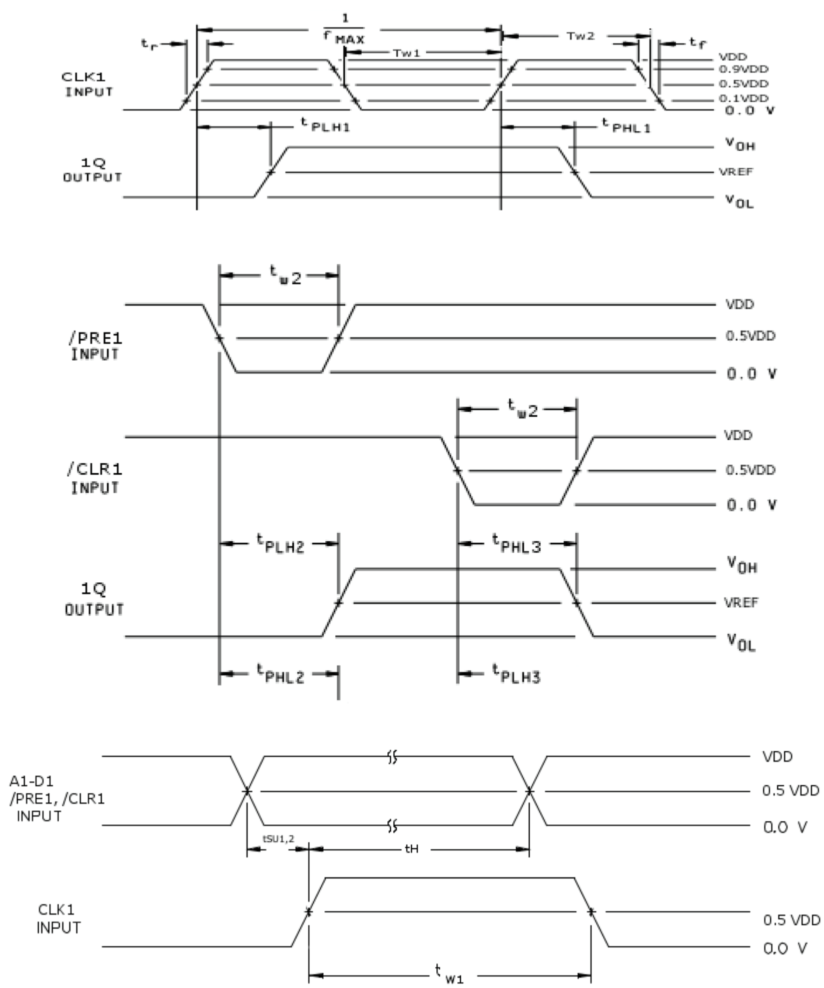


Figure 3. Equivalent Test Circuit

Note:

1) CL = 78 pF minimum or equivalent (includes scope probe and test socket). Measurement of data output occurs at the low to high or high to low transition mid-point, typically VDD/2.



1F99 D Flip Flop

Figure 4. 1F99 D Flip Flop Timing Diagram

Notes:

1) $V_{REF} = V_{DD}/2$
2) C_L = 78 pF or equivalent (includes test jig and probe capacitance).
3) I_{SRC} is set to -1.0 mA and I_{SNK} is set to 1.0 mA for t_{PHL} and t_{PLH} measurements
4) Input signal from pulse generator: V_{IN} = 0.0 V to V_{DD}; f ≤ 10 MHz; tR = 1.0 V/ns ±0.3 V/ns; tr = 1.0 V/ns ±0.3 V/ns; tr and tf shall be measured from 0.1 V_{DD} to 0.9 V_{DD} and from 0.9 V_{DD} to 0.1 V_{DD}, respectively.
5) Equivalent test circuit means that DUT performance will be correlated and remain guaranteed to the applicable test Circuit, above, whenever a test platform change necessitates a deviation from the applicable test circuit.

1L99 Transparent Latch

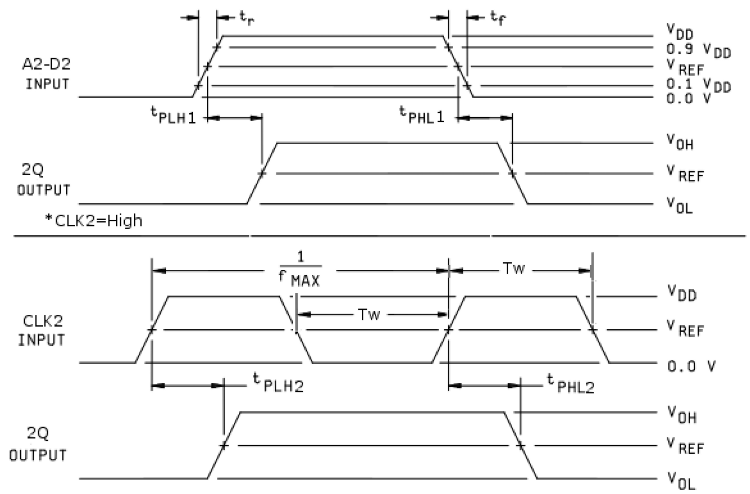


Figure 5 1L99 Transparent Latch Timing Diagram.

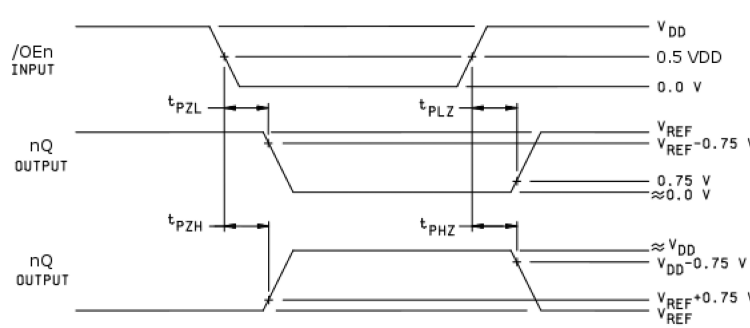


Figure 6 Output Enable and Disable Timing Diagrams.

Notes:

1) $V_{REF} = V_{DD}/2$
2) C_L = 78 pF or equivalent (includes test jig and probe capacitance).
3) I_{SRC} is set to -1.0 mA and I_{SNK} is set to 1.0 mA for t_{PHL} measurements
4) Input signal from pulse generator: V_{IN} = 0.0 V to V_{DD}; f ≤ 10 MHz; tR = 1.0 V/ns ±0.3 V/ns; tr = 1.0 V/ns ±0.3 V/ns; tr and tf shall be measured from 0.1 V_{DD} to 0.9 V_{DD} and from 0.9 V_{DD} to 0.1 V_{DD}, respectively.
5) Equivalent test circuit means that DUT performance will be correlated and remain guaranteed to the applicable test Circuit, above, whenever a test platform change necessitates a deviation from the applicable test circuit.

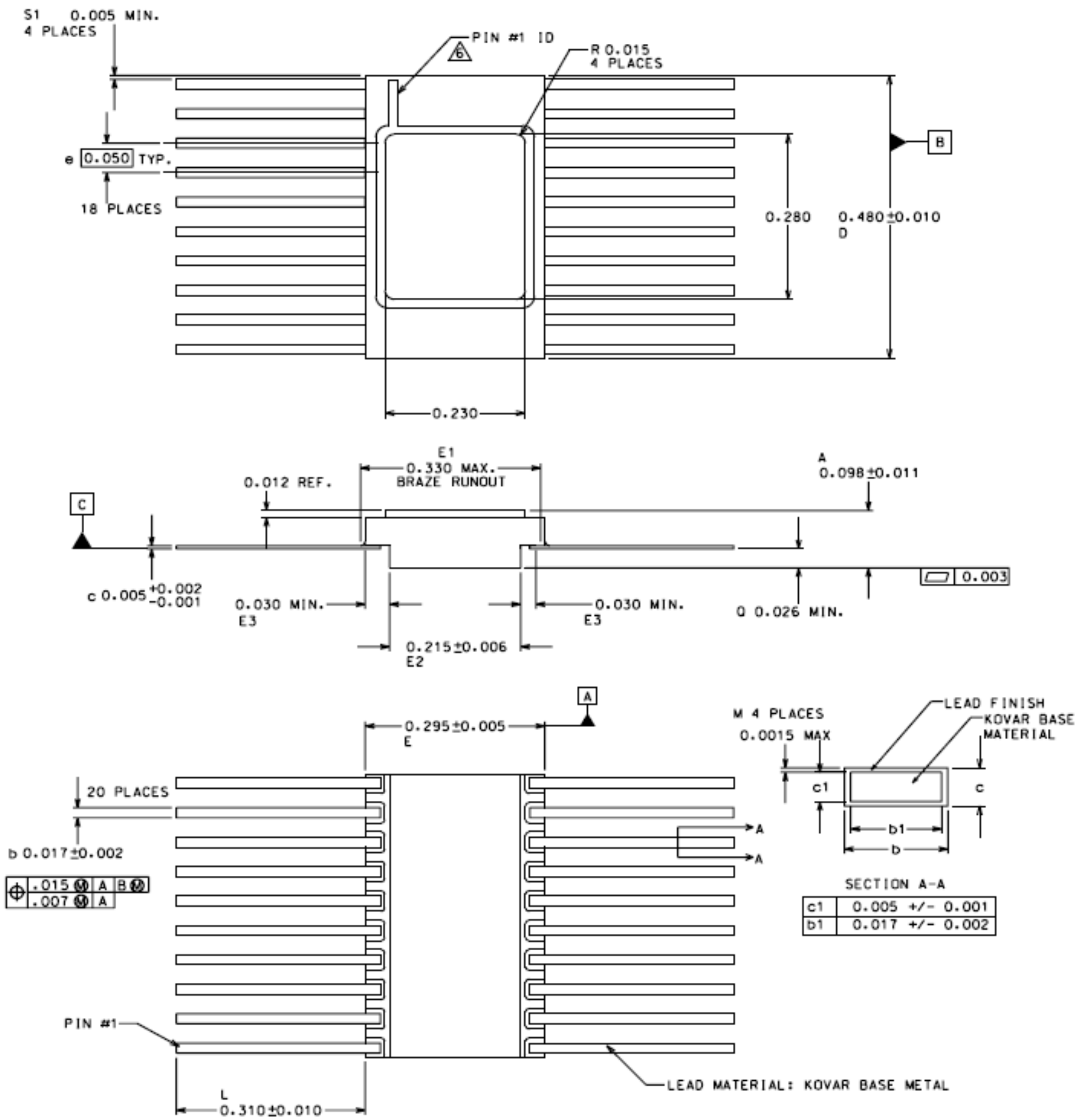


Figure 7. 20-lead Ceramic Flatpack

Notes:

1) All exposed metalized areas must be gold plated over electrically plated nickel per MIL-PRF-38535.
2) The lid is electrically connected to VSS.
3) Lead finishes are in accordance with MIL-PRF-38535.
4) Dimensions symbology is in accordance with MIL-PRF-38535.
5) Lead position and coplanarity are not measured
6) ID mark symbol is vendor option: No Alphanumerics.

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10 UT54ACS2S99S Sequential ManyGate Logic Gate

UT********* - * * * *

Lead Finish: **(NOTE 1 & 2)**
- (A)= Hot Solder Dipped
- (C)= Gold
- (X)= Factory option (gold or solder)

Screening Level: **(NOTE 3 & 4)**
- (C) = HiRel flow (-55°C to +125°C)
- (P) = Prototype flow (+25°C only)

Case Outline:
- (X) = 20-lead Ceramic Flatpack

Access Time
- (-)

Device Type: ACS2S99S

Notes:

1) Lead finish (A, C, or X) must be specified.
2) If an "X" is specified when ordering, then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3) Prototype flow per CAES Manufacturing Flows Document. Tested at 25°C only. Lead finish is GOLD ONLY. Radiation neither tested nor guaranteed.
4) HiRel Temperature Range flow per CAES Manufacturing Flows Document. Devices are tested at -55°C, room temp, and +125°C. Radiation neither tested nor guaranteed.

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11 UT54ACS2S99S Sequential ManyGate Logic Gate: SMD

5962- XXXXX ** * * *

Lead Finish: **(NOTE 1)**
A = Solder
C = Gold
X = Optional

Case Outline: **(NOTE 2)**
(X) = 20-lead Ceramic Flatpack

Screening Level: **(NOTE 3)**
(Q) = QML Class Q
(V) = QML Class V

Device Type: **(NOTE 4)**
(01) = 50 to 300 rads(Si)/sec
(02) = 1 rad(Si)/sec

Drawing Number:
5962-15239

Total Dose:
G = 5E5 rad(Si)
R = 1E5 rad(Si)
F = 3E5 rad(Si)
H= 1E6 rad(Si)

Notes:

1) Lead finish (A,C, or X) must be specified.
2) If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3) Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening. For prototype inquiries, contact factory.
4) Device Type 02 is only offered with a TID tolerance guarantee of 1E6 rads(Si) and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A and section 3.11.2. Device type 01 is only offered with a TID tolerance guarantee of 1E5 rads(Si), 3E5 rads(Si), and 5E5 rads(Si), and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A.

Dual, Sequential, ManyGate Configurable Logic Gate

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Data Sheet Revision History

REV	Revision Date	Description of Change	Page(s)	Author
0.1.0	7/15	Posted Advanced Datasheet		Massey
0.2.0	10/15	Table 9-10-11 edits to existing logic diagrams. Page 1 Added to Introduction.	1-6-7-8	Massey
0.3.0	12/15	Added Device Type 02 to the DC Characteristics table and order information. Corrected and added Note numbers to order information.	10-11-17-18	Massey
0.4.0	1/16	Replaced Figure 3	3	Massey
1.0.0	4.16	QML Q & V qualified	1	Massey

DATASHEET

RELEASED 5/16

Dual, Sequential, ManyGate Configurable Logic Gate

UT54ACS2S99S

Datasheet Definitions

	DEFINITION
Advanced Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet **is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final**.
Preliminary Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

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