DATASHEET

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Quadruple 2-Input NAND Gates

UT54ACS00E

Features

- 0.6µm CRH CMOS process
  - Latchup immune
- High speed
- Low power consumption
- Wide power supply operating ranges from 3.0V to 5.5V
- Available QML Q or V processes
- 14-lead flatpack
- UT54ACS00E - SMD 5962-96512

Description

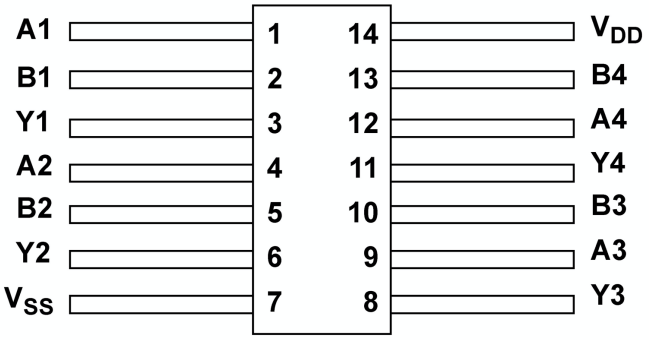
The UT54ACS00E is a performance and voltage enhanced version of the UT54ACS00 quadruple, two-input NAND gate. The circuit performs the Boolean functions $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The device is characterized over full military temperature range of -55°C to +125°C.

Function Table

Inputs		Output
A	B	Y
H	H	L
L	X	H
X	L	H

Pinout



14-Lead Flatpack
TopView

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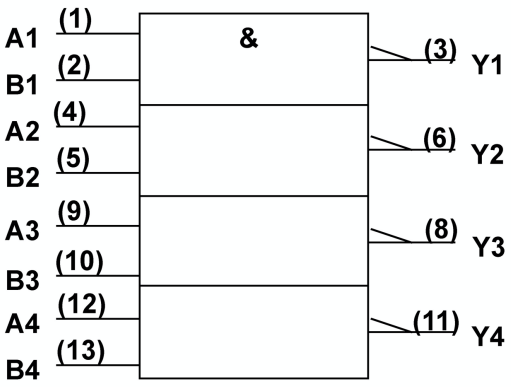
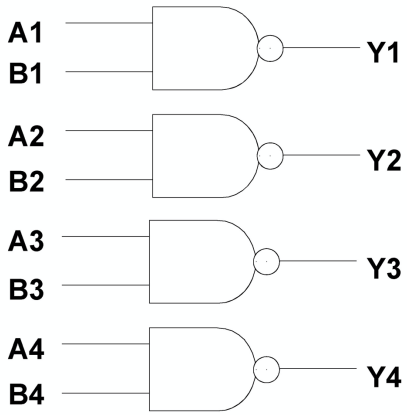
Logic Symbol



Note:

1) Logic symbol in accordance with ANSI/IEEE standard 91-1984 and IEC Publication 617-12.

Logic Diagram



Operational Environment [1]

Parameter	Limit	Units
Total Dose	1.0E6	rads(Si)
SEU Threshold [2]	108	MeV-cm^2/mg
SEL Threshold	120	MeV-cm^2/mg
Neutron Fluence	1.0E14	n/cm^2

Notes:

1) Logic will not latchup during radiation exposure within the limits defined in the table.
2) Device storage elements are immune to SEU affects.

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Absolute Maximum Ratings[1]

Symbol	Parameter	Limit	Units
V_{DD}	Supply voltage	-0.3 to 7.0	V
$V_{I/O}$	Voltage any pin	-0.3 to V_{DD} +0.3	V
T_{STG}	Storage Temperature range	-65 to +150	°C
T_J	Maximum junction temperature	+175	°C
T_{LS}	Lead temperature (soldering 5 seconds)	+300	°C
Θ_{JC}	Thermal resistance junction to case	15	°C/W
I_I	DC input current	±10	mA
P_D [2]	Maximum package power dissipation permitted @ Tc = +125°C	3.2	W

Notes:

1) Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2) Per MIL-STD-883, method 1012.1, Section 3.4.1, PD = ($T_{J(max)}$ - $T_{c(max)}$) / Θ_{JC}

Recommended Operating Conditions

Symbol	Parameter	Limit	Units
V_{DD}	Supply voltage	3.0 to 5.5	V
V_{IN}	Input voltage any pin	0 to V_{DD}	V
T_C	Temperature range	-55 to +125	°C

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DC Electrical Characteristics for the UT54ACS00E[7]

(V_{DD} = 3.0V to 5.5V; V_{SS} = 0V[6]; -55°C < Tc < +125°C)

Symbol	Description	Condition	MIN	MAX	Unit
V_{IL}	Low-level input voltage [1]	V_{DD} from 3.0V to 5.5V		0.3V_{DD}	V
V_{IH}	High-level input voltage [1]	V_{DD} from 3.0V to 5.5V	0.7V_{DD}		V
I_{IN}	Input leakage current	V_{IN} = V_{DD} or V_{SS}	-1	1	µA
V_{OL1}	Low-level output voltage [3]	I_{OL} = 100µA		0.25	V
V_{OH2}	High-level output voltage [3]	I_{OH} = -100µA	V_{DD} - 0.25		V
I_{OS1}	Short-circuit output current [2, 4]	V_O = V_{DD} and V_{SS} V_{DD} from 4.5V to 5.5V	-200	+200	mA
I_{OS2}	Short-circuit output current [2, 4]	V_O = V_{DD} and V_{SS} V_{DD} from 3.0V to 3.6V	-100	+100	mA
I_{OL1}	Low level output current [10]	V_{IN} = V_{DD} or V_{SS} V_{OL} = 0.4V V_{DD} from 4.5V to 5.5V	+8		mA
I_{OL2}	Low level output current [10]	V_{IN} = V_{DD} or V_{SS} V_{OL} = 0.4V V_{DD} from 3.0V to 3.6V	+6		mA
I_{OH1}	High level output current [10]	V_{IN} = V_{DD} or V_{SS} V_{OH} = V_{DD}-0.4V V_{DD} from 4.5V to 5.5V	-8		mA
I_{OH2}	High level output current[10]	V_{IN} = V_{DD} or V_{SS} V_{OH} = V_{DD}-0.4V V_{DD} from 3.0V to 3.6V	-6		mA
P_{total1}	Power dissipation [2, 8, 9]	C_L = 50pF V_{DD} = 4.5V to 5.5V		1.0	mW/ MHz
P_{total2}	Power dissipation [2, 8, 9]	C_L = 50pF V_{DD} = 3.0V to 3.6V		0.5	mW/ MHz
I_{DDQ}	Quiescent Supply Current	V_{DD} =5.5V		25	µA
C_{IN}	Input capacitance [5]	f = 1MHz V_{DD} = 5V		15	pF
C_{OUT}	Output capacitance [5]	f= 1MHz V_{DD} = 0V		15	pF

Notes:

1) Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: V_{IH} = V_{IH}(min) + 20%, - 0%; V_{IL} = V_{IL}(max) + 0%, - 50%, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to V_{IH}(min) and V_{IL}(max).
2) Supplied as a design limit but not guaranteed or tested.
3) Per MIL-PRF-38535, for current density ≤5.0E5 amps/cm^2, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765pF/ MHz.
4) Not more than one output may be shorted at a time for maximum duration of one second.
5) Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz and a signal amplitude of 50mV rms maximum.
6) Maximum allowable relative shift equals 50mV.

7) For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 method 1019 condition A up to the maximum TID level procured.
8) Power dissipation specified per switching output.
9) Power does not include power contribution of any TTL output sink current.
10) Guaranteed by characterization, but not tested.

AC Electrical Characteristics for the UT54ACS00E[2]

(V_{DD} = 3.0V to 5.5V; V_{SS} = 0V[1]; -55°C < Tc < +125°C)

Symbol	Parameter	Condition	V_{DD}	Minimum	Maximum	Unit
t_{PLH}	Input to Yn	C_L = 50pF	4.5V to 5.5V	1	6	ns
			3.0V to 3.6V	1	8	
t_{PHL}	Input to Yn	C_L = 50pF	4.5V to 5.5V	1	7	ns
			3.0V to 3.6V	1	9	

Notes:

1) Maximum allowable relative shift equals 50mV.
2) For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 method 1019 condition A up to the maximum TID level procured.

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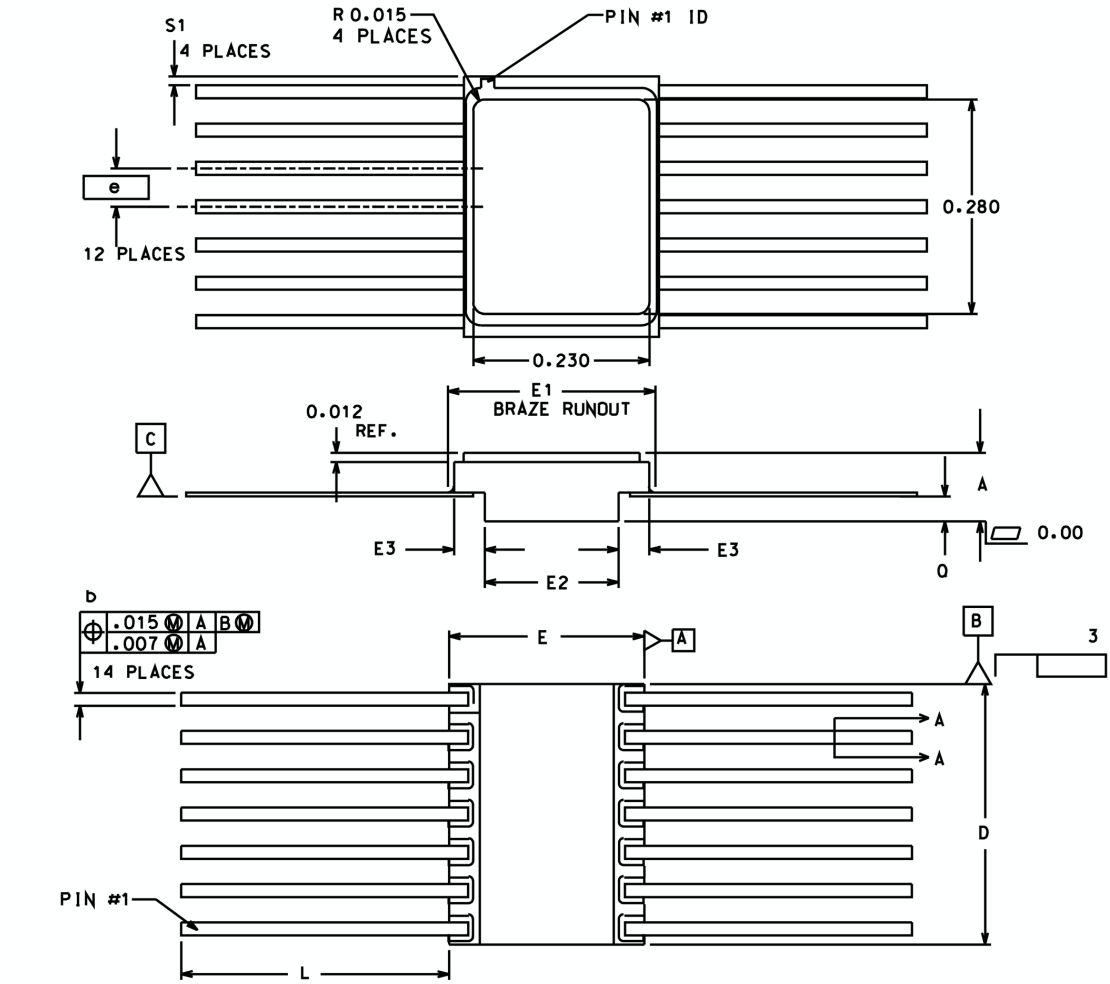
Packaging



DIM	INCH MIN.	INCH MAX.	MILLIMETER MIN.	MILLIMETER MAX.
A	0.079	0.101	2.007	2.575
b	0.015	0.019	0.381	0.483
c	0.004	0.006	0.102	0.152
D	0.333	0.347	8.438	8.814
E	0.250	0.260	6.350	6.604
E1	-----	0.290	-----	7.366
E2	0.170	0.180	4.318	4.572
E3	0.030	-----	0.762	-----
e	0.050 BSC		1.270 BSC	
L	0.340	0.360	8.636	9.144
Q	0.026	-----	0.660	-----
S1	0.005	-----	0.127	-----

Figure 1. 14 Lead Flatpack

Notes:

1) All exposed metallized areas are gold plated over electroplated nickel per MIL-PRF-38535.
2) The lid is electrically connected to V_{SS}.
3) Lead finishes are in accordance with MIL-PRF-38535.
4) Dimension symbol is in accordance with MIL-PRF-38533.
5) Lead position and coplanarity are not measured.

Quadruple 2-Input NAND Gates

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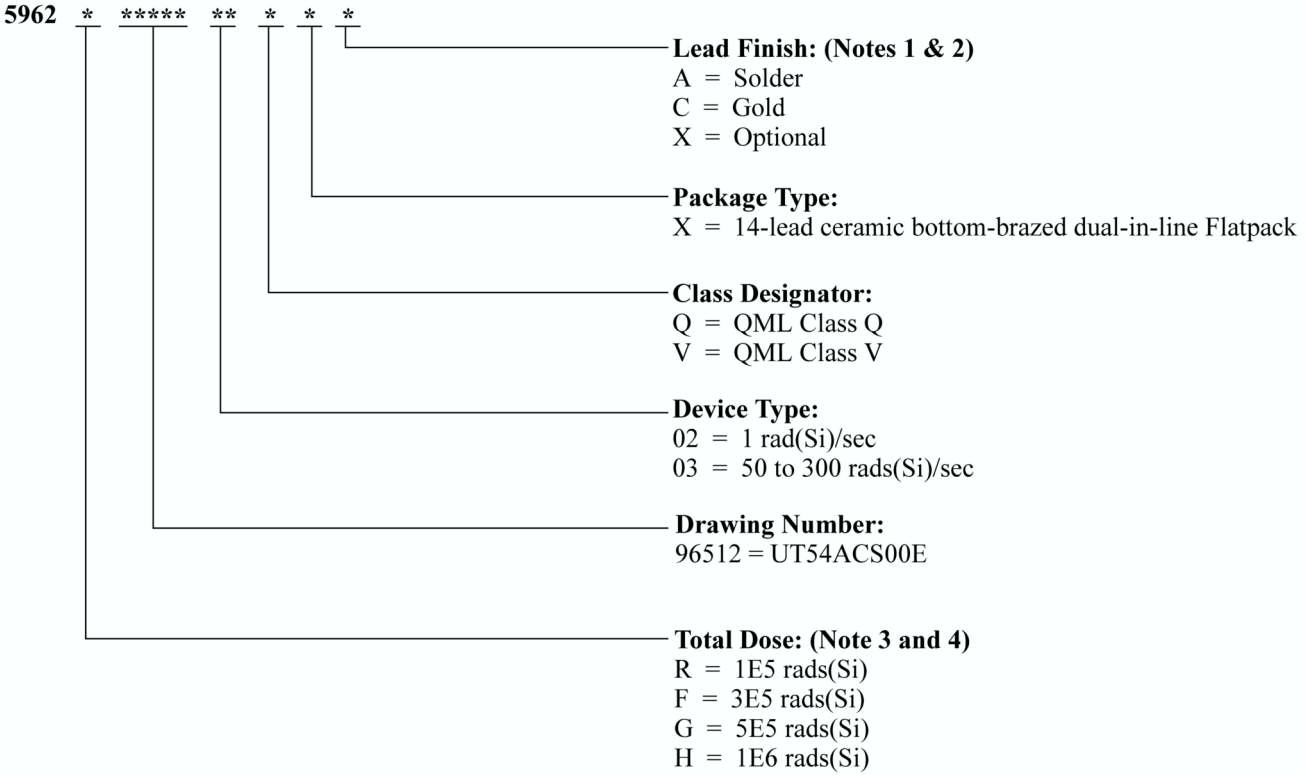
Ordering Information: UT54ACS00E: SMD



Notes:

1) Lead finish (A, C, or X) must be specified.
2) If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3) Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening. For prototype inquiries, contact factory.
4) Device type 02 is only offered with a TID tolerance guarantee of 3E5 rads(Si) or 1E6 rads(Si) and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A and section 3.11.2. Device type 03 is only offered with a TID tolerance guarantee of 1E5 rads(Si), 3E5 rads(Si), and 5E5 rads(Si), and is tested in accordance with MIL-STD-883 Test Method 1019 Condition A.

Datasheet Revision History

Revision Date	Description of Change
March 2015 Version 1.0.0	Initial Release of Datasheet

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Datasheet Definitions

	DEFINITION
Advanced Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet **is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final**.
Preliminary Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

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