DATASHEET

RELEASED 04/2022

Radiation-Hardened 32K x 8 PROM

UT28F256LVQLE

Features

- Programmable, read-only, asynchronous, radiation-hardened, 32K x 8 memory
  - Supported by industry standard programmer
  - Programming yield estimated at 80% or greater (ref note on ordering page(s))
- 65ns maximum address access time (-55°C to+125°C)
- Three-state data bus
- Low operating and standby current
  - Operating: 50.0mA maximum @15.4 MHz
    - Derating: 1.7mA/MHz
  - Standby: 1.0mA maximum (post-rad)
- Radiation-hardened process and design; total dose irradiation testing to MIL-STD-883, Method 1019
  - Total dose: 100Krad to 1Megarad(Si)
  - Onset LET: 40 MeV-cm^2/mg
  - SEL Immune ≥110 MeV-cm^2/mg
- QML Q & V compliant part
  - AC and DC testing at factory
- No post-program conditioning required
- Packaging options:
  - 28-lead 50-mil center flatpack (0.490 x 0.74)
- V_{DD}: 3.0 to 3.6V
- Standard Microcircuit Drawing 5962-01517

Product Description

The UT28F256LVQLE amorphous silicon redundant Via Link™ PROM is a high performance, asynchronous, radiation-hardened, 32K x 8 programmable memory device. The UT28F256LVQLE PROM features fully asynchronous operation requiring no external clocks or timing strobes. An advanced radiation-hardened twin-well CMOS process technology is used to implement the UT28F256LVQLE. The combination of radiation-hardness, fast access time, and low power consumption make the UT28F256LQLE ideal for high speed systems designed for operation in radiation environments.

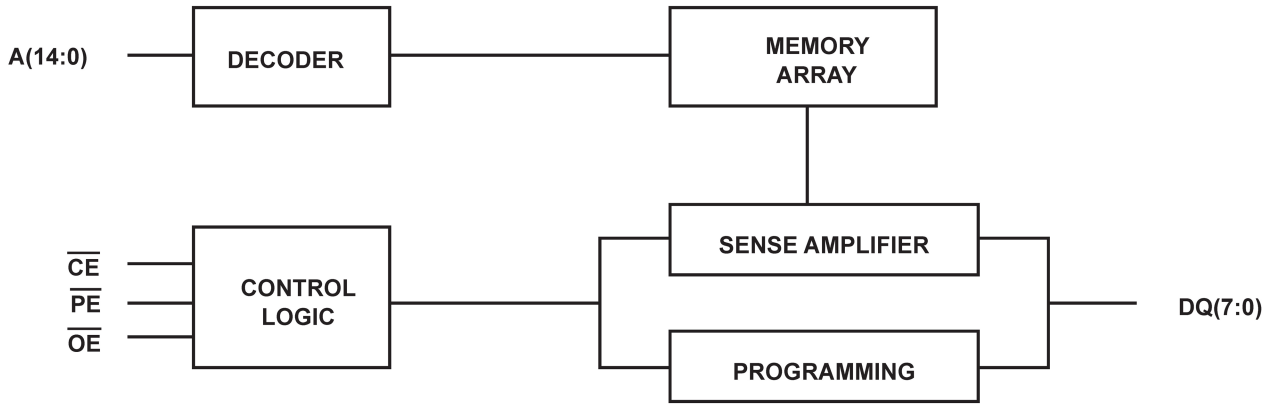

Figure 1. PROM Block Diagram

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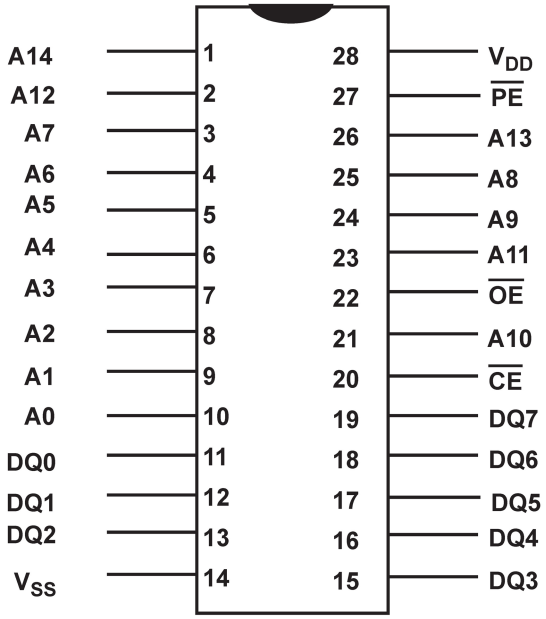
Device Operation

The UT28F256LVQLE has three control inputs: Chip Enable ($\overline{CE}$), Program Enable ($\overline{PE}$), and Output Enable ($\overline{OE}$); fifteen address inputs, A(14:0); and eight bidirectional data lines, DQ(7:0). $\overline{CE}$ is the device enable input that controls chip selection, active, and standby modes. Asserting $\overline{CE}$ causes I_{DD} to rise to its active value and decodes the fifteen address inputs to select one of 32,768 words in the memory. $\overline{PE}$ controls program and read operations. During a read cycle, $\overline{OE}$ must be asserted to enable the outputs.

Pin Configuration



Pin Names

A(14:0)	Address
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PE}$	Program Enable
DQ(7:0)	Data Input/Data Output

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Table 1. Device Operation Truth Table [1]

$\overline{OE}$	$\overline{PE}$	$\overline{CE}$	I/O Mode	Mode
X	1	1	Three-state	Standby
0	1	0	Data Out	Read
1	0	0	Data In	Program
1	1	0	Three-state	Read[2]

Notes:

1) "X" is defined as a "don't care" condition.
2) Device active; outputs disabled.

Absolute Maximum Ratings [1]

(Referenced to V_{SS})

Symbol	Parameter	Limits	Units
V_{DD}	DC supply voltage	-0.3 to 6.0	V
$V_{I/O}$	Voltage on any pin	-0.5 to (V_{DD} + 0.5)	V
T_{STG}	Storage Temperature	-65 to +150	°C
P_D	Maximum power dissipation	1.5	W
T_J	Maximum junction temperature	+175	°C
Θ_{JC}	Thermal resistance junction to case [2]	3.3	°C/W
I_I	DC input current	±10	mA

Notes:

1) Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating Only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2) Test per MIL-STD-883, Method 1012, infinite heat sink.

Recommended Operating Conditions

Symbol	Parameter	Limits	Units
V_{DD}	Positive supply voltage	3.0 to 3.6	V
T_C	Case temperature range	-5.5 to +125	°C
V_{IN}	DC input voltage	0 to V_{DD}	V

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DC Electrical Characteristics (Pre/Post-Radiation) *

(V_{DD} = 3.0V to 3.6V; -55°C < T_C < +125°C)

Symbol	Parameter	Condition	Minimum	Maximum	Unit
V_{IH}[5]	High-level input voltage		0.7V_{DD}		V
V_{IL}[5]	Low-level input voltage			0.25V_{DD}	V
V_{OL1}	Low-level output voltage	I_{OL} = 100µA, V_{DD} = 3.0V		V_{SS} + 0.05	V
V_{OL2}	Low-level output voltage	I_{OL} = 1.0mA, V_{DD} = 3.0V		V_{SS} + 0.10	V
V_{OH1}	High-level output voltage	I_{OH} = -100µA, V_{DD} = 3.0V	V_{DD} - 0.15		V
V_{OH2}	High-level output voltage	I_{OH} = -1.0mA V_{DD} = 3.0V	V_{DD} - 0.3		V
C_{IN}[1]	Input capacitance, all inputs except $\overline{PE}$ Input Capacitance $\overline{PE}$	f = 1MHz, V_{DD} = 3.3V V_{IN} = 0V		15 20	pF
C_{IO}[1]	Bidirectional I/O capacitance	f = 1MHz, V_{DD} = 3.3V V_{OUT} = 0V		15	pF
I_{IN}	Input leakage current	V_{IN} = 0V to V_{DD}, all pins except $\overline{PE}$ V_{IN} = V_{DD}, $\overline{PE}$ only	-3	+3 35	µA µA
I_{OZ}	Three-state output leakage current	V_O = 0V to V_{DD} V_{DD} = 3.6V $\overline{OE}$ = 3.6V	-8	+8	µA
I_{OS}[2,3]	Short-circuit output current	V_{DD} = 3.6V, V_O = V_{DD} V_{DD} = 3.6V, V_O = 0V	 -100	100	mA mA
I_{DD1}(OP)[4]	Supply current operating @15.4MHz (65ns product)	CMOS input levels (I_{OUT} = 0), V_{IL} = 0.2V, V_{DD}, $\overline{PE}$ = 3.6V, V_{IH} = 3.0V		50.0	mA
I_{DD2}(SB) post-rad	Supply current standby	CMOS input levels, V_{IL} = V_{SS} +0.25V $\overline{CE}$ = V_{DD} -025, V_{IH} = V_{DD} -0.25V		1.0	µA

Notes:

*Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019 at 1E6 rads(Si).

1) Measured only for initial qualification, and after process or design changes that could affect input/output capacitance.
2) Supplied as a design limit but not guaranteed or tested.
3) Not more than one output may be shorted at a time for maximum duration of one second.
4) 1.7mA/MHz.
5) V_{IL} and V_{IH} for input signals A6, A7, A8, A9, A12, A13 and A14 guaranteed by design.

Read Cycle

A combination of $\overline{PE}$ greater than V_{IH}(min), and $\overline{CE}$ less than V_{IL}(max) defines a read cycle. Read access time is measured from the latter of device enable, output enable, or valid address to valid data output.

An address access read is initiated by a change in address inputs while the chip is enabled with $\overline{OE}$ asserted and $\overline{PE}$ deasserted. Valid data appears on data output, DQ(7:0), after the specified t_{AVQV} is satisfied. Outputs remain active throughout the entire cycle. As long as device enable and output enable are active, the address inputs may change at a rate equal to the minimum read cycle time.

The chip enable-controlled access is initiated by $\overline{CE}$ going active while $\overline{OE}$ remains asserted, $\overline{PE}$ remains deasserted, and the addresses remain stable for the entire cycle. After the specified t_{ELQV} is satisfied, the eight-bit word addressed by A(14:0) appears at the data outputs DQ(7:0).

Output enable-controlled access is initiated by $\overline{OE}$ going active while $\overline{CE}$ is asserted, $\overline{PE}$ is deasserted, and the addresses are stable. Read access time is t_{GLQV} unless t_{AVQV} or t_{ELQV} have not been satisfied.

AC Electrical Characteristics Read Cycle (Post-Radiation)*

(V_{DD} = 3.0V to 3.6V; -55°C < T_C < +125°C)

Symbol	Parameter	28F256LV-65		Unit
		MIN	MAX	
t_{AVAV} [1]	Read cycle time	65		ns
t_{AVQV}	Read access time		65	ns
t_{AXQX} [2]	Output hold time	0		ns
t_{GLQX} [2]	$\overline{OE}$-controlled output enable time	0		ns
t_{GLQV}	$\overline{OE}$-controlled access time		35	ns
t_{GHQZ}	$\overline{OE}$-controlled output three-state time		35	ns
t_{ELQX} [2]	$\overline{CE}$-controlled output enable time	0		ns
t_{ELQV}	$\overline{CE}$-controlled access time		65	ns
t_{EHQZ}	$\overline{CE}$-controlled output three-state time		35	ns

Notes:

*Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019 at 1E6 rads(Si).

1) Functional test.
2) Three-state is defined as a 200mV change from steady-state output voltage.

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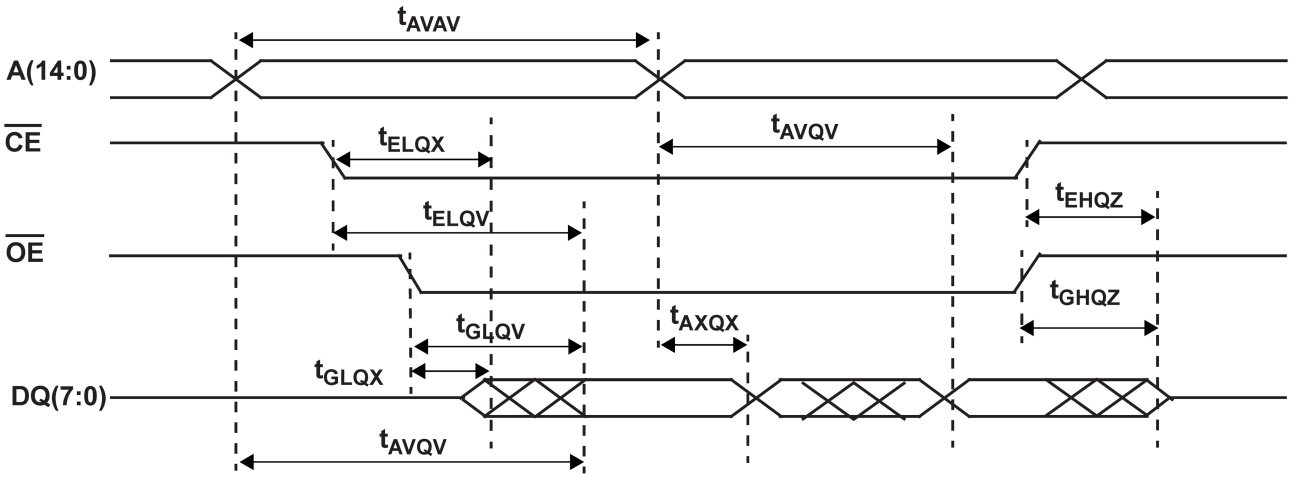

Figure 2. PROM Read Cycle

Radiation Hardness

The UT28F256LVQLE PROM incorporates special design and layout features which allow operation in high-level radiation environments. CAES has developed special low-temperature processing techniques designed to enhance the total-dose radiation hardness of both the gate oxide and the field oxide while maintaining the circuit density and reliability. For transient radiation hardness and latchup immunity, CAES builds all radiation-hardened products on epitaxial wafers using an advanced twin-tub CMOS process. In addition, CAES pays special attention to power and ground distribution during the design phase, minimizing dose-rate upset caused by rail collapse.

Radiation Hardness Design Specifications [1]

Total Dose	1E6	rad(Si)
Latchup LET Threshold	>110	MeV-cm^2/mg
Memory Cell LET Threshold	>100	MeV-cm^2/mg
Logic SEU Onset LET	>40	MeV-cm^2/mg
SEU Cross Section	2.5E-6	cm^2/device
Error rate - geosynchronous orbit, Adams 90% worst case environment	2.5E-12	errors/device day

Note:

1) The PROM will not latchup during radiation exposure under recommended operating conditions.

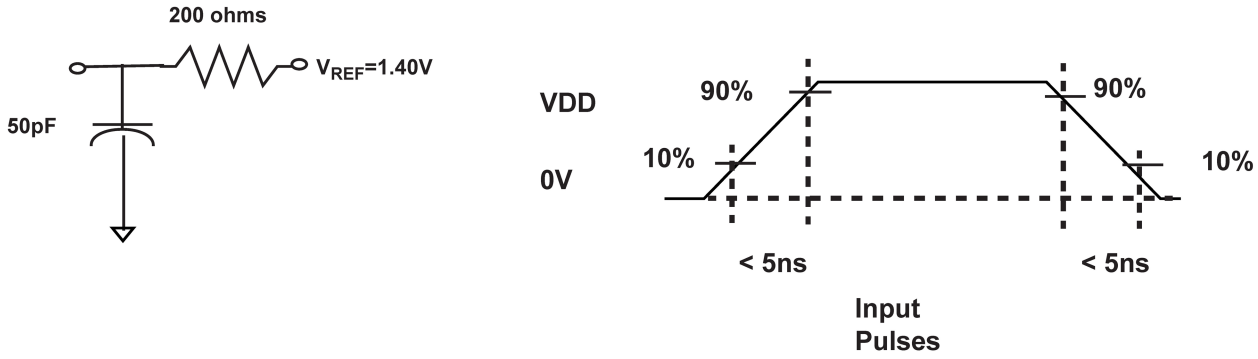

Figure 3. AC Test Loads and Input Waveforms

Notes:

1) 50pF including scope probe and test socket.
2) Measurement of data output occurs at the low to high or high to low transition mid-point.

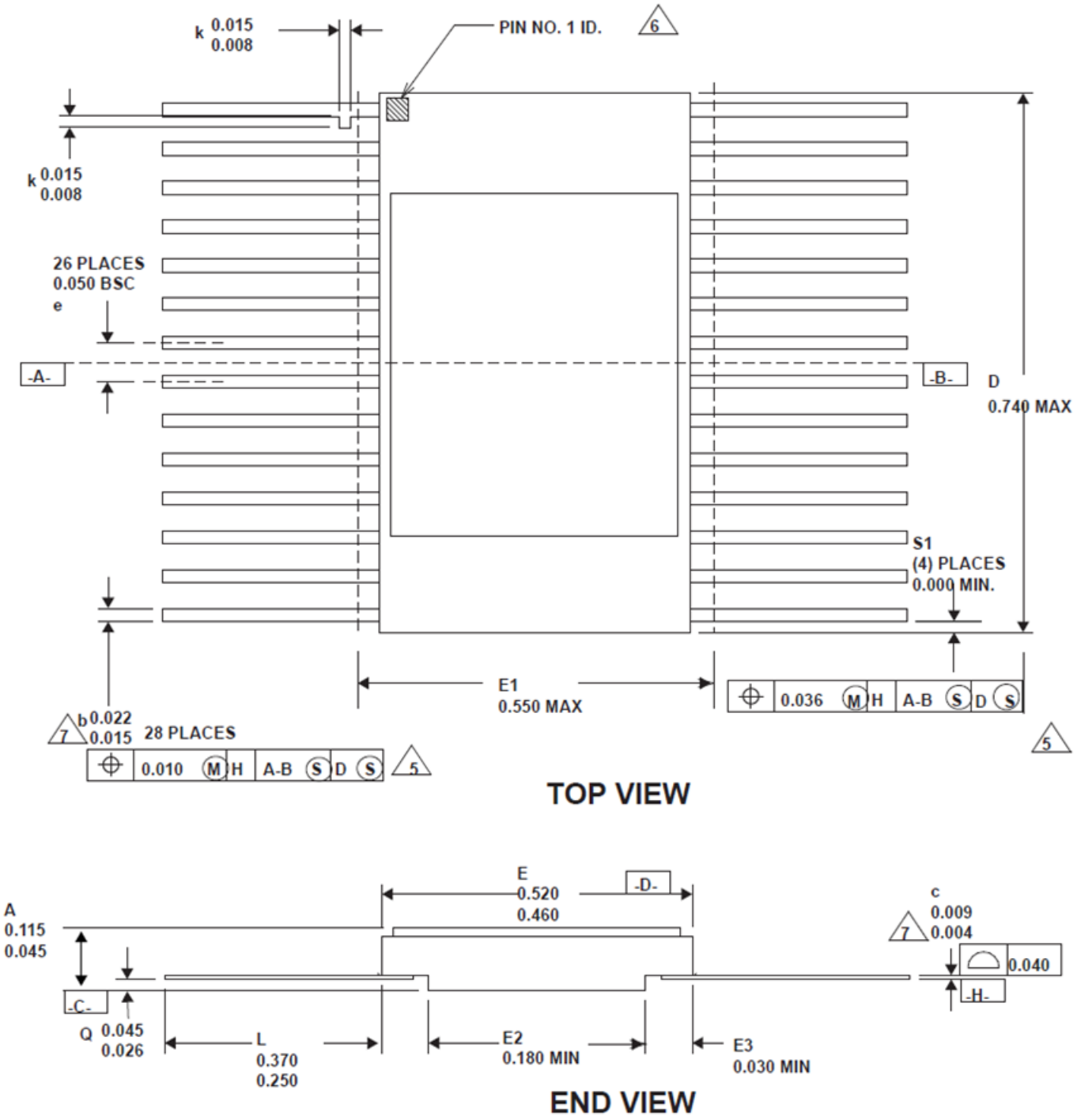

Figure 5. 28-Lead 50-mil Center Flatpack (0.490 x 0.74)

Notes:

1) All exposed metalized areas to be plated per MIL-PRF-38535.
2) The lid is connected to V_{SS}.
3) Lead finishes are in accordance with MIL-PRF-38535.
4) Dimension letters refer to MIL-STD-1835.
5) Lead position and coplanarity are not measured.
6) ID mark symbol is vendor option.
7) With solder, increase maximum by 0.003.
8) Total weight is approximately 2.4 grams.

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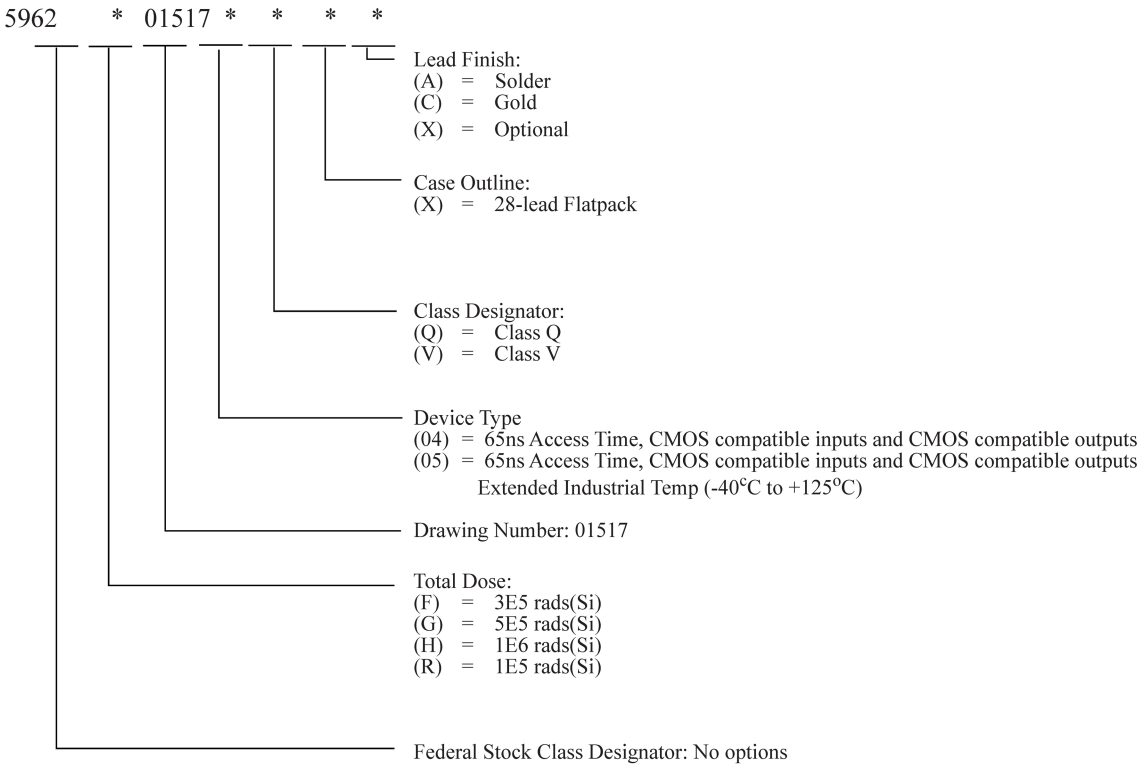
Ordering Information

UT28F256LVQLE PROM: SMD



Notes:

1) Lead finish (A, C, or X) must be specified.
2) If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3) Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening.
4) Device type 03 available with total dose of 1E5 rads(Si) or 3E5 rads(Si).
5) Due to the unique nature of field programmed devices, CAES does not guarantee program yield or accept returns for programming failures. CAES estimates programming yield at 80% or greater. Users should reference the "QLE Programming Guide" and the "QLE Programming Notes" documents available under the Applications Notes tab of the CAES HiRel Microelectronics Memory device webpage for programming instructions and information.

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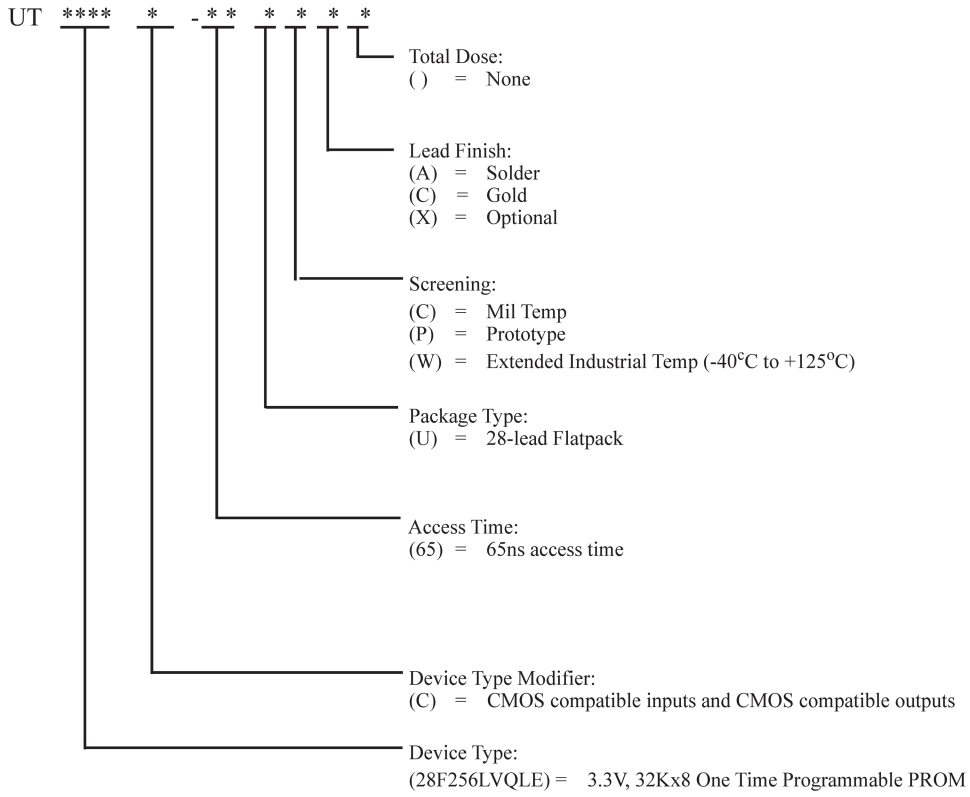

Notes:

1) Lead finish (A,C, or X) must be specified.
2) If an "X" is specified when ordering, then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3) Military Temperature Range flow per CAES Manufacturing Flows Document. Radiation characteristics are neither tested nor guaranteed and may not be specified.
4) Prototype flow per CAES Manufacturing Flows Document. Devices have prototype assembly and are tested at 25°C only. Radiation characteristics are neither tested nor guaranteed and may not be specified.
5) Extended Industrial Range flow per CAES Manufacturing Flows Document. Devices are tested at -40°C, room temp, and 125°C.Radiation neither tested nor guaranteed.
6) Lead finish is gold only.
7) Due to the unique nature of field programmed devices, CAES does not guarantee program yield or accept returns for programming failures. CAES estimates programming yield at 80% or greater. Users should reference the "QLE Programming Guide" and the "QLE Programming Notes" documents available under the Applications Notes tab of the CAES HiRel Microelectronics Memory device webpage for programming instructions and information.

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Revision Change:

Revision Date	Description of Change
March 2007	Initial datasheet used for tracking revision
February 2020	Added program yield comment to features of page one. Added programming yield note to both ordering pages.
April 2022	Added reference to note 5 to VIL VIH specifications and added note 5 to bottom of DC Electrical Characteristics table page 4.

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Datasheet Definitions

	DEFINITION
Advanced Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet **is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final**.
Preliminary Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

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