DATASHEET

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SpaceWire Physical Layer Transceiver

UT200SpWPHY01

Features

- 2-bit Serializer/Deserializer (SerDes) functionality
- LVDS physical layer
- Data rates to 200 Mbits/sec
- Data/Strobe transmit skew <500pS
- 3.3V power supply
- Cold spare on LVDS pins
- Radiation-hardened design; total dose irradiation testing to MIL-STD-883 Method 1019
  - Total-dose: 100 krad(Si)
  - Latchup immune (LET > 109 MeV-cm^2/mg)
- ESD rating Class 1
- Packaged in a 28-pin flatpack
- Standard Microcircuit Drawing 5962-06232
  - QML Q and V complaint part

Introduction

CAES Colorado Springs' UT200SpWPHY01 Physical Layer Transceiver (PHY) is designed to handle the critical timing issues associated with the SpaceWire Data/Strobe Encoding scheme.

The receiver operates on both edges of the recovered RxClk and provides data on the digital outputs in bit pairs. The transmitter operation is the reverse of the receiver. Bit pairs of data and strobe are written into the device on the WrClk signal and the PHY serializes data and strobe onto the LVDS bus using the TxClk signal. The advantages of this SerDes functionality is the interfacing FPGA or ASIC can run at reduced clock rate with high-speed clock not requiring a stringent phase relationship.

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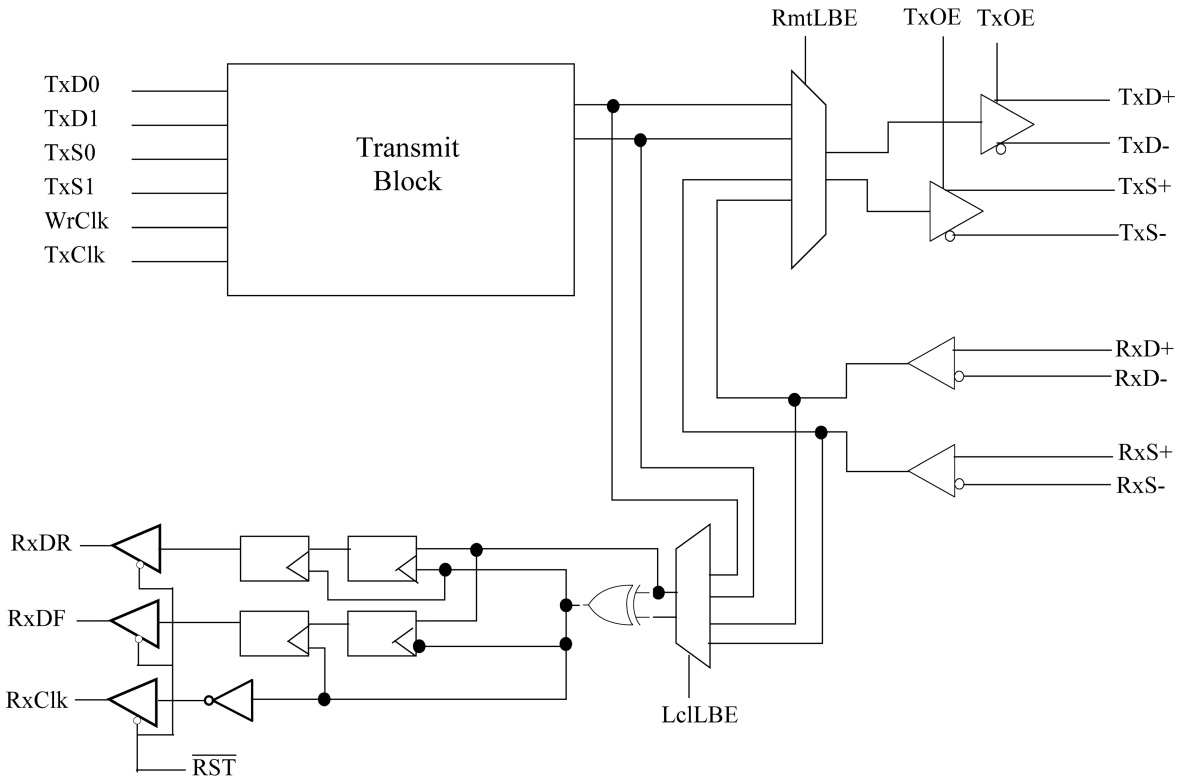

Figure 1. UT200SpWPHY01 SpaceWire PHY Chip Block Diagram

Applications Information

CAES Colorado Springs' UT200SpWPHY01 SpaceWire Physical Layer Transceiver is designed to maximize the speed of SpaceWire links implemented in Field Programmable Gate Arrays. The UT200SpWPHY01 is designed to handle the critical timing issues associated with the SpaceWire data/strobe encoding scheme.

Receiver Fail-Safe

The UT200SpWPHY01 SpaceWire Physical Layer Transceiver is a high gain, high speed device that amplifies a small differential signal (20mV) to TTL logic levels. Due to the high gain and tight threshold of the receiver, care should be taken to prevent noise from appearing as a valid signal.

The receiver's internal fail-safe circuitry is designed to source/ sink a small amount of current, providing fail-safe protection (a stable known state of HIGH output voltage) for floating, terminated or shorted receiver inputs.

1) **Open Input Pins**. If an application requires an unused channel, the inputs should be left OPEN. Do not tie unused receiver inputs to ground or any other voltages. The input is biased by internal high value pull up and pull down resistors to set the output to a HIGH state. This internal circuitry will guarantee a HIGH, stable output state for open inputs.

2) **Terminated Input**. If the driver is disconnected (cable unplugged), or if the driver is in a three-state or power-off condition, the receiver output will again be in a HIGH state, even with the end of cable 100Ω termination resistor across the input pins. The unplugged cable can become a floating antenna which can pick up noise. If the cable picks up more than 10mV of differential noise, the receiver may see the noise as a valid signal and switch. To insure that any noise is seen as common-mode and not differential, a balanced interconnect should be used. Twisted pair cable offers better balance than flat ribbon cable.

Shorted Inputs. If a fault condition occurs that shorts the receiver inputs together, thus resulting in a 0V differential input voltage, the receiver output remains in a HIGH state. Shorted input failsafe is not supported across the common-mode range of the device (V_{SS} to 2.4V). It is only supported with inputs shorted and no external common-mode voltage applied.

Table 1: SpaceWire Physical Layer Transceiver Device Operation Truth Table

TxOE	$\overline{RST}$	LclLBE	RmtLBE	Tx Outputs	Rx Outputs
0	0	X	X	Hi-Z	Hi-Z
1	1	0	0	CMOS Tx Inputs	LVDS Rx Inputs
0	1	0	X	Hi-Z	LVDS Rx Inputs
0	1	1	X	Hi-Z	CMOS Tx Inputs
1	0	X	0	0	Hi-Z
1	0	X	1	LVDS Rx Inputs	Hi-Z
1	1	0	1	LVDS Rx Inputs	LVDS Rx Inputs
1	1	1	0	CMOS Tx Inputs	CMOS Tx Inputs
1	1	1	1	LVDS Rx Inputs	CMOS Tx Inputs

Radiation

Parameter	Limit	Units
Total Ionizing Dose (TID)	>3E5 and 1E6	rads(Si)
Single Event Latchup (SEL) [1, 2]	>109	MeV-cm^2/mg
SEU Saturated Cross-Section (σ_{sat})	1.0E-8	cm^2/device
Onset Single Event Upset (SEU) LET Threshold [3]	109	MeV-cm^2/mg
Neutron Fluence	1.0E14	n/cm^2
Dose Rate Upset	TBD	rads(Si)/sec
Dose Rate Survivability	TBD	rads(Si)/sec

Notes:

1) The UT200SpW02 are latchup immune to particle LETs >109 MeV-cm^2/mg.
2) Worst case temperature and voltage of T_C = +125°C, V_{DD} = 3.6V, V_{DD}Q1/Q3/Q4 = 3.6V for SEL.
3) Worst case temperature and voltage of T_C = +25°C, V_{DD} = 3.0V, V_{DD}Q1/Q3/Q4 = 3.0V for SEU.
4) Adams 90% worst case particle environment, Geosynchronous orbit, 100mils of Aluminium shielding.

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UT200SpWPHY01

28-pin Flatpack Pin Description			
Pin Name	**Pin Number**	**Pin Type**	**Description**
LclLBE	1	LVCMOS Input [1]	**Local Loopback Enable** 0: No loopback, received data comes from LVDS Rx inputs (RxD+, ...) 1: Local loopback, received data comes from LVCMOS Tx inputs (TxD0, ...)
RmtLBE	2	LVCMOS Input [1]	**Remote Loopback Enable** 0: No loopback, Transmit LVDS data comes from the LVCMOS Tx inputs (TxD0, ...) 1. Remote Loopback, Transmit LVDS data comes from LVDS Rx inputs.
RxD+	3	LVDS Input	LVDS Rx differential positive Data input
RxD-	4	LVDS Input	LVDS Rx differential negative Data input
RxS+	5	LVDS Input	LVDS Rx differential positive Strobe input
RxS-	6	LVDS Input	LVDS Rx differential negative Strobe input
V_{DD}	7, 22, 28		VDD 3.3V power supply
GND	8,14,21,27		Vss 0V
TxS+	9	LVDS Output	LVDS Tx differential positive Strobe output
TxS-	10	LVDS Output	LVDS Tx differential negative Strobe output
TxD+	11	LVDS Output	LVDS Tx differential positive Data output
TxD-	12	LVDS Output	LVDS Tx differential negative Data output
TxOE	13	LVCMOS Input [1]	TxOE=High: Enables LVDS transmit TxOE=Low: Tri-states LVDS transmit
RxDR	26	LVCMOS Output	Receiver rising edge (even) bit output (See Figure 7)
RxDF	25	LVCMOS Output	Receiver falling edge (odd) bit output (See Figure 7)
RxClk	24	LVCMOS Output	Receiver clock output
$\overline{RST}$	23	LVCMOS Input [1]	$\overline{RST}$ must remain low for 3 clock cycles before transitioning high, and must transition high 3 clock cycles before valid data.
TxClk	20	LVCMOS Input [1]	Clock input to transmitter used to clock LVDS output. Any phase relationship is allowed between TxClk & WrClk but both must come from the same clock source and TxClk must be twice the frequency of the WrClk.
WrClk	19	LVCMOS Input [1]	Transmitter input data Clock used to clock CMOS input to transmitter. Any phase relationship is allowed between TxClk & WrClk but both must come from the same clock source and WrClk must 1/2 of TxClk.
TxS0	18	LVCMOS Input	First (even) bit of 2bit parallel strobe input to transmitter
TxS1	17	LVCMOS Input	Second (odd) bit of 2bit parallel strobe input to transmitter
TxD0	16	LVCMOS Input	First, even bit of 2bit parallel data input to transmitter
TxD1	15	LVCMOS Input	Second, odd bit of 2bit parallel data input to transmitter

Note:

1) LVTTL compatible

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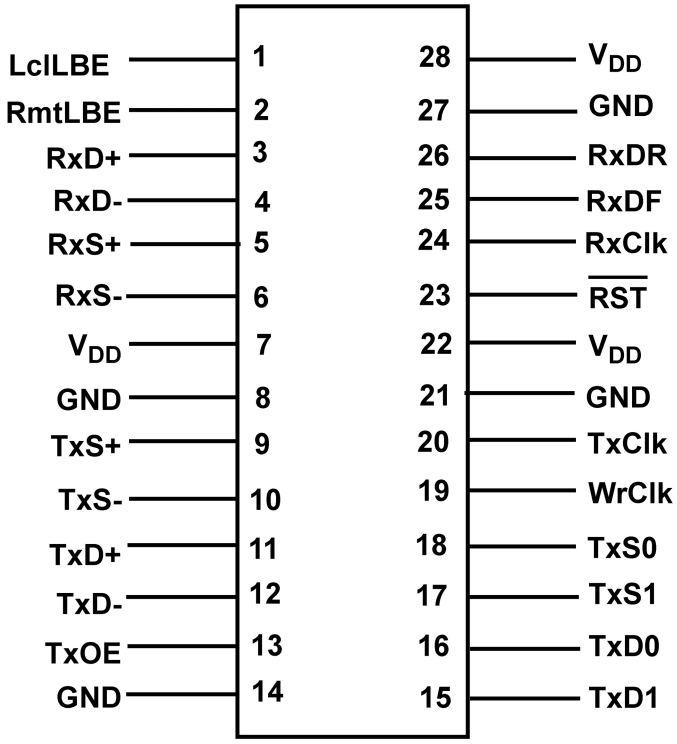
Pin Configuration



Absolute Maximum Ratings [1]

(Referenced to V_{SS})

Symbol	Parameter	Limits
V_{DD}	DC supply voltage	-0.3 to 4.0V
$V_{I/O}$	Voltage on any pin during operation	-0.3 to (V_{DD} + 0.3V)
	Voltage on any LVDS pin during cold spare [2]	-.3 to 4.0V
T_{STG}	Storage temperature	-65 to +150°C
P_D	Maximum power dissipation[3]	2.5W
Θ_{JC}	Thermal resistance, junction-to-case [4]	10°C/W
I_I	DC input current	±10mA

Notes:

1) Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2) LVCMOS pins are not cold spare.
3) Per MIL-STD_883, Method 1012.1 Section 3.4.1, $\frac{P_D = T_J(max) - T_C(max)}{\Theta_{JC}}$
4) Test per MIL-STD-883, Method 1012.

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Recommended Operating Conditions

Symbol	Description	Conditions	Limit	Units
V_{DD}	I/O supply voltage		3.0 to 3.6	V
V_{IN}	Input voltage on any pin		0 to V_{DD}	V
T_C	Case Temperature		-55 to 125	°C
t_{RISE}	Input rise time [1]	CMOS Inputs (VIL to VIH)	≤ 20	ns
		LVDS Inputs (VTL to VTH)	≤ 20	ns
t_{FALL}	Input fall time [1]	CMOS Inputs (VIH to VIL)	≤ 20	ns
		LVDS Inputs (VTH to VTL)	≤ 20	ns

Notes:

1) Supplied as a design guideline, not characterized nor tested.

DC Electrical Characteristics [1]

(V_{DD} = 3.3V ± 0.3V; -55°C < T_C < +125°C)

Symbol	Parameter	Condition	MIN	MAX	Unit
V_{IH}	High-level input voltage (CMOS)		2.0		V
V_{IL}	Low-level input voltage (CMOS)			0.8	V
V_{OL}	Low-level output voltage (LVCMOS)	IOL = 12mA		0.4	V
V_{OH}	High-level output voltage (LVCMOS)	IOH = -12mA	2.4		V
I_{INLVDS}	Input leakage current	V_{IN} = V_{DD} or GND, V_{DD} = 3.6V	-20	+20	uA
I_{INCMOS}	Input leakage current	V_{IN} = V_{DD} or GND, V_{DD} = 3.6V	-10	+10	uA
I_{CS}	Cold Spare Leakage Current	V_{IN}=3.6V, V_{DD} = V_{SS} = 0V	-20	+20	uA
V_{TH}	Differential Input High Threshold	VCM = +1.2V		+100	mV
V_{TL}	Differential Input Low Threshold	VCM = +1.2V	-100		mV
V_{OD}	Differential Output Voltage	R_L = 100Ω	250	400	mV
ΔV_{OD}	Change in Magnitude of V_{OD} for Complementary Output States	R_L = 100Ω		35	mV
V_{OS}	Offset Voltage	RL = 100Ω, $\left(V_{OS}=\frac{Voh + Vol}{2}\right)$	1.125	1.450	V
ΔV_{OS}	Change in Magnitude of V_{OS} for Complementary Output States	R_L = 100Ω		25	mV
I_{OZ}	LVDS Output Three-State Current	TxOE = Gnd V_{OUT} = 0V or V_{DD}, V_{DD} = 3.6V	-10	+10	mA

I_{CCL}	Loaded supply current, drivers enabled	R_{TEST} = 50Ω all channels, running in full duplex V_{IN} = V_{DD} or V_{SS} (all inputs) C_L = 37pF, F = 200MHz		120	mA
I_{CCZ}	Loaded supply current, drivers disabled	D_{IN} = V_{DD} or V_{SS} Clock and Data not toggling		10	mA
I_{CCI}	Supply current, data toggling, clocks running, device in standby	Clock @ 200 Mhz, TxOE = 0 Data @ 200 Mbits/sec, $\overline{RST}$ = 0		25	mA
C_{IN} [2]	LVCMOS input capacitance	f = 1MHz @ 0V		7	pF
C_{OUT} [2]	LVCMOS output capacitance	f = 1MHz @ 0V		15	pF
C_{INLVDS} [2]	LVDS input capacitance	f = 1MHz @ 0V		6	pF
$C_{OUTLVDS}$ [2]	LVDS output capacitance	f = 1MHz @ 0V		7	pF

Notes:

1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except differential voltages.
2) Capacitance is measured for initial qualification and when design changes may affect the input/output capacitance. Capacitance is measured between the designated terminal and V_{SS} at a frequency of 1MHz and a signal amplitude of 50mV maximum.
3) R_{TEST} is the tester load. R_L is the LVDS termination load.

AC Switching Characteristics

(V_{DD} = +3.3V ± 0.3V, T_A = -55°C to +125°C)

Symbol	Parameter	MIN	MAX	Unit
t_{CDLH}	TxClk to differential Data output low to high prop delay R_{TEST} =50, C_L = 37pF (figure 2)	2	4	ns
t_{CDHL}	TxClk to differential Data output high to low prop delay R_{TEST} =50, C_L = 37pF (figure 2)	2	4	ns
t_{CSLH}	TxClk to differential Strobe output low to high prop delay R_{TEST} =50, C_L = 37pF (figure 2)	2	4	ns
t_{CSHL}	TxClk to differential Strobe output high to low prop delay R_{TEST} =50, C_L = 37pF (figure 2)	2	4	ns
t_{DCS}	Differential Channel Skew		0.4	ns
t_{CCS} [1]	Channel to Channel Skew		0.5	ns
t_{TLH} [2]	Rise time LVDS Driver (figure 2) R_L=100, C_L = 37pF		1.5	ns
t_{THL} [2]	Fall time LVDS Driver (figure 2) R_L=100, C_L = 37pF		1.5	ns
t_{OEHZ}	Output Enable Low to Data or Strobe High to Z (figure 3, 4) R_{TEST} = 50, C_L = 37pF		5	ns
t_{OELZ}	Output Enable Low to Data or Strobe Low to Z (figure 3, 4) R_{TEST} = 50, C_L = 37pF		5.0	ns
t_{OEZH}	Output Enable High to Data or Strobe Z to High (figure 3, 4) R_{TEST} = 50, C_L = 37pF		5	ns
t_{OEZL}	Output Enable High to Data or Strobe Z to Low (figure 3, 4) R_{TEST} = 50, C_L = 37pF		5.0	ns
$t_{SETUP\ TX}$	Minimum required setup of Data or Strobe with respect to WrClk (figure 6)	2		ns
$t_{HOLD\ TX}$	Minimum required hold of Data or Strobe with respect to WrClk (figure 6)	0		ns
t_{INRISE} [3]	Maximum rise time into Data/Strobe inputs (0.8V to 2V)		14	% of bit width
t_{INFALL} [3]	Maximum fall time into Data/Strobe inputs (0.8V to 2V)		14	% of bit width
t_{DRST}	Minimum number of full clock cycles (WrClk) between rising edge of $\overline{RST}$ and rising edge of first valid data or strobe (TxDO, TxD1, TxS0, TxS1) (figure 5)	3		WrClk cycles
t_{CRST}	Minimum number of full clock cycles (WrClk) that $\overline{RST}$ must remain low before $\overline{RST}$ can transition high (figure 5)	3		WrClk cycles
t_{CO}	Delay between RxClk falling and data edge (figure 7)		1	ns
t_{RLZ}	Delay between $\overline{RST}$ going low and CMOS output tri-state (figure 7) R_{TEST} = 50, C_L = 37pF		5	ns
t_{RHV}	Delay between $\overline{RST}$ going high and CMOS output valid (figure 7) R_{TEST} = 50, C_L = 37pF		5	ns
t_{RISE}	CMOS 20-80% Receiver output rise time (figure 8) C_L = 37pF		1	ns
t_{FALL}	CMOS 20-80% Receiver output fall time (figure 8) C_L = 37pF		1	ns
t_S [3]	LVDS Rx input data to strobe separation (figure 9)	2.5		ns
$TxClk_{PMIN}$	Minimum Transmit Clock period		5	ns
$WrClk_{PMIN}$	Minimum Write Clock period		10	ns
t_{CPMIN}	Minimum High or Low Clock Pulse Width	2		ns

Notes:

1) Includes differential skew
2) Guaranteed by characterization
3) Specified as a design guidelines only, not tested.
4) 2.5 ns of separation requires a R_{XOUT} Load of <= 10pF

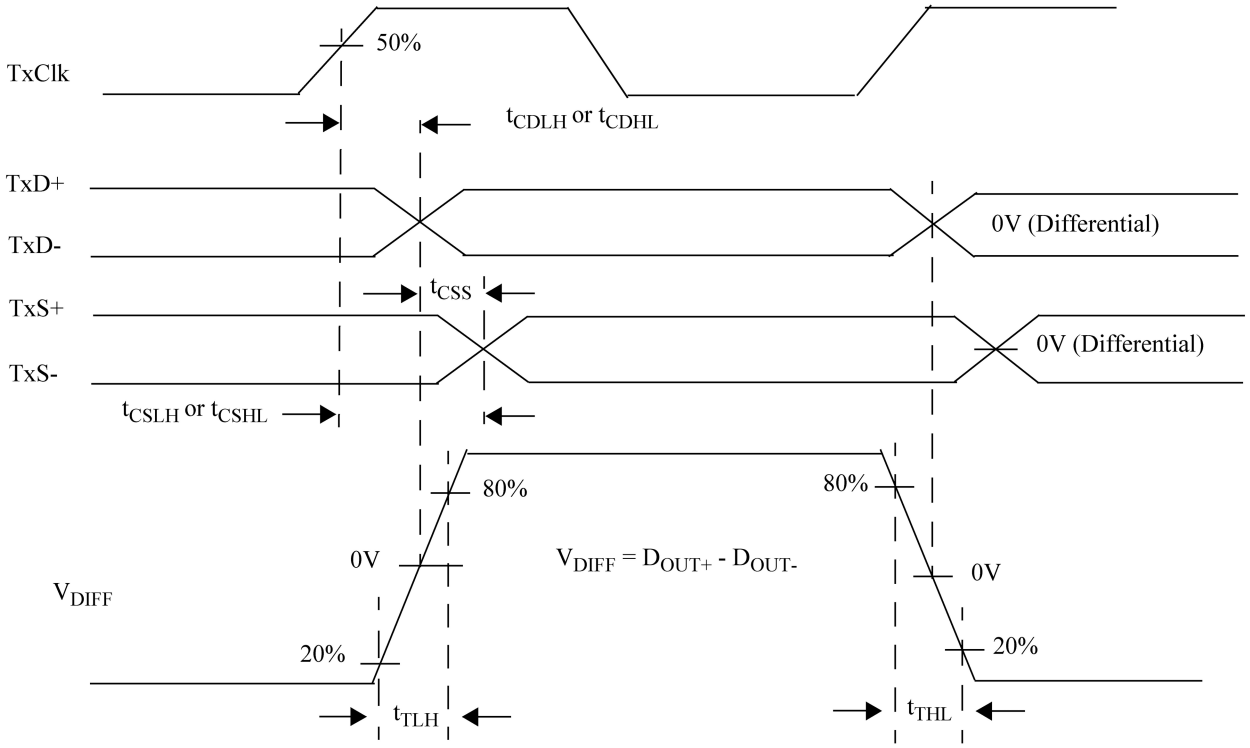


Figure 2. Driver Rise and Fall Times and Channel Skew

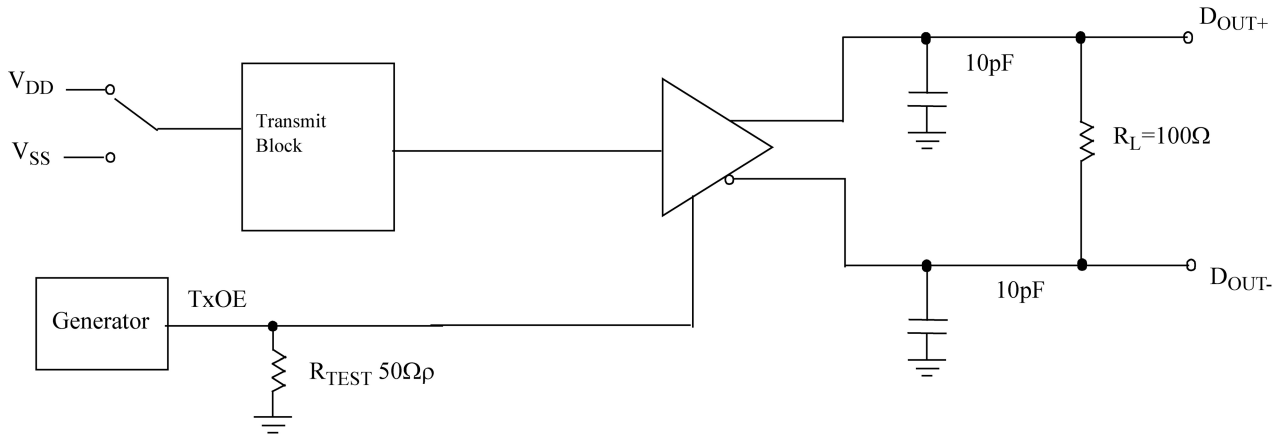


Figure 3. Driver Three-State Delay Time Test or Equivalent Circuit

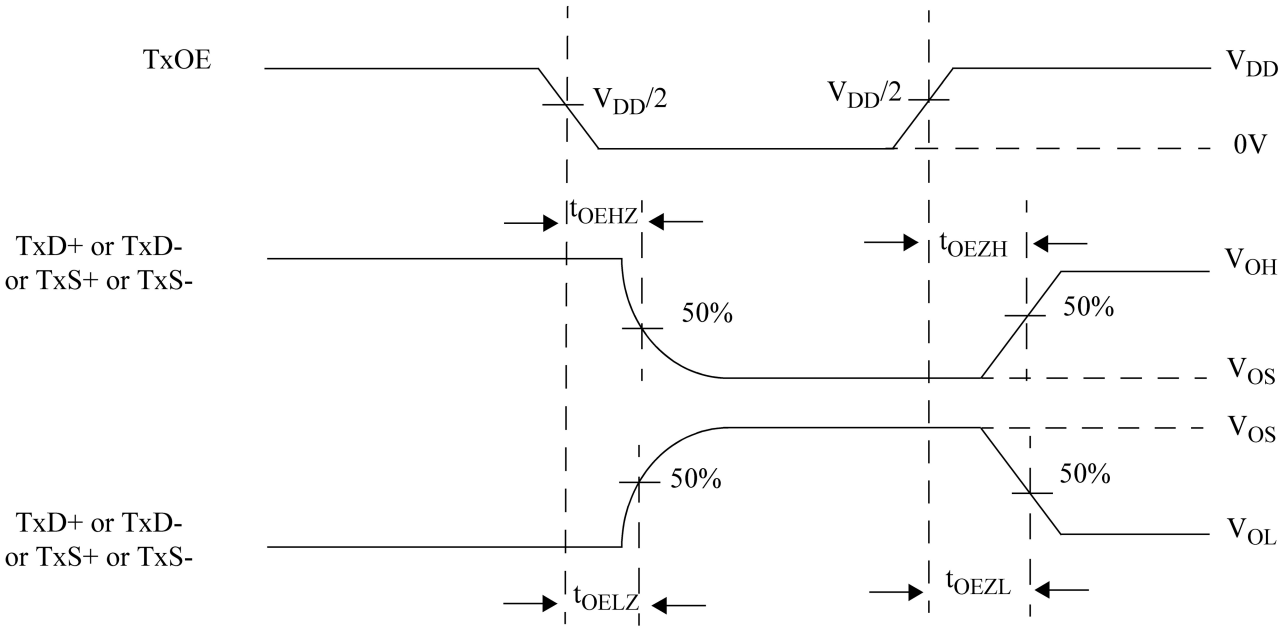


Figure 4. Output Enable to Data Out Timing

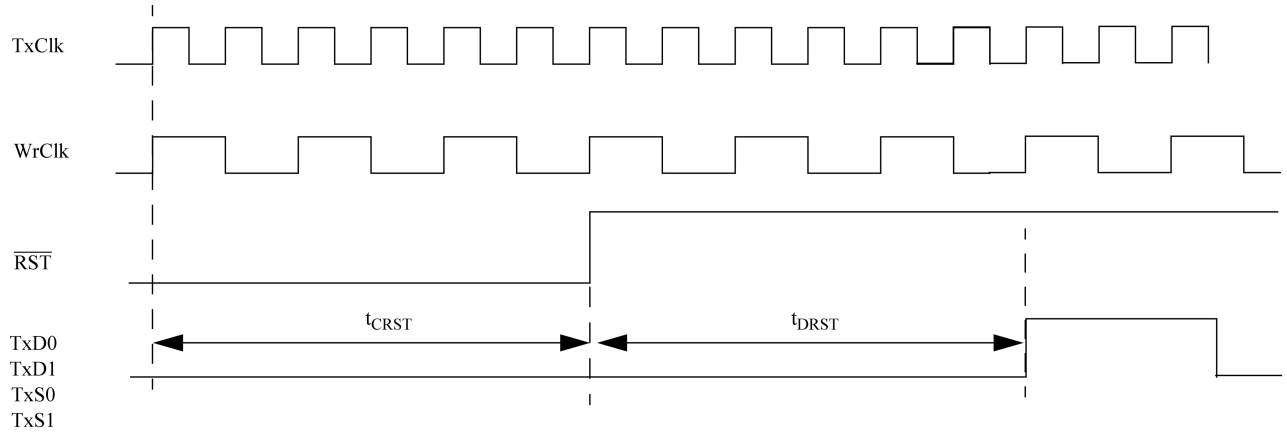


Figure 5. Reset Timing Diagram

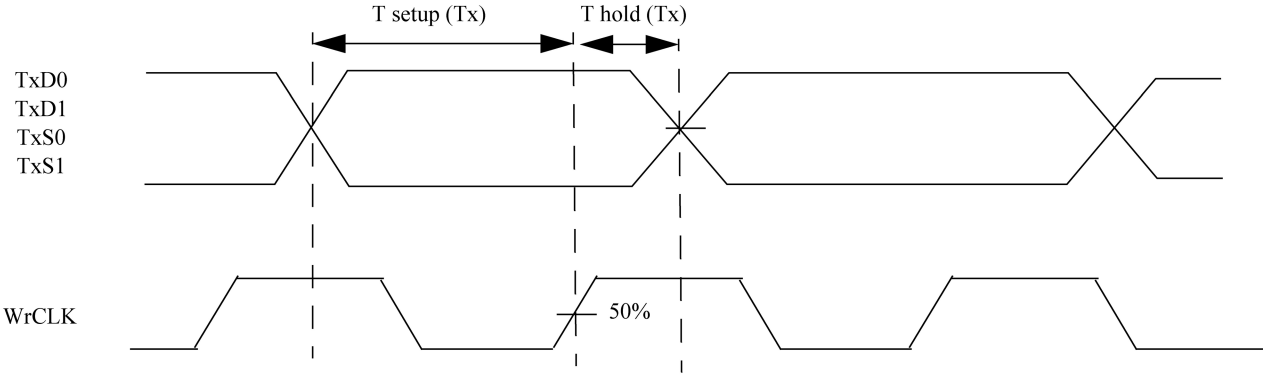


Figure 6. Transmitter Input Timing Diagram

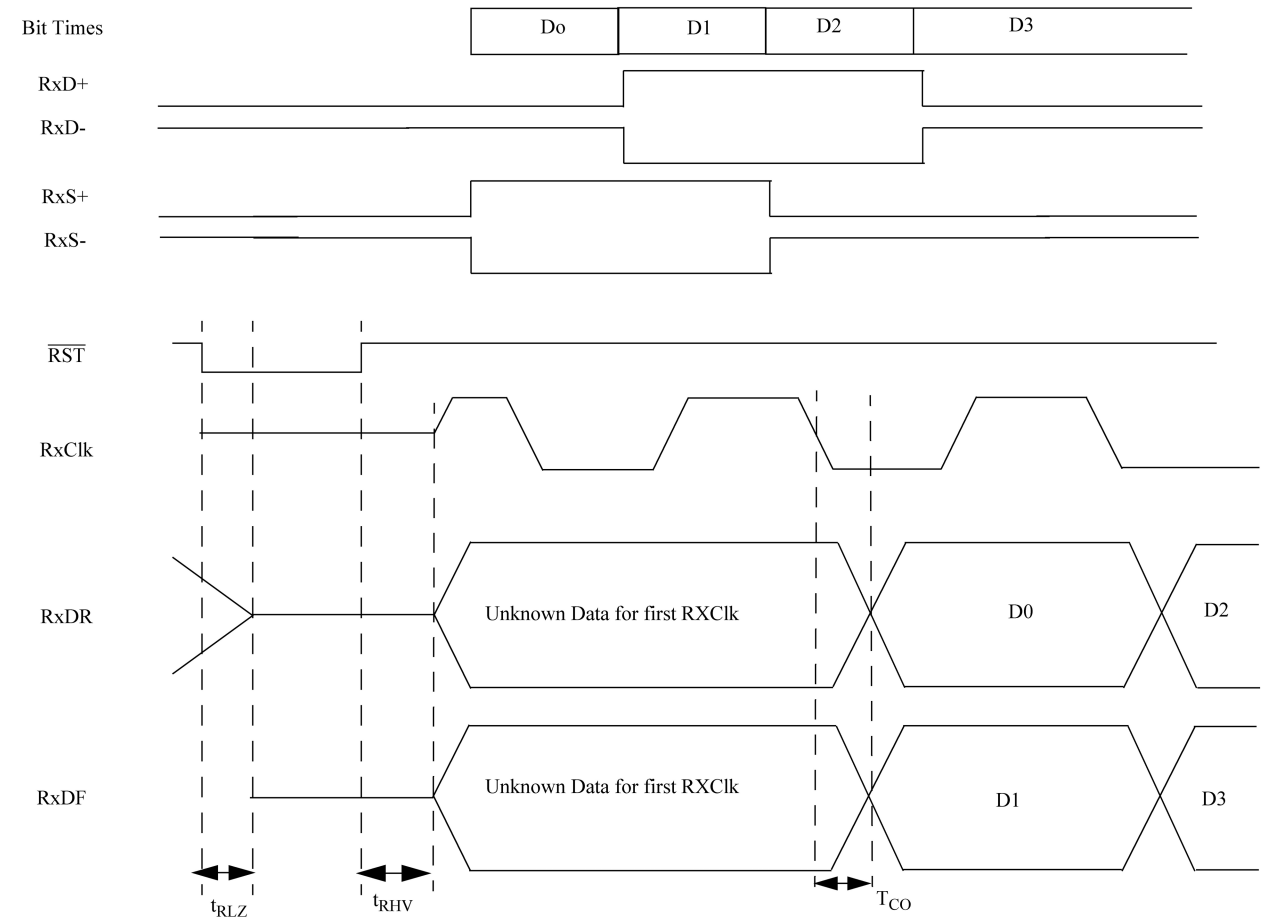


Figure 7. Receiver Output Timing Diagram

Figure 8. Receiver Output Rise and Fall Times Waveform

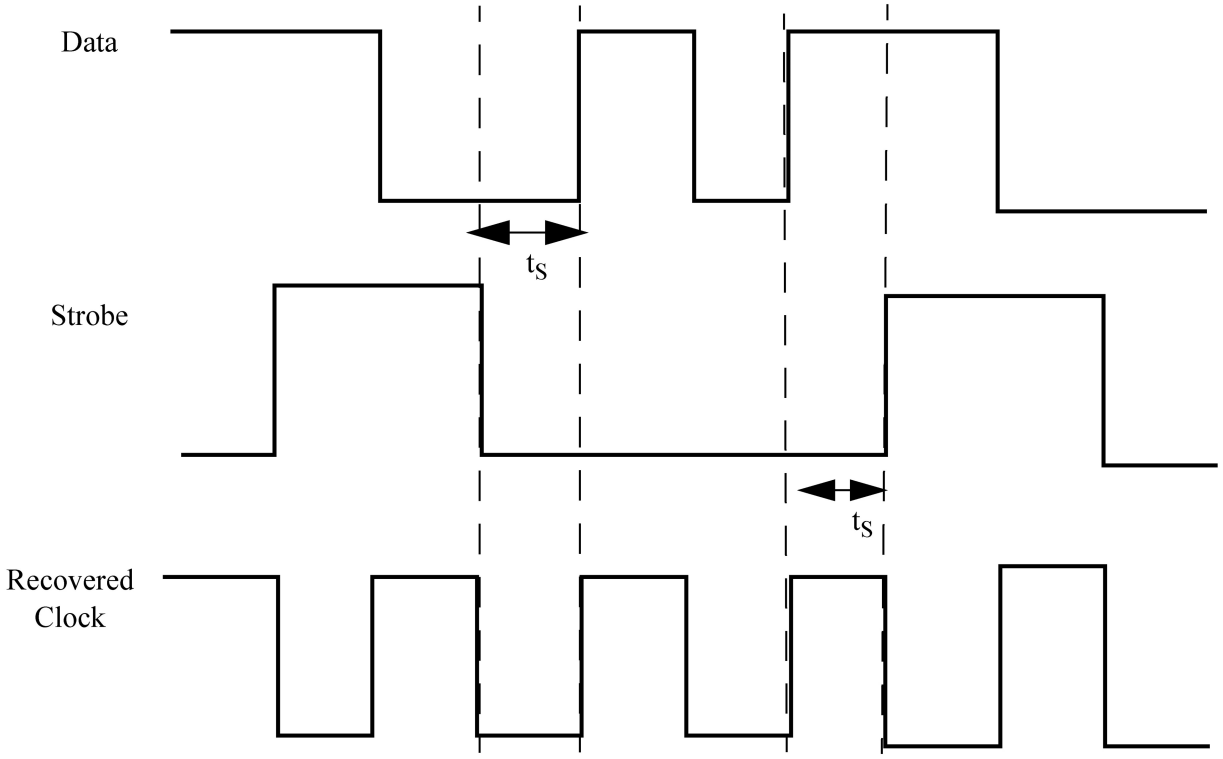


Figure 9. Data/Strobe Separation

Packaging

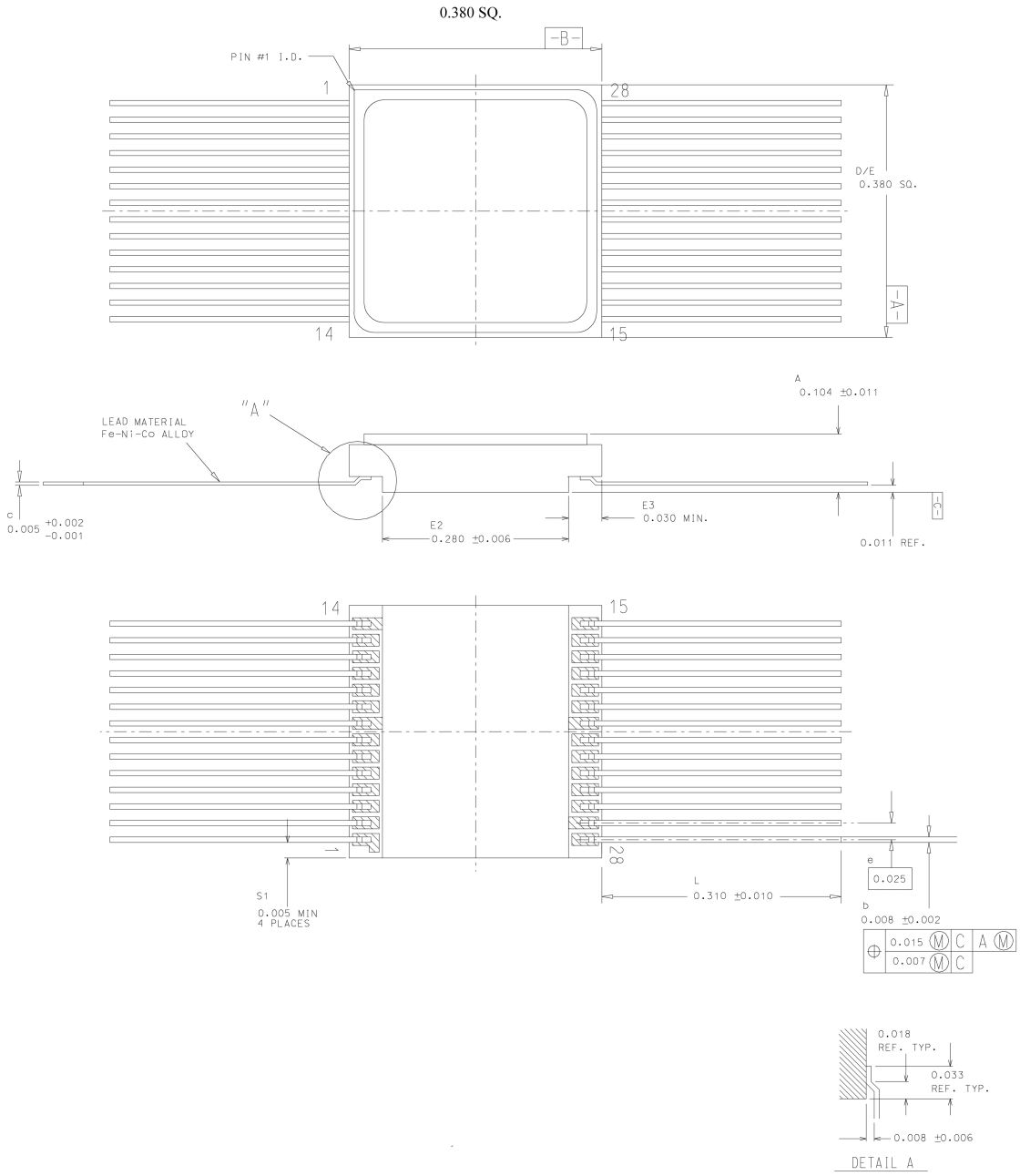


Figure 10. 28-pin Flatpack

Notes:

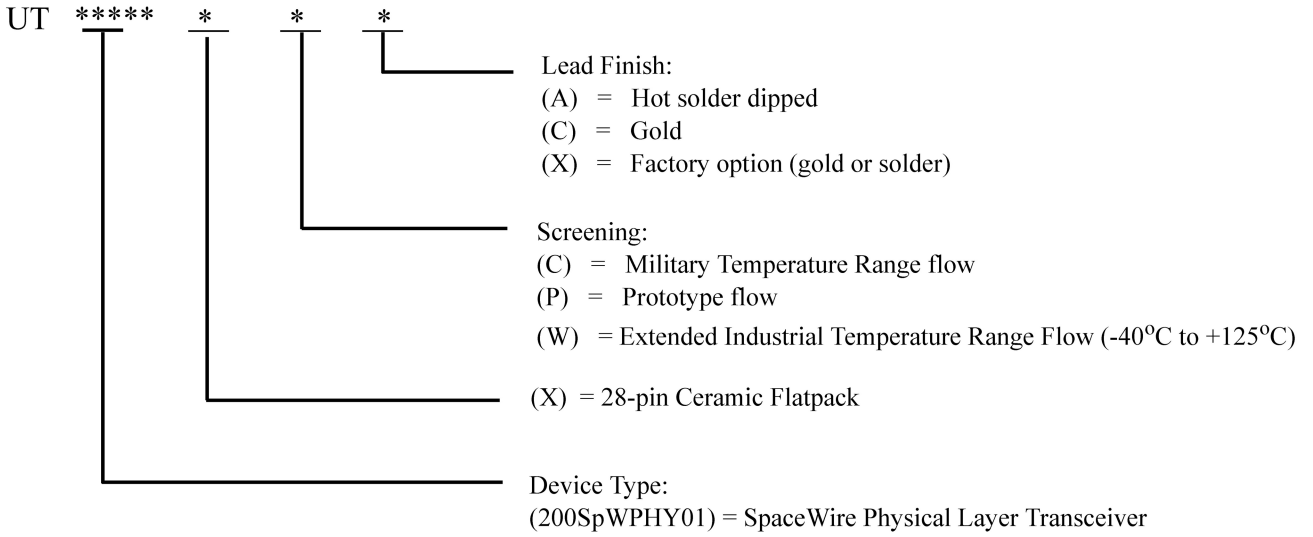
1) All exposed metallized areas are gold plated over electrically plated nickel per MIL-PRF-38535.
2) The lid is electrically connected to V_{SS}.
3) Lead finishes are in accordance with MIL-PRF-38535.
4) Dimension symbology is in accordance with MIL-PRF-38535.
5) Lead position and coplanarity are not measured.
6) ID mark symbol is vendor option: no alphanumerics.

SpaceWire Physical Layer Transceiver

UT200SpWPHY01

Ordering Information

UT200SpWPHY01: SpaceWire Physical Layer Transceiver



Notes:

1) Lead finish (A,C, or X) must be specified.
2) If an "X" is specified when ordering, then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3) Prototype flow per CAES Manufacturing Flows Document. Tested at 25°C only. Lead finish is GOLD ONLY. Radiation neither tested nor guaranteed.
4) Military Temperature Range flow per CAES Manufacturing Flows Document. Devices are tested at -55°C, room temp, and 125°C. Radiation neither tested nor guaranteed.
5) Extended Industrial Range flow per CAES Colorado Springs Manufacturing Flows Document. Devices are tested at -40°C, room temp, and 125°C. Radiation neither tested nor guaranteed.

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SpaceWire Physical Layer Transceiver

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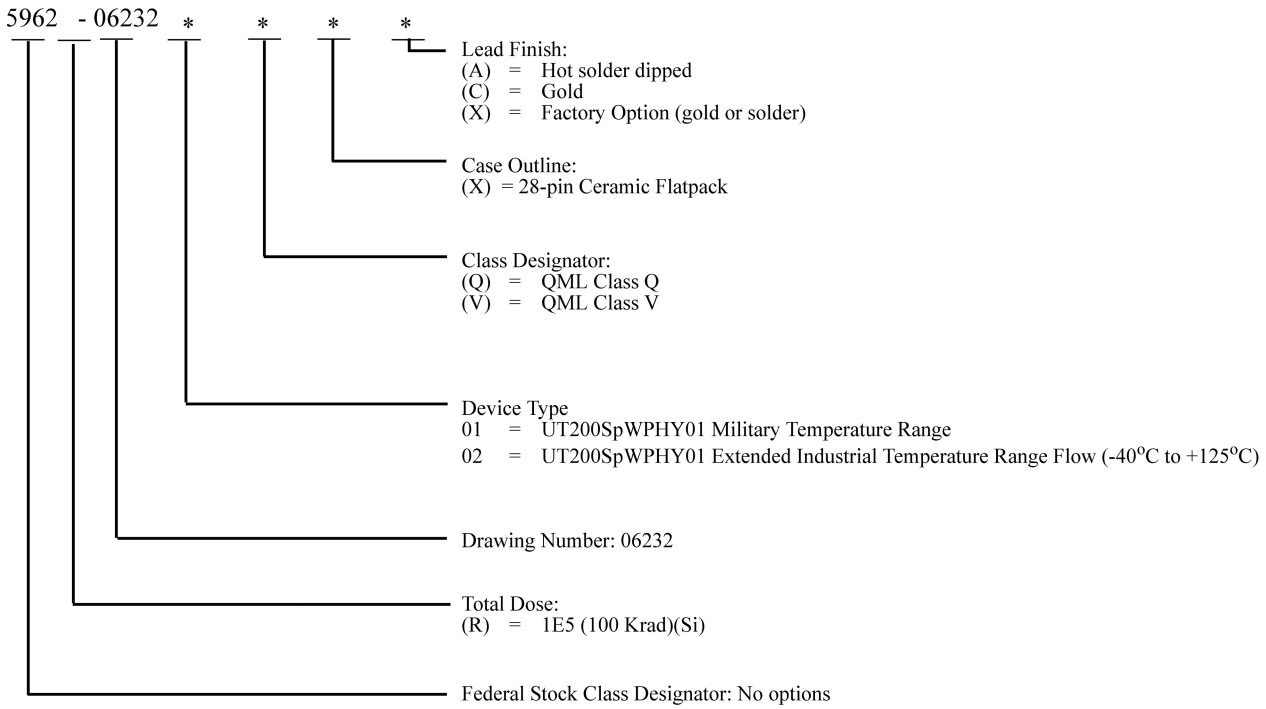
UT200SpWPHY01: SMD



Notes:

1) Lead finish (A,C, or X) must be specified.
2) If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3) Total dose radiation must be specified when ordering. QML Q and QML V not available without radiation hardening.

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Datasheet Revision History

Revision Date	Description of Change	Pages	By
Jan 2021	Initial revision history captured from current datasheet Feb 2008 Changed PD to 2.5W from 432mW. Corrected the PD specification by adding note 3 and moving note 3 to note 4. Added TC. Trise and Tfall to recommended operating conditions.	5,6	MJL
Feb 2022	Changed units for Iinlvds, Iincmos, Ics from mA to uA which got inadvertently changed during the CAES formatting.	6	MJL

Datasheet Definitions

	DEFINITION
Advanced Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet **is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final**.
Preliminary Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

The following United States (U.S.) Department of Commerce statement shall be applicable if these commodities, technology, or software are exported from the U.S.: These commodities, technology, or software were exported from the United States in accordance with the Export Administration Regulations. Diversion contrary to U.S. law is prohibited.