DATASHEET

RELEASED 4/08/13

4-Port SpaceWire Router

UT200SpW4RTR

Features

- 4-Port SpaceWire Router with a system interface port for a total of 5 ports
- Data rates up to 200Mbps full duplex on all 4 SpaceWire ports
- Compliant to the SpaceWire Standard, Document Number ECSS-E-ST-50-12C (http://www.ecss.nl/)
- Group adaptive routing for 2 ports when using logical addressing
- Replicated lookup tables for each receive port no arbitration is necessary when accessing lookup table data
- Host (FIFO) clock max frequency: 50MHz for 200Mbps -9 by 128 receive and transmit FIFOs on each port
- Non-blocking cross-point switch connecting any receive port to any transmit port
- Path and logical addressing support
- Internal status/error registers accessible via the configuration protocol
- Routing is table accessible via the configuration protocol which holds the logical address to transmit port mapping
- Any SpaceWire port can READ or WRITE to the configuration port, along with the host processor, by utilizing the configuration protocol
- Internal control logic to support the operation of arbitration and group adaptive routing. (Group Adaptive routing for 2 ports)
- In external time-code interface comprising TICK_IN, TICK_OUT and current tick count value
- System Interface Features
  - Low-power FIFO memories
  - Clocked PUSH and POP interfaces
  - Hard set Full/Almost Full/Empty/Almost Empty flags
  - SpaceWire In/out ports are controlled by separate clock and enable signals. Transmit FIFO input port is controlled by a free-running clock (HOST_CLK).
- Cold spare on LVDS pins
- 3.3V I/O Supply (V_{DD})
- 2.5V Core Supply (V_{DDC})
- ESD rating Class 2 2000 V for LVDS pins
- Temperature range: -40°C to +105°C
- Operational environment:
  - Total-dose: 100 krad(Si)
  - Latchup immune (LET >100 MeV-cm^2/mg)
- Packaging options:
  - 255-lead CLGA
  - 255-lead CBGA
  - 255-lead CCGA
- Standard Microcircuit Drawing 5962-08244
  - QML Q and QML V

Introduction

The CAES UT200SpW4RTR is a 4-Port Router capable of operating at data rates from 10 to 200 Mbps. A parallel host interface is also provided for a total of 5 ports on the router. The router implements a non-blocking cross point switch and a "Round Robin" arbitration scheme allowing all 5 receive ports access to all 5 transmit ports.

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4-Port SpaceWire Router

UT200SpW4RTR

Path and logical addressing are supported (Per ECSS-E-ST-50- 12C) and lookup table storage is replicated 5 times giving each receive port a dedicated block of memory for logical addressing. Configuration of lookup tables, as well as access to internal registers may occur through any of the 5 ports using a simple configuration protocol. A group adaptive function is also provided for 2 ports when implementing logical addressing.

Each of the four SpaceWire ports is capable of running at an independent speed. This allows for systems to be configured with nodes/instruments running at different speeds. If one node/instrument does not need to be sampled as often as another a more efficient power management scheme can be achieved.

The physical interfaces can be either a LVDS or LVCMOS interface. This allows the user to select the interface that best meets system and reliability requirements. The LVDS interface can directly connect and drive up to 10 meters of cable. The LVCMOS interface must interface to LVDS drivers and receivers.

Independent look up table memory space is provided for each port. Having separate look up tables reduces bottle necks by allowing each port access to a non shared lookup table.

4-Port SpaceWire Router

UT200SpW4RTR

CAES UT200SpW4RTR 4 Port SpaceWire Router

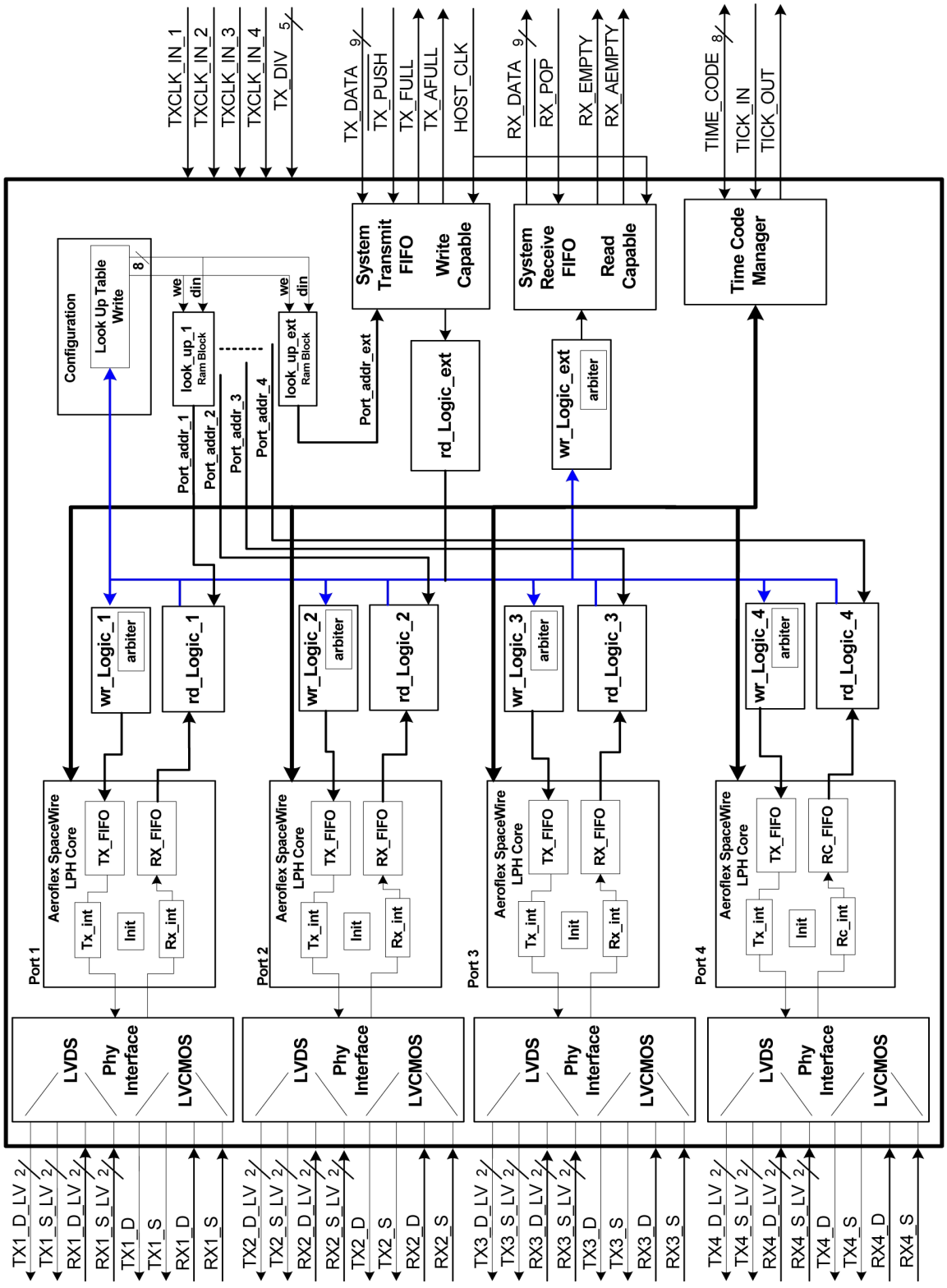


Figure 1. UT200SpW4RTR SpaceWire 4-Port Router Block Diagram

Applications Information

CAES Colorado Springs' UT200SpW4RTR 4-Port Router offers a highly adaptable solution for a distributed network. The number of ports allows for a very reliable system where multiple nodes can be connected together to gain performance. Using the non-blocking cross-point switch the shortest path between nodes can be configured. Each node can transmit and receive packets and each connection between nodes can carry multiple packets. The 4-Port Router is full duplex on each of the ports. The router also allows for a small Centralized network configuration.

1.0 Interfaces

1.1 SpaceWire

The UT200SpW4RTR 4-Port Router provides fourECSS-E-ST-50-12C compliant node interfaces. Each node contains a transmit and receive FIFO used to buffer data being sent within the network. The transmit FIFO takes data from a host system and transmits it to a node. Whereas the receive FIFO accepts data from a node and passes it to the host system. A host system is what the node is connected to and can be a microprocessor, computer, sensor or memory unit and is responsible for data management.

1.1.1 Port Initialization

All four ports follow the initialization procedure as defined in ECSS-E-ST-50-12C. Following are the key components of the initialization process. After a reset or disconnect the link will initiate operation at a signaling rate of 10 Mbps, ±1 Mbps. This provides the system with a common data rate while the system is checked for proper operation. Once the operation of the system is validated each of the four ports will switch to the specified transmit data rate. Each of the four ports must be capable of running at 10 ± 1 Mbps.

1.2 System Interface

The UT200SpW4RTR 4-Port Router provides a system interface to the user in the form of Receive and Transmit FIFO's. Each FIFO is 9 bits wide by 128 deep. Data format for the FIFO is 8-bits of data [7:0] and one bit [8] to indicate when an EOP or an EEP has been received. A EOP is an End-of-Packet marker and is used to indicate that a packet of data has been successfully sent. An EEP is an Error-End-of-Packet and signals that there was an error with in the packet. Table 1 shows the EOP/EEP handling.

Table 1. EOP and EEP Handling

9-bit Data	Character Type
100000000	EOP
100000001	EEP

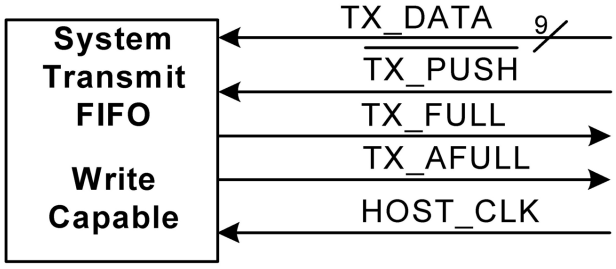


Figure 2. System Transmit Interface

1.2.1 System Port Transmit FIFO

The Transmit FIFO is write capable by the user and is 9 bits wide by 128 deep. Full (TX_FULL) and Almost Full (TX_AFULL) flags are provided to help the user prevent overwriting the FIFO. Data will be written into the FIFO on the rising edge of the clock when $\overline{\text{TX\_PUSH}}$ is "Low". The levels of the Almost Full flags cannot be changed by the user.

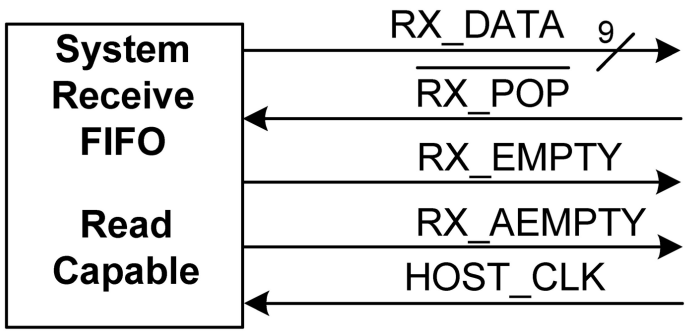


Figure 3. System Receive Interface

1.2.2 System Port Receive FIFO

A second 9 bit wide by 128 deep FIFO is provided for the user interface to receive data. Data received from one of the SpaceWire ports is read from the receive FIFO on the rising edge of the HOST clock when $\overline{\text{RX\_POP}}$ is "Low". This FIFO is first Byte Fall Through.

1.3 SpaceWire Physical Interface

The UT200SpW4RTR provides two different physical interfaces to the user. The first is on chip LVDS that can drive cable lengths up to 10 meters. The second is single ended LVCMOS in the event the user wishes to use discrete LVDS drivers and receivers. Examples of these two configurations are shown in Figures 4 and 5. In Figure 5 the external LVDS devices are CAES quad drivers and receivers.

4-Port SpaceWire Router

UT200SpW4RTR

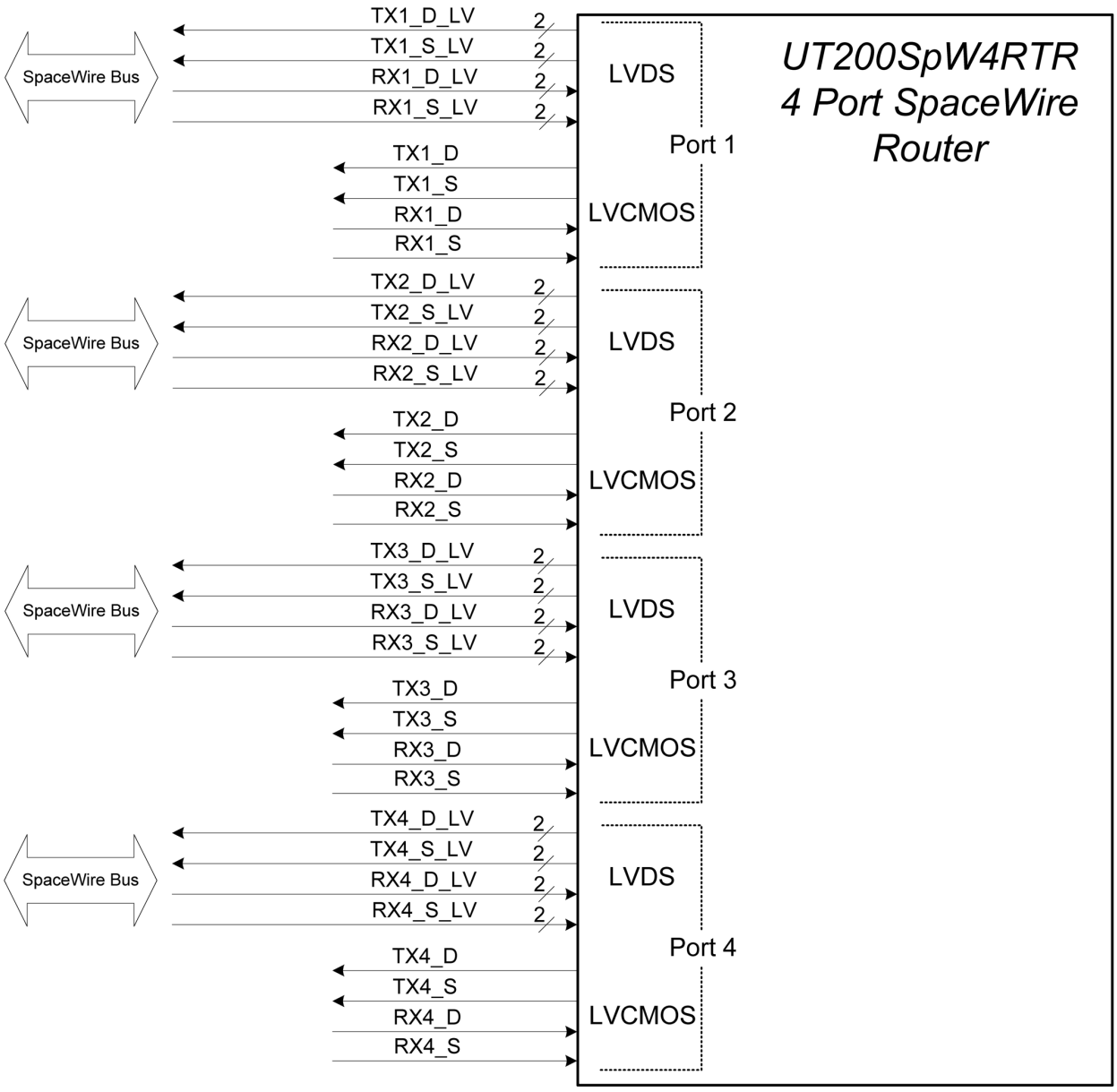


Figure 4. 4-Port Router on Chip LVDS Interface

UT200SpW4RTR

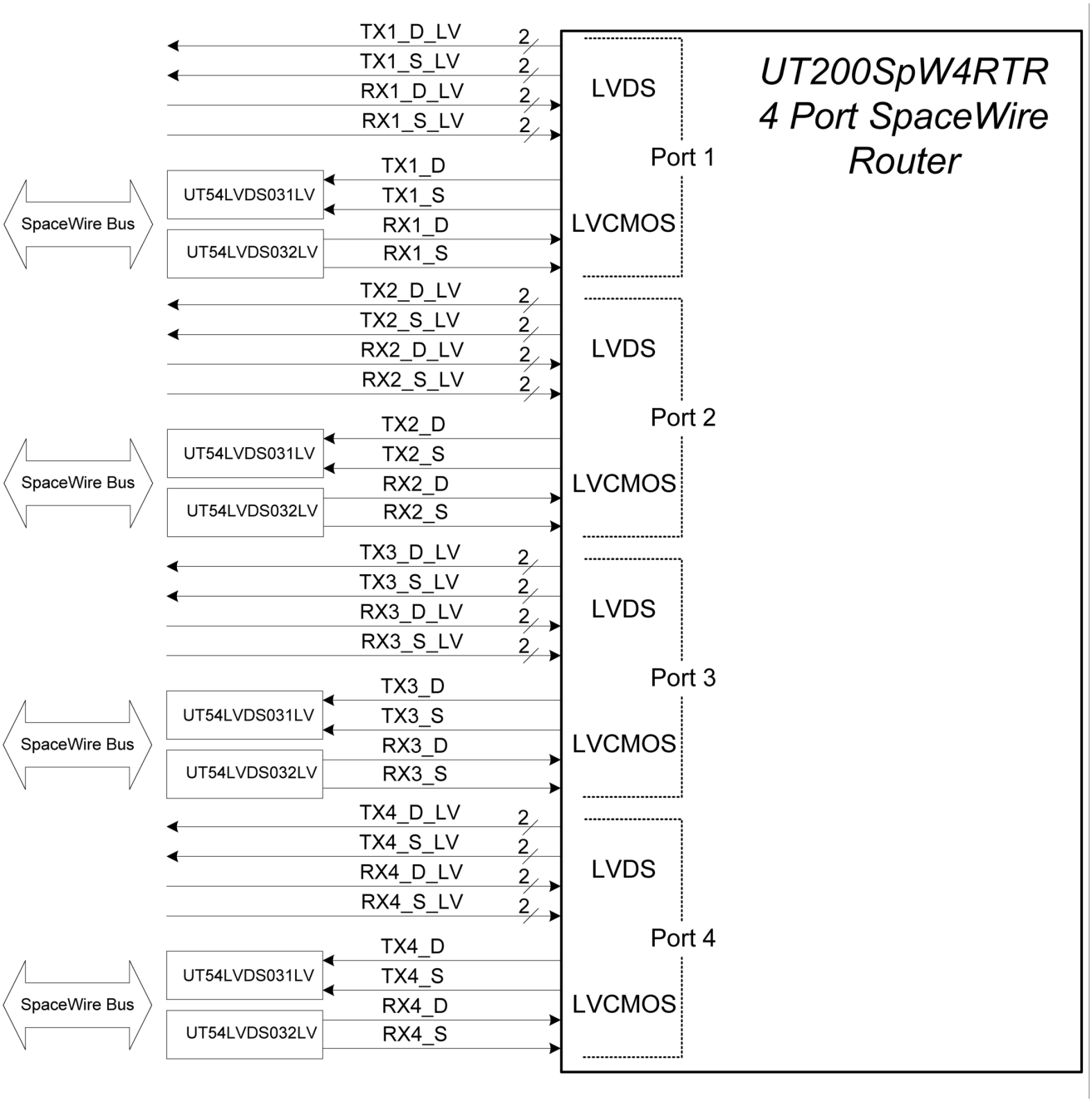


Figure 5. 4-Port Router External LVDS Interface

1.4 Power Requirements

The four-port router shall operate with a 2.5V core voltage supply and an I/O supply set at 3.3V.

Table 2. Power and Ground Pins

Pin Name	Pin Number	Description
V_{DD}	T11, T5, N8, P11, N9, P14, N13, M7, K15, M10, J4, K3, J13, G3, H4, E7, H13, E10, G13, C11, G15, C14, D8, A5, D9, D13, A11	I/O and LVDS supply voltage
V_{DDC}	T8, R1, P8, N4, M15, L6, L11, K5, K12, H1, G5, G12, F6, F11, E15, D4, C8, B1, A8	Core supply voltage
V_{SS}	T1, N14, T14, L5, R8, L13, R11, L15, P3, J15, M1, H15, M5, F5, M8, F13, M9, F15, M12, D14, L7, L8, L9, L10, K6, K7, K8, K9, K10, K11,J1, J5, J6, J7, J8, J9, J10, J11, J12, H5, H6, H7, H8, H9, H10, H11, H12, G6, G7, G8, G9, G10, G11, F7, F8, F9, F10, E1, E5, E8, E9, E12, C3, B8, B11, A2, A14, R7,P5, P6, P7, P9, P10, N5, N6, N7, N10, N11, N12, M4, M6, M11, L4, K4, H2, G4, F4	I/O and Core supply ground
N/C	P12, R14, P13, M13, L12, K13, F12, E11, E13, C10, C9, C7, L3, M3, N2, E4, E6, D5, D6, D7, D10, D11, D12, C12, C13, B14	No Connect, Pins must be left floating

1.4.1 Power Sequencing

To avoid large surge currents, V_{DD} should be powered up either before V_{DDC} or synchronously with V_{DDC} (V_{DD} >V_{DDC}). DO NOT power up the core voltage supply V_{DDC} before the I/O supply V_{DD}; doing so will cause a large in-rush current from V_{DDC} to V_{DD} that will stress the power supplies and router components. For proper operation, connect all V_{DD} pins to 3.3V, V_{DDC} pins to 2.5V, and ground all V_{SS} pins (i.e., no floating V_{DD}, V_{DDC}, or V_{SS} input power pins). If V_{DD} and V_{DDC} are being powered up synchronously ensure that the voltage difference between V_{DDC} and V_{DD} does not exceed0.4V (V_{DDC} - V_{DD}< 0.4V). See AC Electrical Characteristics.

1.4.2 LVCMOS I/O

Tie unused LVCMOS inputs to V_{SS} through a 1k Ω to 10k Ω resistor. It is good design practice to tie unused inputs to V_{SS} via a resistor to reduce noise susceptibility. The resistor protects the input pin by limiting the current from high going variations in V_{SS} which could damage the input to the device. Unused LVCMOS outputs can be left open.

1.4.3 LVDS I/O

All unused LVDS receiver inputs and driver outputs can be left open if not in use. No termination resistors are required across the differential LVDS driver output pins. If the differential outputs on the driver are shorted together, there will be 0V between the 2 outputs. Assuming that the outputs are only shorted to each other, no damage will occur. The output of the LVDS drivers is a constant current source that delivers a nominal current of ~3.5mA through the 100Ω termination resistor. Assuming that the outputs are shorted, the 3.5mA flows through the short between the outputs. If LVDS receiver inputs are left floating, there is a failsafe mode on the Receiver that will force the outputs to a high state. The receiver fail-safe conditions are:

Open Input Pins

The unused inputs should be left OPEN. Do not tie unused receiver inputs to ground or any other voltages. This internal circuitry will guarantee a HIGH, stable output state for open inputs.

Terminated Input

If the driver is disconnected (cable unplugged), or if the driver is in a three-state or poweroff condition, the receiver output will again be in a HIGH state, even with the end of cable 100Ω termination resistor across the input pins.

Shorted Inputs

If a fault condition occurs that shorts the receiver inputs together, thus resulting in a 0V differential input voltage, the receiver output remains in a HIGH state. If both differential inputs are at V_{DD} the output will be HIGH. Shorted input fail-safe is not supported across the common-mode range of the device (V_{SS} to 2.4V). It is only supported with inputs shorted.

1.5 Clocks

The UT200SpW4RTR requires a transmit clock input for each of the ports. Each of the ports is capable of running at an independent speed up to 200 Mbps. Separate external clock signals must be provided if each port is going to run at a different rate.

If each Spacewire port is going to run at a different rate TX_CLK_IN_1, TX_CLK_IN_2, TX_CLK_IN_3, TX_CLK_IN_4, as well as HOST_CLK must be provided. Each of the SpaceWire ports is capable of running at an independent speed up to 200Mbps (200MHz clock). There is a one to-one rule for the SpaceWire ports clocks. If Port 1 is going to run at 160Mbps a clock of 160MHz needs to be provided, 40Mbps requires a 40MHz clock, etc.

The data values are transmitted directly and the strobe signal changes state whenever the data remains constant from one data bit interval to the next. The clock is recovered or extracted by XORing the data and strobe signals. There is a slight delay between edges of Data/Strobe, and the recovered clock. DS encoding allows for the SpaceWire port speeds to have same transmit clock speed and offers good jitter tolerance, but the receiver data is asynchronous to local (transmit) clock, refer to ECSS-E-ST-50-12C.

The HOST_CLK is used for the FIFO interface and also by the routing circuitry. The maximum HOST_CLK frequency is 50MHz. HOST_CLK frequency requirements are based on the fastest SpaceWire port data rate. There is a division by four rule that applies to HOST_CLK and the output ports of the router. If one port of the router is configured to run at 200Mbps, HOST_CLK must run at 50MHz. And if the maximum output frequency of one of the SpaceWire ports is 100Mbps HOST_CLK only needs to run at 25MHz. The clock requirements for the 4-Port Router are shown in Table 4.

Jitter on the input clocks must be minimized in order to reduce the cumulative effect on the data-strobe skew. Jitter on the TX_CLK_IN_n input clocks directly affect the data-strobe outputs. An unstable clock edge will skew the data-strobe alignment. Jitter must be accounted for in the system skew budget calculations.

It is recommended that the rate at which a SpaceWire link transmits and receives speeds are within 10x each other. Meaning if the UT200SpW4RTR is transmitting at 100Mbps, the receive side should be no less than 10Mbps.

1.5.1 Initialization and Link Run Data Rates

The SpaceWire standard requires an initialization data rate of 10Mbps, this provides the system with a common data rate while it is checked for proper operation. The TX_DIV[4:0] input signals are used to load Clock Divide registers for the10Mbps initialization data rate requirement. Once initialization is complete the data rate may go to the maximum specified by the user up to the maximum capability of the device. The user must know what division factor is needed for each port to divide down to 10Mbps.

Table 3: Clock Signals

Signal	I/O	Description
TX_CLK_IN_1	I	Transmit clock for Port 1. Max of 200 MHz
TX_CLK_IN_2	I	Transmit clock for Port 2. Max of 200 MHz
TX_CLK_IN_3	I	Transmit clock for Port 3. Max of 200 MHz
TX_CLK_IN_4	I	Transmit clock for Port 4. Max of 200 MHz
HOST_CLK	I	Used for all internal router functions and to read and write to/ from the External FIFO's and the SpaceWire FIFO's
TX_DIV[4:0]	I	Input clock divide for the initial 10 Mbps data rate

2.0 Router Architecture

The UT200SpW4RTR Router is a modular design consisting of four major blocks with descriptions of each as follows.

2.1 SpaceWire Link Protocol Handlers

There are four identical Link Protocol Handler (LPH) modules in the router. Each LPH consists of a Transmit FIFO, a receive FIFO, Receiver, Transmitter and Initialization block. All of these blocks combined are designed to handle the SpaceWire serial protocol as defined in document number ECSS-E-ST-50-12C.

2.2 Read Logic Block

There is a Read Logic Block connected to all four of the Receive FIFO's and the System Interface Transmit FIFO. This block monitors the empty flag on the receive FIFO and reads a byte of data whenever the FIFO is not empty. This block also checks the first byte of data read after an EOP to determine the port address or whether a configuration transaction will be initiated. A configuration transaction is described later in this document. For Path or Logical addressing, the Read Logic Block uses the first byte of data after an EOP/EEP.

Example:

If the first byte of data after an EOP/EEP is between 0x20 and 0xFF. The Read Logic Block uses the data as an address for the lookup table. The data stored in the lookup table will be used as the port address. The first byte of data with value 0x00 received by any router port after reset or an EOP/EEP will initiate a configuration transaction. If the first byte after an EOP/EEP is between0x01 and 0x05 path addressing will be used.

2.3 Write Logic Block

The Write Logic Blocks control the data to the transmit FIFOs and the System Receive Port (shown in figure 3). A "Round Robin" arbiter manages access and makes sure only one Read Logic Block accesses the Write Logic Block. If more than one receives ports is waiting to send data out of the same output port a round-robin arbitration scheme has been implemented.

It is also important to note that the configuration block will be accessing the Write Logic Block when read configuration packets are requested. In this case, the configuration block is treated as another Read Logic Block.

2.3.1 Arbitration

Each transmit FIFO (TX_FIFO in figure 6.) write logic block contains an arbiter that manages the flow of data to each of the four physical interface ports and the System Receive Port. The arbiter is a "Round Robin" type and gives each receive port equal opportunity for access. The arbiter starts counting whenever a request for that port is received from any of the five receive ports. The count is from Port 1, Port 2, etc. until the count reaches Port 5, looks for configuration commands, and then starts over.

Example:

If a transmit Port (this is any of the physical ports or the user interface port) receives a request, for example, from Port 1 and Port 5 at the same time, the Port 1 packet will be sent first. If during the time Port 1 packet is sent and a packet from Port 3 is requested, the Port 3 packet will be sent before Port 5 because of the way the arbiter counts.

2.4 Configuration

The Configuration block is used to set up lookup tables as well as registers that control the operation of the router. In addition, status registers and commands are accessed through this block.

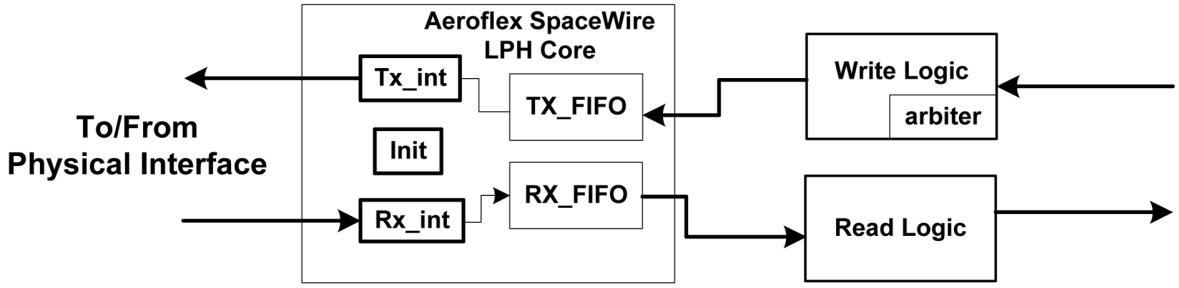


Figure 6. SpaceWire LPH Module

3.0 General Operation

The ECSS-E-ST-50-12C defines two types of characters, data and control characters. These characters are then further defined as either link characters or normal characters. A link character does not get passed from the Exchange Level to the Packet Level. Some examples of a Link character are flow control tokens (FCT), escape (ESC), NULL control code (ESC + FCT), and the Time-Codes (ESC + data character). A Normal Character ends with an EOP or EEP and is passed through the router at a packet level.

3.1 Data Character

Data characters hold an eight-bit data value, transmitted least significant bit (LSB) to most significant bit (MSB). A data character contains a parity bit, data-control flag, and eight bits of data. Per ECSS-E-ST-50-12C data parity is odd.

The parity bit will be calculated by adding the number of ones that are contained in the previous 8-bits of data. If the number of 1's in bits added together is even, the data character is said to have even parity. The data-control flag is set to zero to indicate that the current character is a data character. The following figure shows the 10-bit data character field. The LSB Bit "P" is the parity bit, bit "DC" is the data-control flag and must be set to zero for data, and Bits "D0 to D7" is the data. The parity bit covers the previous eight bits of a data character or two bits of a control character, the current parity bit and the current data-control flag. The parity bit is implemented in each data or control character to aid in detection of transmission errors.

3.2 Control Character

A control character is made up of a parity bit, data-control flag and two control bits. The data control flag is set to one to indicate that the current character is a control character. Parity coverage is similar to that for a data character. One of the four possible control characters is the escape code (ESC). This can be used to form control codes. Two control codes are specified and valid which are the NULL code and the Time-Code. The LSB of the control character is the parity bit "P", bit "DC" is the data control Bit and should be set to one for control, and Bits "C0 and C1" are the control codes. Refer to ECCS-E-ST-50- 12C section 7.3 for further details. The control codes are defined in Table 4.

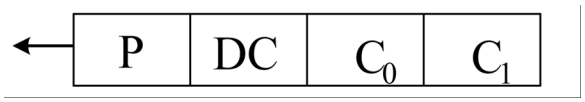


Figure 8. Control Characters

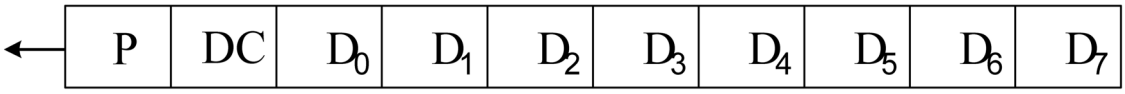


Figure 7A. Data Character

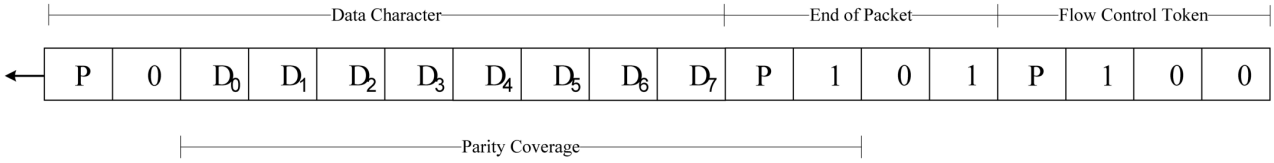


Figure 7B. Parity Coverage

3.3 Sending Packets

The first byte of data received on the bus after power up or after an EOP/EEP is the Header Byte. The EOP/EEP are treated the same by the router. The Header Byte determines whether Path Addressing (0x01 to 0x05), Logical Addressing (0x20 to 0xFF), or a Configuration Transaction 0x00 occur. If no Configuration Write transaction had occurred path addressing will be supported. Path addressing will be used because the lookup tables have not yet been configured. Currently, there is no restriction on the size of the packets that can be sent through the router.

3.4 Bad Packet

Packets that do not have a valid "Path Address" or do not have a look up table location configured are considered bad packets. Bad packets can be read from the receive FIFO, but not sent to any of the Transmit FIFOs. This is commonly known as" Spilling the Packet". The router supports Path Address from 1to 5 (physical output ports on the router) and logical address from 32 to 255, Figure 5.

Table 4. Control Character Table

Control Character	Definition	Character Type	C0:C1
FCT	Flow control token	Link	00
EOP	End of packet	Normal	01
EEP	Error end of packet	Normal	10
ESC	Escape	Link	11

Table 5. Bad Address Identification

Bad Address	Description
0x06 to 0x1F	The 4-Port Router has 4 SpaceWire ports and one external port for a total of 5 ports that will be supported using Path Addressing
0x20 to 0xFF that contain a value of 0x00	Look up tables will not be reset. Any unused Logical addresses should be set to contain hex 0x00.

4.0 Configuration Protocol

The UT200SpW4RTR 4-Port Router is configured through anyone of the four SpaceWire ports or the External Port. The default configuration is for all ports to be configuration ports. If one or more ports are set up to be configuration ports only one configuration command can be sent at a time.

4.1 Configuration Ports

If multiple ports are set up as configuration ports and more than one configuration command is being sent within the router the configuration packets will be corrupted.

The first byte of data with value 0x00 received by any router port after reset or an EOP/EEP will initiate a configuration transaction. (ECSS-E-ST-50-12C). Configuration transaction sallow access to the lookup tables, configuration registers and status registers. The packet protocols for configuration reads and writes are specified in the following two sections.

4.2 Configuration Write

A configuration write packet loads a 16-bit data word to the specified 16-bit address location in the configuration memory space. A configuration write packet begins with zero (0x00) or can contain additional router address bytes, followed the final destination address byte set to zero. A Configuration Write packet is shown in Figure 9.

Next, the router ID byte should be set to the value in the receiving router ID register. The Packet Type byte should be set to Write (see table 6.), followed by the address least significant byte, the address most significant byte, then the data least significant byte and the data most significant byte.

The last byte before the end of packet (EOP) will be the arithmetic Checksum value, which is an arithmetic sum of the final destination address, the router ID, the Packet Type, the Address and Data bytes. If the checksum value does not match, the command will not be executed. If the packet has less than eight (8) bytes or the Checksum value is not the last byte, the command will not be executed. (ECSS-E-ST-50-12C).

4.3 Configuration Read

The Read packet will read a number (Count) of 8-bit data values from consecutive 16-bit address locations and transmit the data to the return location specified. This packet begins with zero or more hardware or logical address bytes followed by the final destination address byte set to zero.

Next, the router ID byte should be set to the value in the route rid register, unless the router ID is being read. The Packet Type byte should be set to Read, (0x01 or 0x02) followed by the address least significant byte, the address most significant byte, the word count byte, and one or more return path address byte(s). The order of the return path address bytes are to read in the order they are received.

That is to say, the first return path address byte will be the path out of the first router with subsequent bytes to be used for the next layers of routers.

The last byte will be the checksum value, which is an arithmetic sum of the destination address, router ID, packet type, address bytes, data bytes and return path bytes.

If the checksum received does not match the calculated value, an error end of packet will be sent to the return address. The word count byte must be greater than zero. A value of zero will cause the command to not be executed. The return address path must contain one or more bytes and the first header byte must not be zero; otherwise the command will be considered invalid and not be executed. Figure 10 shows the bytes required for a Read Packet Command.

4.3.1 Read No Clear Packet Type

A read no clear packet type will read the data as requested in by the read request packet.

4.3.2 Read Clear Packet Type

The Read Clear packet type will read the data in the requested address space and delete the information contained there.

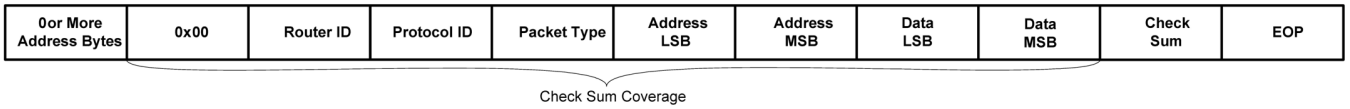


Figure 9. Configuration Port Write Packet Command

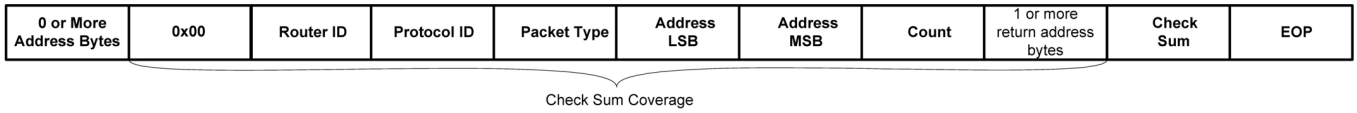


Figure 10. Configuration Port Read Packet Command

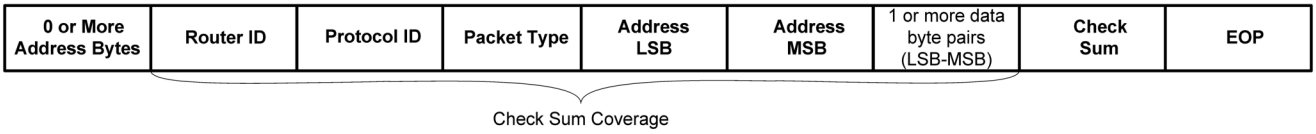


Figure 11. Configuration Port Read Packet Response

4.4 Configuration Read Response

The read response will follow the protocol shown in Figure 11A read response will be sent back to the requesting address after a Read command is executed. The Read packet command as shown in figure 5 sets up the address to read data from (Address LSB/MSB), how many 8-bit values to read (Count), and the return address bytes path. After the Read command is executed a Read Response command will be issued and will contain the data byte pairs read from the specified address.

4.5 Packet Type Byte Definition

The various configuration protocols define a "Packet Type" byte. This byte tells the router or the user in the case of the Read Response type what type of transaction is being commanded or received. Table 6 defines the different Packet Types.

Table 6. Packet Type Definitions

Packet Type	Value (HEX)
Write	0x00
Read no clear	0x01
Read clear	0x02
Read response	0x03
Reserved	0x04-0xFF

5.0 Port Addressing

5.1 Path Addressing

For any byte received immediately after an EOP/EEP byte with the value 0x01 to 0x05, path addressing will be implemented. Addresses from 0x06 to 0x1F will be spilled. The entire port address space is defined in Table 13.

5.2 Logical Addressing

There are 4 lookup tables (one for each port) on the router. Each lookup table is 224 by 16 and all 4 lookup tables have the same data written into them using the Configuration Protocol. A single configuration write will load each of the lookup tables with identical data the format for the lookup table data is described in the following sections.

5.2.1 Lookup Table Data Format

The lookup tables on the router are organized into 16-bits and are organized as shown in Table 7 below.

Table 7. Lookup Table Data Format

Parity	Unused			Enable Group Adaptive	Enable Header Delete	Group Adaptive Address Bits					Primary Logical Address Bits				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

5.2.2 Primary Logical Address Bits

The five LSB bits [4:0] are the Primary Logical Address bits and are for selecting ports 1 through 4 regardless of whether Group Adaptive has been enabled or not. When Group Adaptive has been enabled the router looks at the port address specified by these bits first and if that port is busy will then look at the port specified by the Group Adaptive Address Bits.

5.2.3 Group Adaptive Address Bits

Bits [9:5] are used when Group Adaptive has been enabled and the port selected by the Primary Logical Address Bits is busy. If group adaptive routing is not enabled and port selected by the Primary Logical Address Bits is busy the packet will have to wait until the selected port is free.

5.2.4 Enable Header Delete Bit

Bit [10] is used to enable the header delete function for the port selected by either the Group Adaptive Address bits or the Primary Logical Address Bits. Whenever this bit is set high the router will delete the header before sending the packet out of he requested transmit port.

5.2.5 Enable Group Adaptive Bit

Bit [11] is used to enable the Group Adaptive function on the router. Setting this bit high tells the router to use bits [9:5] for the port select in the event the port select for the Primary Address Bits is busy.

5.2.6 Unused Bits

Look up table bits [14:12] need to be set to 0x00. In order for the parity bit to be correct all three unused bits need to contain 0's. If these bits are set to something other than 0x00 the parity calculation it will not be the same as what the router is calculating.

5.2.7 Parity Bit

A Parity Bit is included for each lookup table location. The parity is even. When the header byte is decoded and falls between address 0x20 and 0xFF, a lookup table address will be retrieved by the lookup table.

Again, parity will be calculated by adding the number of ones that are contained in the previous 8-bits data. If the total number of 1's in bits added together is odd, the parity is odd parity. And if the number of 1's in bits added is even it is said to have even parity. The current parity bit will then be compared to the calculated parity and if they are not the same, the packet will bread out of the receive FIFO. This is commonly referred to as "Spilling the Packet". Additionally, the Parity Error Register will be incremented.

Parity error register is different from the previously discusses SpaceWire parity. The parity error register is based on the data in the lookup table.

6.0 Configuration and Status Registers

The router has a number of configuration and status registers which are used for initial setup of the router and for monitoring the router's performance. Table 14 is a summary of all the router registers with detailed descriptions outlined in each subsection.

6.1 Router Identification Register

The Router Identification Register is accessed through configuration address 0x0100 in Hex. The router ID defaults to 0x00upon reset and the user can write an 8-bit value using the configuration write protocol and using 00 for the router ID byte in the protocol.

Configuring the router ID register allows multiple routers to be networked together. Assuming each router has unique identifier, the router ID bits used in the configuration protocol will allow each individual router on the network, to have different look up table.

6.2 Version

This read only register located at address 0x0101 will tell the user what version of the router is being accessed.

6.3 Configure Port Enable

At power up, by default all of the ports on the router can be used as configuration ports. A Read and Write register at address 0X0102 allows the user the ability to specify certain ports as configuration ports. Refer to Table 8 for the bit mapping for this register.

Table 8. Configure Port Enable

Address	Bit Number	Description and Comments	
		Low	High
0x0102	0	Disable Port 1	Enable Port 1
	1	Disable Port 2	Enable Port 2
	2	Disable Port 3	Enable Port 3
	3	Disable Port 4	Enable Port 4
	4	Disable External	Enable External

6.4 Link Run Register

Address 0x0103 indicates to the user which ports are in the run state. Bit 0 is for port 1 and bit 4 is for the External Port.

Table 9. Link Run Register

Address	Bit Number	Port Number
0x0103	0	1
	1	2
	2	3
	3	4
	4	External

6.5 Transmit Full Register

Address 0x0104 indicates to the user which Transmit port FIFO's are full. Bit 0 is for port 1 and bit 4 is for the External Port.

6.6 Router Error Count

Address 0x0105 manages error counting. The port has an error counter that is 4-bits wide. Refer to Table 10 for the bit assignments for each error counter.

Table 10. Router Error Count Registers

Address HEX	Range	Error Counter
0x0105	[3:0]	Port 1
	[7:4]	Port 2
	[11:8]	Port 3
	[15:9]	Port 4

6.7 Parity Error Register

Any time a parity error is detected during a lookup table access register 0x0106 will get written to. Data is formatted as follows. Bit 5 indicates whether there has been a parity error during a Receive transaction. Bits 4 to 0 indicate which Receive Port the error occurred on.

6.8 Link Disable Register

All ports on the router can be enabled or disabled by writing into register 0x0107. Writing the appropriate bit in the Link Disable Register will disable that port. Refer to Table 11 for the bit assignments.

Table 11. Link Disable Register

Address	Bit Number	Description and Comments	
		High	Low
0x0107	0	Disable Port 1	Enable Port 1
	1	Disable Port 2	Enable Port 2
	2	Disable Port 3	Enable Port 3
	3	Disable Port 4	Enable Port 4

6.9 Port Busy Registers

Registers 0x0109 to 0x010D are to indicate which transmit ports busy administering a receive port. The five bit data field issued to indicate which transmit port is connected to the desired receive port.

6.10 Time Master Register

The Time Code Master Register, 0x010E, is used to tell the router which port is connected to the time master of the network. The default is Port 5, the external port.

6.11 Initialization Divide Registers

Used to set the correct 10Mbps transmit data rate during initialization. Value stored in registers 0x010F, 0x0110, 0x0111, and 0x0112 are 5-bit registers are used to divide the TX_CLK thus deriving the 10Mbps clock. On power up or reset the router will load the TX_DIV[4:0] bits into all 4 registers. The port that will be used to configure the router will have to have the correct value set by TX_DIV.

Example:

If the user wishes to configure the router through Port 3 and the transmit speed will be 100Mbps the user will need to set TX_DIV to 0x0A or 10 in decimal. Port 3 will have the correct divider for the 10Mbps clock and will be able to initialize the SpaceWire link. If the other ports are transmitting at different data rates the 10Mbps initialization data rate will not be correct. The user will then use Port 3 to set the Transmit 10Mbps Register such that the initialization data rate will be 10Mbps. Table 13 shows some common data rates along with the correct register value to achieve the 10Mbps initialization data rate.

Table 12. Clock Settings and Unit Data Rate

TX_CLK (Mbps)	TX_DIV[4:0] (HEX)	Initialization Data Rate (Mbps)
200	0x14	10
150	0x0F	10
10	0x01	10
5	0x01	5

It is important to note that if TX_CLK is set to less than 10Mbps the Initialization Divide Register must be set to 0x01.

The 4-Port Router will be able to initialize at these data rates. The user needs to be aware however to be careful not to send any data until the links are in the run state. If the initialization data rates are different, one side of the link could reach the run state before the other and if that link begins to send data there is a good possibility the other side will disconnect because it received a normal character before reaching the run state.

6.12 Router Reset

A write command to the address 0x0114 will reset the router with exception to the look up tables. SpaceWire ports are not reset, only the router which includes the state machines used to select ports and read and write to FIFO's.

6.13 Receive FIFO Reset

Writing to address 0x0115 and setting any or all of the 5 bits will reset the appropriate Receive FIFO. For example, setting bit 0 will reset the Receive FIFO of Port 1. Setting bit 1 will reset the Port 2 Receive FIFO and so on.

6.14 Transmit FIFO Reset

This 5-bit register at address 0x0116 is used to reset any or all of the Transmit FIFOs. Bit 0 will reset Port 1, Bit 1 will reset Port 2 and so on.

Table 13. Header Byte Memory Map

Port Address Byte (HEX)	Port
0x00	Configuration access
0x01	Path address for Port 1
0x02	Path address for Port 2
0x03	Path address for Port 3
0x04	Path address for Port 4
0x05	Path address for Port 5
0x06 to 0x1F	Not used
0x20 to 0xFF	Logical address locations

Table 14: Configuration and Status Registers

Address (Hex)	R/W	Name	Default (Hex)	Description	Number Bits
0x0020-0x00FF	R/W	Lookup table	XXXX	Logical Address Lookup Table. Look up tables are not reset. User should initialize the unused addresses to 0x00.	
0x0100	R/W	Router ID	0X00	Router Identification Register	8
0x0101	R	Version register	0X01	Router Version Register	
0x0102	R/W		0X1F	Using this register, ports can be enabled or disabled as configuration ports.	5
0x0103	R	Link run register	0X00	Indicates which ports are in the run state. One bit for each port	4
0x0104	R	Transmit full register	0X00	Transmit FIFO Full Register. Indicates which Transmit FIFO's are Full, one bit for each Transmit FIFO	5
0x0105	R/RC	Router error count	0X00	Router Error Count Registers. Each nibble within this register represents the SpaceWire error count for a given router port.	
0x0106	R/RC	Parity error register	0X00	Indicates when a parity error has occurred and the receive port number that last showed an error	6
0x0107	R/W	Link disable register	0X00	Enables or Disables individual links	4
0x0108	R/W	Reserved	0X00		
0x0109 to 0x010D	R	Port busy registers	0X00	These registers indicate the current receive port to transmit port connection. Address 0109 is for Receive Port 1 and address 010D is for the External Port	5
0x010E	R/W	Time master select register	0X05	This register is used to tell the router which port is connected to the time master	3
0x010F	R/W	Port 1 initialization divide register	TX_DIV	Port 1 10Mbps data rate divider	5
0x0110	R/W	Port 2 initialization divide register	TX_DIV	Port 2 10Mbps data rate divider	5
0x0111	R/W	Port 3 initialization divide register	TX_DIV	Port 3 10Mbps data rate divider	5
0x0112	R/W	Port 4 initialization divide register	TX_DIV	Port 4 10Mbps data rate divider	5
0x0113	R/W	Protocol ID	0X00	Programmable Protocol Identifier	
0x0114	W	Router reset	N/A	A write command to this address will reset the entire router. The data in this case is don't care	
0x0115	W	Receive FIFO reset	N/A	Used to Reset any or all of the Receive FIFO's	5
0x0116	W	Transmit FIFO reset	N/A	Used to Reset any or all of the Transmit FIFO's	5

7.0 Time Codes

Time codes are handled as they are described in the standard. A time code distributes system time over a network. A Time code does not get saved into the FIFO memory buffer. Any valid time code received on a router port will be sent to all of the other ports of the router. A valid time code is defined as a time code value that is one greater than the previous time code value.

A time code is made up of an ESC character followed by eight bit data character. The data character holds six bits of system time and two reserved bits. Bits "T0 to T5" are the 6-bit time counter and are the LSB of the time code. Bits "T6 to T7" are the timing control flags (currently reserved by the working group) and should both be set to zero. Figure 12 illustrates a time-code packet

7.1 System Time Management

The timing of the system is controlled by two signals, TICK_IN and TICK_OUT. TICK_IN and TICK_OUT are the system time controllers is the external port is the time master. When a TICK_IN is received it tells the node to send a Time Code Character. Only one node in the system should have an active TICK_IN and that node will provide the master time reference for the entire network. Then TICK_OUT is asserted it tells the user that a Valid time code character has been received.

7.2 Transmit Time

The transmitter encodes data and transmits it through the network using DS encoding. The transmitter must receive either a Time-Code, flow control token (FCT), or an N-Char (data, EOP or EEP) to initiate a transmit transaction. If the transmitter does not have any data to send it will send NULL characters.

The transmitter sends N-Chars if the node at the other end of the link has room in the receive FIFO buffer. A transmit transactions initiated by the node at the end of the link sending a FCT, this tells the transmitter that the node that it is ready to accept another8 N-Chars. The transmitter keeps track of the FCTs received and the number of N-Chars sent to avoid input buffer overflow. This is done by the transmitter holding a credit count of the number of characters it has been given permission to send.

7.3 Time Code Latency

SpaceWire system time accuracy is dependent on the number of links traversed and the operating speed of each link. A delay approximately 14-bit periods (ESC + data character) is added to the system time for each link the time code traverses. Time code skew across a network is equal to tTCSKEW = (14*S)/A where S is the number of SpaceWire links traversed, A is the average link operating speed, and 14 is the time code bit period.

7.4 Transmitter Status

The transmitter can be in one of four states:

Reset: The transmitter does nothing.

Send NULLs: Transmitter will only send NULLs out on the link. No N-Chars are read in from the Transmit Host Interface. Transmitter will not accept an order to send FCT from the Host System. It does not send Time-Codes.

Send FCTs or NULLs: Transmitter can send flow control tokens or NULLs, but still does not read N-Chars from the Transmit Host Interface. It does not send Time-Codes.

Send Time-Codes, FCTs, N-Chars or NULLs: Normal system operation. Transmitter is sending NULLs, FCTs, Time-Codes and N-Chars.

Figure 12. Time Code

8.0 Control Signals

8.1 LV_$\overline{CM}$

Allows the user to select the external interface either LVDS or LVCMOS. When LV_ $\overline{CM}$ is high the LVDS interface will be active. For example signal I/O that will be active areTX1_D_LV[1:0], TX1_S_LV[1:0], RX1_D_LV[1:0], and RX1_S_LV[1:0]. While TX1_D, TX1_S, RX1_D, and RX1_Swould be tri-stated. Table 15 shows the relationship between LV_$\overline{CM}$ and the transmit receive interface.

8.2 $\overline{OE}$

This signal is used to control the outputs of the Receive FIFO. $\overline{OE}$ supports the memory interface timing of host controller that incorporates multiplexed address and data on the bus. If no $\overline{OE}$ signal is available for the host controller, and the $\overline{CSEL}$ signal is asserted while the controller still has its address information on the bus, data may be driven onto the bus and cause bus contention.

8.3 $\overline{CSEL}$

Allows the state of the control signals for FIFOs to be connected to internal router logic. If $\overline{CSEL}$ is "High" the signals $\overline{TX\_PUSH}$, $\overline{RX\_POP}$, and any other backend inputs should not be allowed to be passed on to internal logic. Additionally, output signals RX_DATA and TIME_CODE[7:0] should be tristated. See Table 16.

It should be noted that TICK_IN and TICK_OUT are independent of the states of output enable ($\overline{OE}$), chip select ($\overline{CSEL}$), reset($\overline{RST}$). And the time code (TIME_CODE[7:0]) port will come up as an input port because the default time master is the external port.

Table 15. Control Signals

LV_$\overline{CM}$	TX#_D_LV/TX#_S_LV RX#_D_LV/RX#_S_LV (LVDS)	TX#_D/TX#_S RX#_D/RX#_S (LVCMOS)
1	Active	Z
0	Z	Active

Table 16. Enable and Select Signals Truth Table

$\overline{OE}$	$\overline{CSEL}$	$\overline{RST}$	TIME_CODE[7:0]	RX_DATA[8:0]	$\overline{TX\_PUSH}$ / $\overline{RX\_POP}$
1	1	1	Active	Z	Inactive
1	1	0	Z	Z	Inactive
1	0	1	Active	Z	Active
1	0	0	Z	Z	Inactive
0	1	1	Active	Z	Inactive
0	1	0	Z	Z	Inactive
0	0	1	Active	Active	Active
0	0	0	Z	Z	Inactive

9.0 Service Configuration

There are a few different ways that the UT200SpW4RTR can be configured to service multiple system requirements

9.1 Stand Alone Router

The router can be used as a stand-alone router with up to four SpaceWire links connected to it, Figure 13. Configuration of the lookup tables should be done by sending packets containing configuration commands.

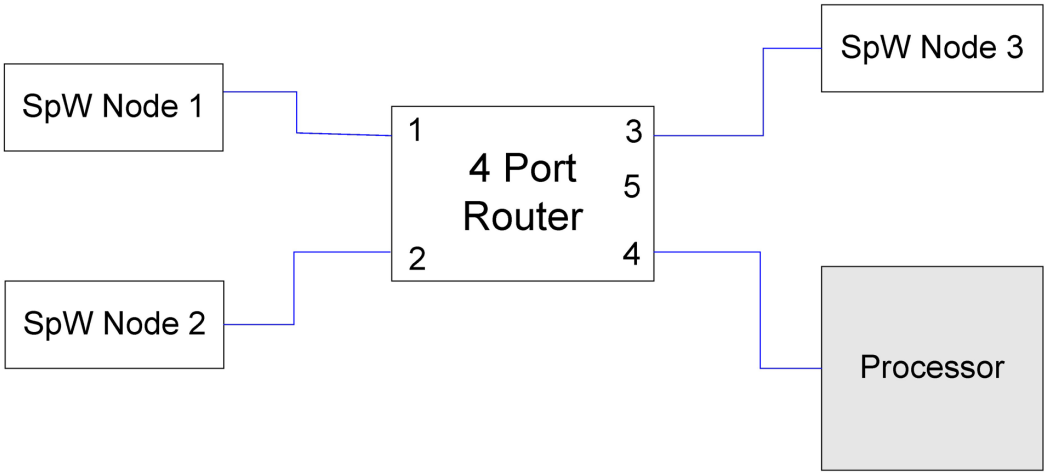


Figure 13. Stand Alone Router Configuration

9.2 Interfacing Multiple Routers

Network topology may require a router with more than four SpaceWire ports or more system ports. Multiple four port routers can be interfaced together in numerous configurations to produce the required I/O count.

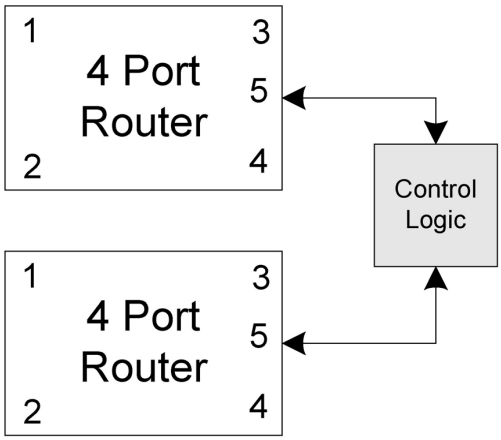


Figure 14. 8-Port Extended Configuration using External Logic

Routers can be connected together via the system ports to expand to an 8-Port Router. External logic will be required to connect the system ports together in this way. The router ID register for each of the routers connected in this way should be unique. An extra path addressing byte will be needed to route packets between the routers connected through the system ports.

Three routers can be connected to a FPGA or processor through the system port and to each other through the SpaceWire ports. This configuration generates eight SpaceWire ports for connection to SpaceWire nodes. The system ports of each router are used to connect to user logic in an FPGA or processor.

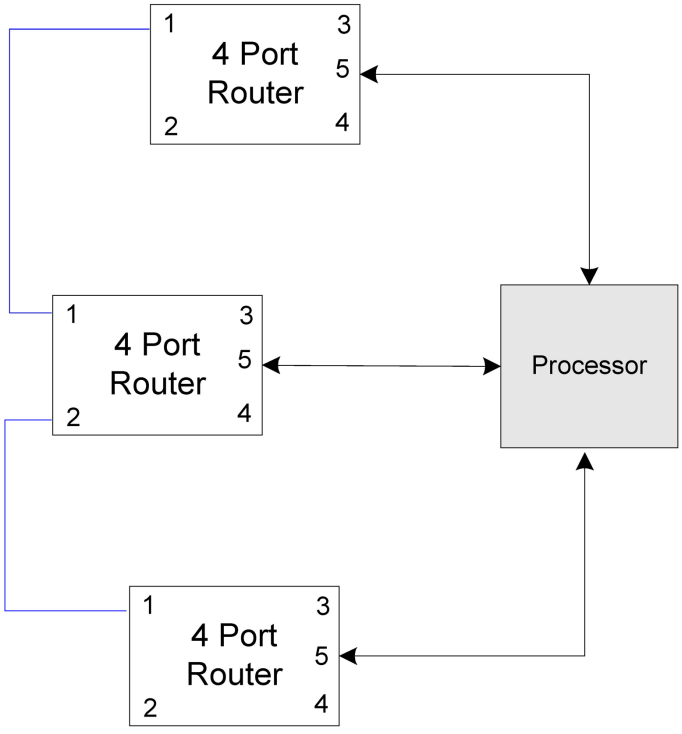


Figure 15. 8-Port Extended Configuration Using uP

10.0 Networking

Many network configurations are possible using the 4-PortRouter. Certain parameters need to be considered when choosing a network topology to use. Performance, fault-tolerance, and harness mass are key attributes a designer must consider when designing a SpW network.

10.1 Centralized Networks

In a centralized network configuration, all communications are routed by a router at the center of the network. Allows certain functions are handled by the router, resulting in high performance. If a failure occurs on one node, other nodes are not affected. Centralized networks are simple to configure because the look up tables do not need to be configured. Data can be easily accessed from all nodes via the central router. Centralization's weaknesses is the heavy reliance on the central router and the high harness mass required.

10.2 Distributed Networks

Distributed network configurations are characterized by smaller routers all connected together. Many configurations are possible, allowing for a more reliable system. All nodes on the network are connected together through some route. Data can be accessed from all nodes but a path must be specified for how to route the data through the network. Distributed networks are more complex to configure because the Lookup tables usually need to be configured resulting in slower performance.

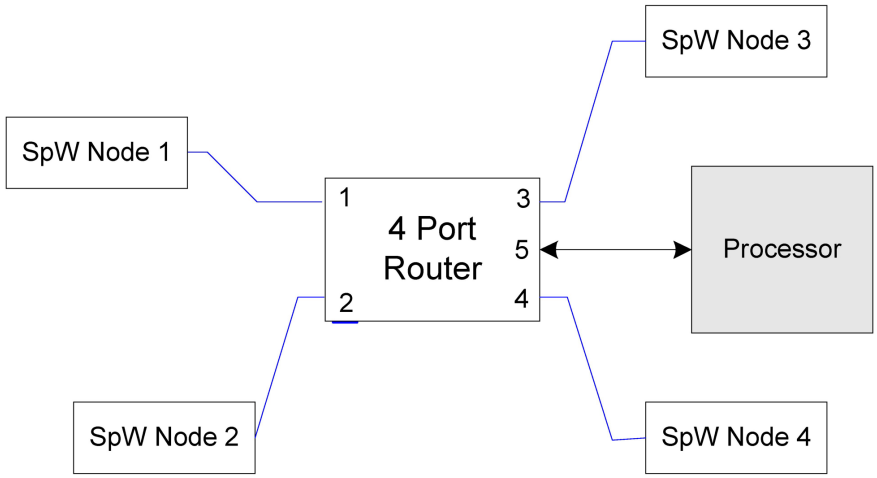


Figure 16. Centralized Network Example

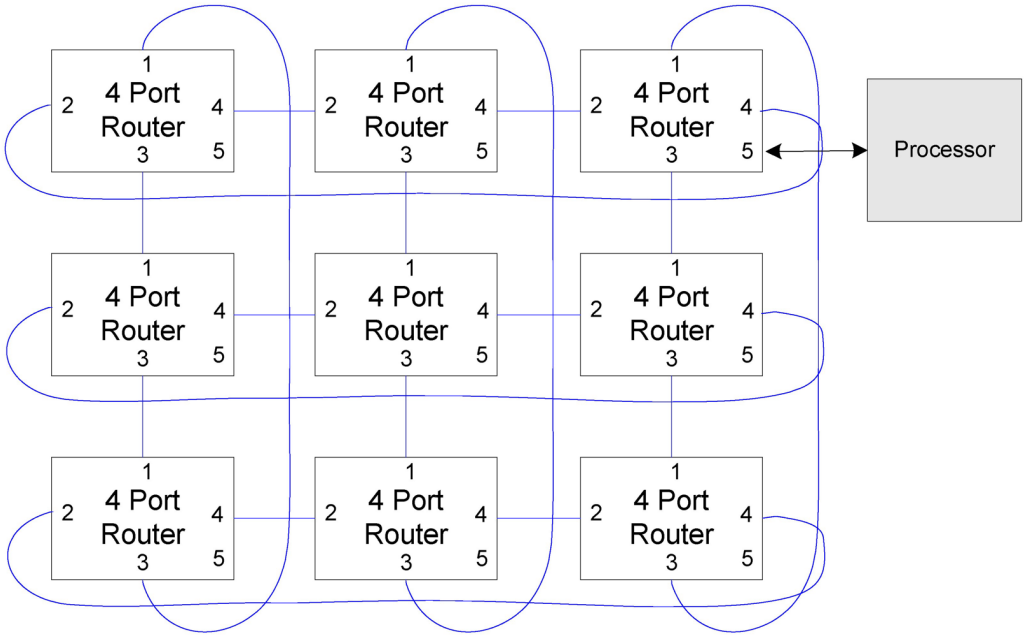


Figure 17A. Distributed Network Example #1

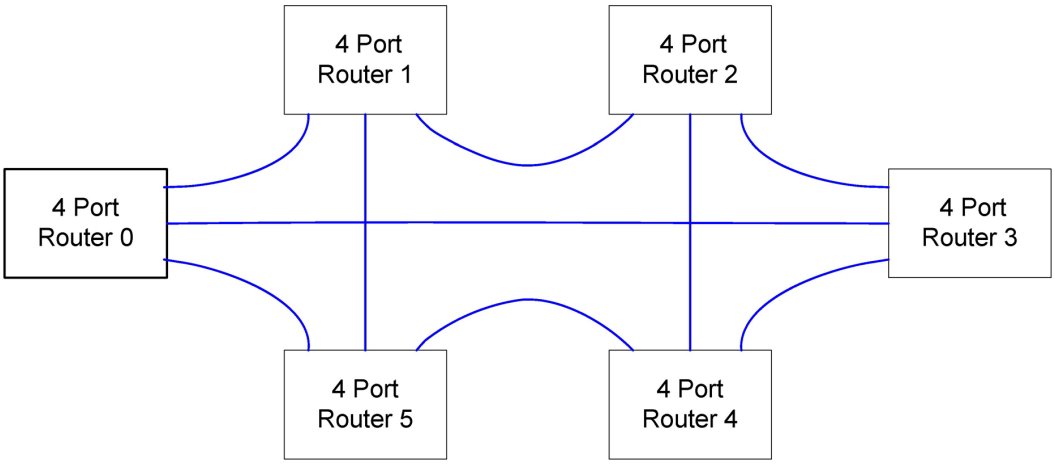
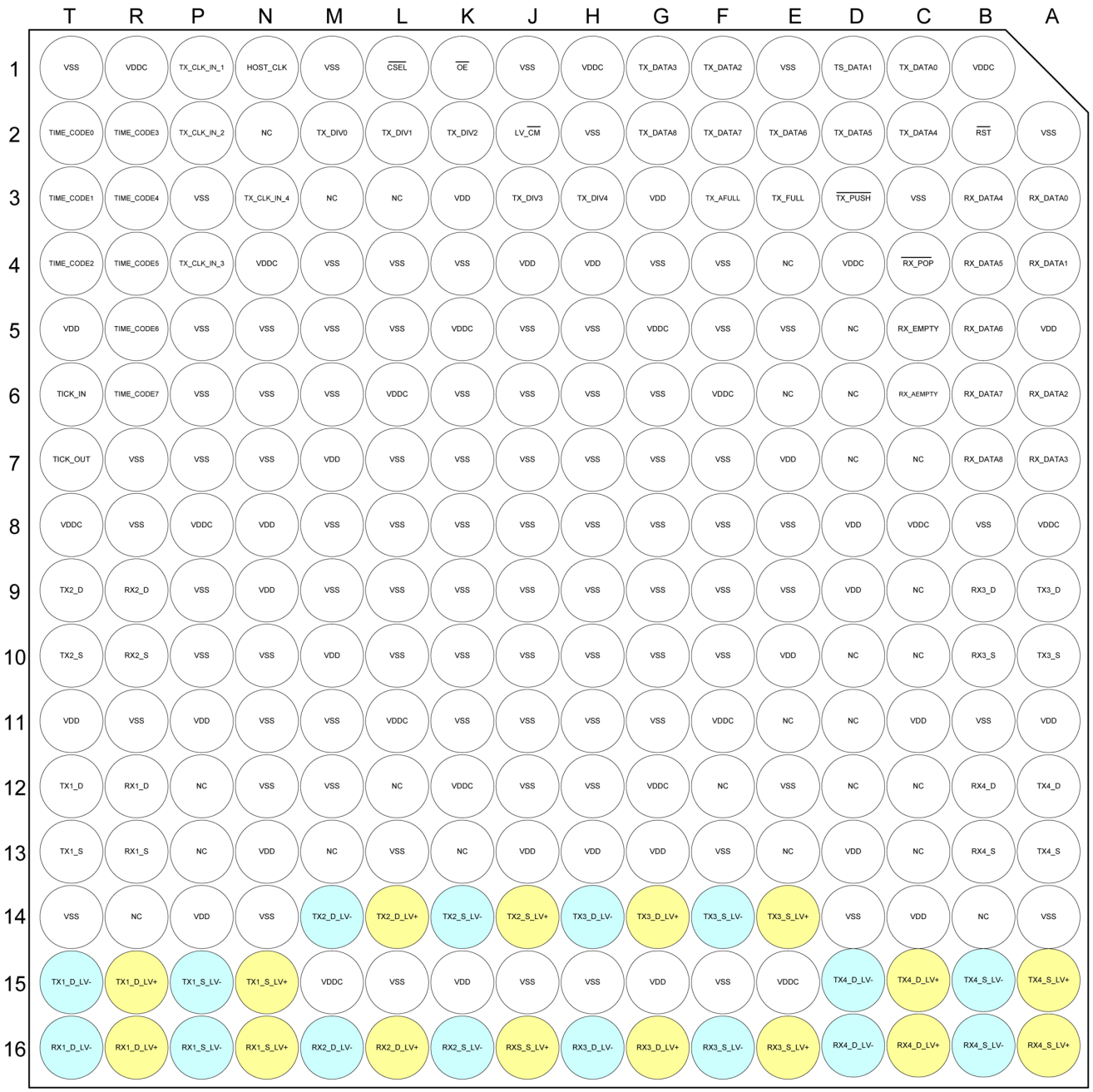


Figure 17B. Distributed Network Example #2

4-Port SpaceWire Router

UT200SpW4RTR

11.0 255-Lead CLGA Pin Out



	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A
1	VSS	VDDC	TX_CLK_IN_1	HOST_CLK	VSS	$\overline{CSEL}$	$\overline{OE}$	VSS	VDDC	TX_DATA3	TX_DATA2	VSS	TS_DATA1	TX_DATA0	VDDC	
2	TIME_CODE0	TIME_CODE3	TX_CLK_IN_2	NC	TX_DIV0	TX_DIV1	TX_DIV2	LV_$\overline{CM}$	VSS	TX_DATA8	TX_DATA7	TX_DATA6	TX_DATA5	TX_DATA4	$\overline{RST}$	VSS
3	TIME_CODE1	TIME_CODE4	VSS	TX_CLK_IN_4	NC	NC	VDD	TX_DIV3	TX_DIV4	VDD	TX_AFULL	TX_FULL	$\overline{TX\_PUSH}$	VSS	RX_DATA4	RX_DATA0
4	TIME_CODE2	TIME_CODE5	TX_CLK_IN_3	VDDC	VSS	VSS	VSS	VDD	VDD	VSS	VSS	NC	VDDC	$\overline{RX\_POP}$	RX_DATA5	RX_DATA1
5	VDD	TIME_CODE6	VSS	VSS	VSS	VSS	VDDC	VSS	VSS	VDDC	VSS	VSS	NC	RX_EMPTY	RX_DATA6	VDD
6	TICK_IN	TIME_CODE7	VSS	VSS	VSS	VDDC	VSS	VSS	VSS	VSS	VDDC	NC	NC	RX_AEMPTY	RX_DATA7	RX_DATA2
7	TICK_OUT	VSS	VSS	VSS	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD	NC	NC	RX_DATA8	RX_DATA3
8	VDDC	VSS	VDDC	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD	VDDC	VSS	VDDC
9	TX2_D	RX2_D	VSS	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD	NC	RX3_D	TX3_D
10	TX2_S	RX2_S	VSS	VSS	VDD	VSS	VSS	VSS	VSS	VSS	VSS	VDD	NC	NC	RX3_S	TX3_S
11	VDD	VSS	VDD	VSS	VSS	VDDC	VSS	VSS	VSS	VSS	VDDC	NC	NC	VDD	VSS	VDD
12	TX1_D	RX1_D	NC	VSS	VSS	NC	VDDC	VSS	VSS	VDDC	NC	VSS	NC	NC	RX4_D	TX4_D
13	TX1_S	RX1_S	NC	VDD	NC	VSS	NC	VDD	VDD	VDD	VSS	NC	VDD	NC	RX4_S	TX4_S
14	VSS	NC	VDD	VSS	TX2_D_LV-	TX2_D_LV+	TX2_S_LV-	TX2_S_LV+	TX3_D_LV-	TX3_D_LV+	TX3_S_LV-	TX3_S_LV+	VSS	VDD	NC	VSS
15	TX1_D_LV-	TX1_D_LV+	TX1_S_LV-	TX1_S_LV+	VDDC	VSS	VDD	VSS	VSS	VDD	VSS	VDDC	TX4_D_LV-	TX4_D_LV+	TX4_S_LV-	TX4_S_LV+
16	RX1_D_LV-	RX1_D_LV+	RX1_S_LV-	RX1_S_LV+	RX2_D_LV-	RX2_D_LV+	RX2_S_LV-	RXS_S_LV+	RX3_D_LV-	RX3_D_LV+	RX3_S_LV-	RX3_S_LV+	RX4_D_LV-	RX4_D_LV+	RX4_S_LV-	RX4_S_LV+

12.0 Pin Descriptions

System Pins				
Pin No.	**Pin Name**	**I/O**	**Type**	**Description**
	V_{DDC}	PWR	Power	Core Power Supply 2.5V
	V_{DD}	PWR	Power	I/O Power Supply3.3V
	GND	PWR	Power	Ground VSS
N1	HOST_CLK	I	LVCMOS	50MHz system clock

SpaceWire Interface				
Pin No.	**Pin Name**	**I/O**	**Type**	**Description**
B2	$\overline{RST}$	I	LVCMOS Schmitt	RST must remain low for 6 clock cycles before transitioning high, and must transition high 3 clock cycles before valid data.
P1	TXCLK_IN_1	I	LVCMOS	Clock input 1 to transmitter used to clock LVDS output. Any phase relationship is allowed between TXCLK _IN & HOST_CLK.
P2	TXCLK_IN_2	I	LVCMOS	Clock input 2 to transmitter used to clock LVDS output. Any phase relationship is allowed between TXCLK_IN & HOST_CLK.
P4	TXCLK_IN_3	I	LVCMOS	Clock input 3 to transmitter used to clock LVDS output. Any phase relationship is allowed between TXCLK_IN & HOST_CLK.
N3	TXCLK_IN_4	I	LVCMOS	Clock input 4 to transmitter used to clock LVDS output. Any phase relationship is allowed between TXCLK_IN & HOST_CLK.
T12	TX1_D	O	HS-LVCMOS	Transmit data for Port 1 High speed CMOS 12mA I/O buffers
T13	TXI_S	O	HS-LVCMOS	Transmit strobe for Port 1
R12	RXI_D	I	HS-LVCMOS	Receive data for Port 1
R13	RXI_S	I	HS-LVCMOS	Receive strobe for Port 1
T9	TX2_D	O	HS-LVCMOS	Transmit data for Port 2
T10	TX2_S	O	HS-LVCMOS	Transmit strobe for Port 2
R9	RX2_D	I	HS-LVCMOS	Receive data for Port 2
R10	RX2_S	I	HS-LVCMOS	Receive strobe for Port 2
A9	TX3_D	O	HS-LVCMOS	Transmit data for Port 3
A10	TX3_S	O	HS-LVCMOS	Transmit strobe for Port 3
B9	RX3_D	I	HS-LVCMOS	Receive data for Port 3
B10	RX3_S	I	HS-LVCMOS	Receive strobe for Port 3
A12	TX4_D	O	HS-LVCMOS	Transmit data for Port 4
A13	TX4_S	O	HS-LVCMOS	Transmit strobe for Port 4
B12	RX4_D	I	HS-LVCMOS	Receive data for Port 4
B13	RX4_S	I	HS-LVCMOS	Receive strobe for Port 4

4-Port SpaceWire Router

UT200SpW4RTR

(continued)

SpaceWire Interface				
Pin No.	**Pin Name**	**I/O**	**Type**	**Description**
M2 L2 K2 J3 H3	TX_DIV[4:0]	I	LVCMOS	Initial Transmit divide by input. On power up of RST assertion the data set by these pins will be loaded into all 4 of the Initialization Divide Registers.
R16 T16	RX1_D_LV+ RX1_D_LV-	I	LVDS	Port 1 Non-inverting receive data input pin Port 1 Inverting receive data input pin
N16 P16	RX1_S_LV+ RX1_S_LV-	I	LVDS	Port 1 Non-inverting receive strobe input pin Port 1 Inverting receive strobe input pin
R15 T15	TX1_D_LV+ TX1_D_LV-	O	LVDS	Port 1 Inverting transmit data output pin Port 1 Non-inverting transmit data output pin
N15 P15	TX1_S_LV+ TX1_S_LV-	O	LVDS	Port 1 Non-inverting transmit strobe output pin Port 1 Inverting transmit strobe output pin
L16 M16	RX2_D_LV+ RX2_D_LV-	I	LVDS	Port2Non-inverting receive data input pin Port 2 Inverting receive data input pin
J16 K16	RX2_S_LV+ RX2_S_LV-	I	LVDS	Port 2 Non-inverting receive strobe input pin Port 2 Inverting receive strobe input pin
L14 M14	TX2_D_LV+ TX2_D_LV-	O	LVDS	Port 2 Non-inverting transmit data output pin Port 2 Inverting transmit data output pin
J14 K14	TX2_S_LV+ TX2_S_LV-	O	LVDS	Port 2 Non-inverting transmit strobe output pin Port 2 Inverting transmit strobe output pin
G16 H16	RX3_D_LV+ RX3_D_LV-	I	LVDS	Port 3 Non-inverting receive data input pin Port 3 Inverting receive data input pin
E16 F16	RX3_S_LV+ RX3_S_LV-	I	LVDS	Port 3 Non-inverting receive strobe input pin Port 3 Inverting receive strobe input pin
G14 H14	TX3_D_LV+ TX3_D_LV-	O	LVDS	Port 3 Non-inverting transmit data output pin Port 3 Inverting transmit data output pin
E14 F14	TX3_S_LV+ TX3_S_LV-	O	LVDS	Port 3 Non-inverting transmit strobe output pin Port 3 Inverting transmit strobe output pin
C16 D16	RX4_D_LV+ RX4_D_LV-	I	LVDS	Port 4 Non-inverting receive data input pin Port 4 Inverting receive data input pin
A16 B16	RX4_S_LV+ RX4_S_LV-	I	LVDS	Port 4 Non-inverting receive strobe input pin Port 4 Inverting receive strobe input pin
C15 D15	TX4_D_LV+ TX4_D_LV-	O	LVDS	Port 4 Non-inverting transmit data output pin Port 4 Inverting transmit data output pin
A15 B15	TX4_S_LV+ TX4_S_LV-	O	LVDS	Port 4 Non-inverting transmit strobe output pin Port 4 Inverting transmit strobe output pin
J2	LV_$\overline{CM}$	I	LVCMOS	Interface Enable used to select LVDS I/O or LVCMOS

4-Port SpaceWire Router

UT200SpW4RTR

Time Code Signal				
Pin No.	**Pin Name**	**I/O**	**Type**	**Description**
T6	TICK_IN	I	LVCMOS	When asserted and the link interface is in the Run state the transmitter sends a Time-Code immediately after the current character has been transmitted. Six-bit time input port, a two-bit control flag input port.
T7	TICK_OUT	O	LVCMOS	Will be asserted whenever the link interface is in the Run state and the receiver receives a valid Time-Code. A six-bit time output port and a two-bit control flag output port.
T2 T3 T4 R2 R3 R4 R5 R6	TIME_CODE0 TIME_CODE1 TIME_CODE2 TIME_CODE3 TIME_CODE4 TIME_CODE5 TIME_CODE6 TIME_CODE7	I/O	LVCMOS	8 bit Time code port.

System Interface FIFOs				
Pin No.	**Pin Name**	**I/O**	**Type**	**Description**
C1 D1 F1 G1 C2 D2 E2 F2 G2	TX_DATA0 TX_DATA1 TX_DATA2 TX_DATA3 TX_DATA4 TX_DATA5 TX_DATA6 TX_DATA7 TX_DATA8	I	LVCMOS	Data Inputs for 9-bit Bus
A3 A4 A6 A7 B3 B4 B5 B6 B7	RX_DATA0 RX_DATA1 RX_DATA2 RX_DATA3 RX_DATA4 RX_DATA5 RX_DATA6 RX_DATA7 RX_DATA8	O	LVCMOS	Data Outputs for 9-bit Bus
K1	$\overline{OE}$	I	LVCMOS	External Port Output Enable
L1	$\overline{CSEL}$	I	LVCMOS	External Chip Select input

System Interface FIFOs				
Pin No.	**Pin Name**	**I/O**	**Type**	**Description**
D3	$\overline{\text{TX\_PUSH}}$	I	LVCMOS	Transmit Push signal. One location of data will be loaded in the Transmit FIFO on the Rising Edge of HOST_CLK when TX_PUSH is Low
C4	$\overline{\text{RX\_POP}}$	I	LVCMOS	Receive Pop Signal. FIFO pop request, active low
C5	RX_EMPTY	O	LVCMOS	Empty Flag: When RX_EMPTY is High, the RECEIVE FIFO is empty. Synchronized to HOST_CLK.
E3	TX_FULL	O	LVCMOS	Full Flag: When TX_FULL is HIGH, the TRANSMIT FIFO is full. FF is synchronized to HOST-CLK.
C6	RX_AEMPTY	O	LVCMOS	Almost Empty: When the RX_AEMPTY is High, the RECEIVE FIFO is 8 locations from being empty.
F3	TX_AFULL	O	LVCMOS	Almost Full: When the TX_AFULL is High, the TRANSMIT FIFO is 8 locations from being full.

13.0 Operational Environment

Parameter	Limits	Units
Total Ionizing Dose (TID)	>1E5	rads(Si)
Single Event Latchup (SEL) [2]	>100	MeV-cm^2/mg
SEU Saturated Cross-Section	1.1E-6	cm^2/port
Onset Single Event Upset (SEU) LET [3]	>28	MeV-cm^2/mg
Neutron Fluence	1E14	n/cm^2

Notes:

1) Worst case temperature and voltage of T_C = +125°C, V_{DD} = 3.6V, V_{DDC} = 2.7V for SEL.
2) Worst case test temperature and voltage of T_C = +25°C, V_{DD} = 3.0V, V_{DDC} = 2.5V for SEU.

14.0 Electrical Characteristics

14.1 Absolute Maximum Ratings: [1]

(Referenced to VSS)

Symbol	Description	Limits	Units
V_{DDC}	Core supply voltage	-0.3 to 3.6	V
V_{DD}	I/O supply voltage	-0.3 to 4.3	V
$V_{I/O}$	Voltage on any pin during operation	-0.3 to V_{DD} + 0.3	V
I_I	DC Input Current	±10	mA
P_D [2]	Maximum Package Power Dissipation permitted at T_C=105°C	11	W
T_{STG}	Storage Temperature	-65 to +150	°C
Θ_{JC}	Thermal Resistance, Junction to Case	4.0	°C/W
T_J	Junction Temperature	150	°C

Notes:

1) Stresses outside the listed absolute maximum ratings may caught permanent damage to the device. This is stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2) Per MIL-STD-883, Method 1012.1, Section 3.4.1, $P_D = \frac{T_J\ (MAX) - T_C\ (MAX)}{\Theta_{JC}}$

14.2 Recommended Operating Conditions

Symbol	Description		Limits	Units
V_{DDC}	Core supply voltage		2.3 to 2.7	V
V_{DD}	I/O supply voltage		3.0 to 3.6	V
V_{IN}	Input voltage on any pin		0 to V_{DD}	V
T_C	Case Temperature		-40 to +105	°C
t_{RISE}	Input Rise Time	CMOS Inputs (VIL-VIH)	≤ 20	ns
		LVDS Inputs (VTL-VTH)	≤ 20	ns
t_{FALL}	Input Fall Time	CMOS Inputs (VIH-VIL)	≤ 20	ns
		LVDS Inputs (VTH-VTL)	≤ 20	ns

14.3 DC Electrical Characteristics - LVDS Driver (Pre and Post-Radiation) *

(V_{DD} = 3.3V ± 0.3V; V_{DDC} = 2.5V ± 0.2V) Unless otherwise noted, Tc is per the temperature range ordered

Symbol	Parameter	Condition	MIN	MAX	Unit
V_{OL}	Low-level output voltage	R_L = 100Ω	0.8	---	V
V_{OH} [5]	High-level output voltage	R_L = 100Ω	---	2.1	V
V_{OD} [1, 5]	Differential Output Voltage	R_L = 100Ω	250	600	mV
ΔV_{OD} [1]	Change in Magnitude of VOD for Complementary Output States	R_L = 100Ω	---	35	mV
V_{OS} [5]	Offset Voltage	R_L = 100Ω,	1.1	1.8	V
ΔV_{OS}	Change in Magnitude of V_{OS} for Complementary Output States	$R_L = 100\Omega\ \frac{V_{OH}+V_{OL}}{2} = V_{OS}$	---	25	mV
I_{OS} [2, 3]	Output Short Circuit Current	V_{OUT}+ = 0V or V_{DD} V_{OUT}- = 0V or V_{DD}	-9.0	9.0	mA
I_{OZ}	Output Three-State Current	LV_$\overline{CM}$ = V_{SS} V_O = 0V or V_{DD}, V_{DD} = 3.6V	-10	+10	µA
$C_{OUTLVDS}$ [4]	LVDS Output Capacitance		---	10	pF

Notes:
*For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A, up to the maximum TID level procured.

1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except differential voltages.
2) Guaranteed by characterization
3) Output short circuit current (IOS) is specified as magnitude only, minus sign indicates direction only.
4) Capacitance is measured for initial qualification and when design changes may affect the input/output capacitance. Capacitance is measured between the designated terminal and VSS at a frequency of 1MHz and a signal amplitude of 50mV maximum.
5) Supplied as a design guideline, not tested or guaranteed.

14.4 DC Electrical Characteristics - LVDS Receiver (Pre and Post-Radiation) *[1]

(V_{DD} = 3.3V ± 0.3V; V_{DDC} = 2.5V ± 0.2V) Unless otherwise noted, Tc is per the temperature range ordered.

Symbol	Parameter	Condition	MIN	MAX	Unit
V_{CMR} [2]	Common mode supply voltage	V_{ID} = 200mV peak-to-peak	0.1	2.3	V
I_{LVDIN}	Receiver input current	V_{IN} =2.4V	-15	15	µA
I_{CS}	Cold spare leakage current	V_{IN} = 3.6V, V_{DD} = V_{SS}	-10	10	µA
V_{TH} [2]	Differential input high threshold	VCM = +1.2V	V_{CM} +0.1	---	V
V_{TL} [2]	Differential input low threshold	VCM = +1.2V	---	V_{CM} -0.1	V
V_{CL}	Input Clamp Voltage	I_{IN} = ± 1.0mA	-1.5	-0.4	V
C_{INLVDS} [3]	LVDS Input Capacitance		---	10	pF

Notes:
*For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A, up to the maximum TID level procured.

1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground.
2) Guaranteed by characterization and functionally tested.
3) Capacitance is measured for initial qualification and when design changes may affect the input/output capacitance. Capacitance is measured between the designate terminal and VSS at a frequency of 1MHz and a signal amplitude of 50mV maximum.

14.5 DC Electrical Characteristics - LVCMOS I/O (Pre and Post-Radiation) *

(V_{DD} = 3.3V ± 0.3V; V_{DDC} = 2.5V ± 0.2V) Unless otherwise noted, Tc is per the temperature range ordered.

Symbol	Parameter	Condition	MIN	MAX	Unit
V_{IH} [1]	High-level input voltage		0.7V_{DD}	---	V
V_{IL} [1]	Low-level input voltage		---	0.3V_{DD}	V
V_{OL}	Low-level output voltage	IOL = 8.0mA IOL = 12mA IOL = 100µA	---	0.4 0.4 0.25	V
V_{OH}	High-level output voltage	IOH = -8.0mA IOH = -12mA IOH = -100mA	V_{DD}-0.6 V_{DD}-0.6 V_{DD}-0.25	---	V
I_{CMOSIN}	Input leakage current	V_{IN} = V_{DD} or V_{SS}	-1	1	µA
V_{T-}	$\overline{RST}$ Pin Input Low Threshold		---	1.3	V
V_{T+}	$\overline{RST}$ Pin Input HIGH Threshold		1.65	---	V
V_H	$\overline{RST}$ Pin Hysteresis		0.6	---	V
I_{OS} [3, 4]	Output Short Circuit Current	V_O = V_{DD} and V_{SS}	-100	100	mA
I_{OL12} [5]	Output Current (Sink)	V_{IN} = V_{DD} or V_{SS} V_{OL} = 0.4V TX1_D, TX1_S, TX2_D, TX2_S, TX3_D, TX3_S, TX4_D, TX4_S	---	12	mA
I_{OH12} [5]	Output Current (Source)	V_{IN} = V_{DD} or V_{SS} V_{OH} = V_{DD} - 0.6V TX1_D, TX1_S, TX2_D, TX2_S, TX3_D, TX3_S, TX4_D, TX4_S	-12	---	mA
I_{OL8} [5]	Output Current (Sink)	V_{IN} = V_{DD} or V_{SS} V_{OL} = 0.4V TICK_OUT, RX_DATA[8:0], RX_EMPTY, TX_FULL, AEMTY_FLAG, AFULL_FLAG, TIME_CODE[7:0]	---	8	mA
I_{OH8} [5]	Output Current (Source)	V_{IN} = V_{DD} or V_{SS} V_{OH} = V_{DD} -0.6V TICK_OUT, RX_DATA[8:0], RX_EMPTY, TX_FULL, AEMTY_FLAG, AFULL_FLAG, TIME_CODE[7:0]	-8	---	mA
C_{INCMOS} [6]	Input Capacitance			15	pF
$C_{OUTCMOS}$ [6]	Output Capacitance			15	pF

Notes:

*For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C Per MIL-STD-883 Method 1019, Condition A, up to the maximum TID level procured.

1) Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: V_{IH} = V_{IH} (min) + 20%, - 0%; V_{IL} = V_{IL} (max) + 0%, - 50%, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to V_{IH} (min) and V_{IL} (max).
2) Per MIL-PRF-38535, for current density 5.0E5 amps/cm2, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765 pF/MHz.
3) Supplied as a design limit but not guaranteed or tested.
4) Not more than one output may be shorted at a time for maximum duration of one second.
5) Guaranteed by characterization.
6) Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz and a signal amplitude of 50mV rms maximum.

14.6 DC Electrical Characteristics - Power Supply Operating Characteristics (pre- and post-radiation) *

(V_{DD} = 3.3V ± 0.3V; V_{DDC} = 2.5V ± 0.2V) Unless otherwise noted, Tc is per the temperature ordered.

Symbol	Parameter	Condition		MIN	MAX	Unit
I_{DDCLV1}	Active core power supply current one SpW port Active (LVDS)	V_{DDC} = 2.7V	HOST_CLK = 2.5MHz One TXCLK_IN = 10MHz		60	
			HOST_CLK = 25MHz One TXCLK_IN = 100MHz		480	mA
			HOST_CLK = 50MHz One TXCLK_IN = 200MHz		960	
I_{DDCLV4}	Active core power supply current four SpW ports Active (LVDS)	V_{DDC} = 2.7V	HOST_CLK = 2.5MHz TXCLK_IN[1:4] = 10MHz		75	
			HOST_CLK = 25MHz TXCLK_IN[1:4] = 100MHz		650	mA
			HOST_CLK = 50MHz TXCLK_IN[1:4] = 200MHz		1275	
I_{DDLV1}	Active I/O power supply current one SpW port Active (LVDS)	V_{DD} = 3.6V	HOST_CLK = 2.5MHz One TXCLK_IN = 10MHz		21	
			HOST_CLK = 25MHz One TXCLK_IN = 100MHz		26	mA
			HOST_CLK = 50MHz One TXCLK_IN = 200MHz		29	
I_{DDLV4}	Active I/O power supply current four SpW ports Active (LVDS)	V_{DD} = 3.6V	HOST_CLK = 2.5MHz TXCLK_IN[1:4] = 10MHz		30	
			HOST_CLK = 25MHz TXCLK_IN[1:4] = 100MHz		50	mA
			HOST_CLK = 50MHz TXCLK_IN[1:4] = 200MHz		60	
I_{DDCS}	Standby core power supply current	V_{DDC}=2.7V HOST_CLK=0MHz TXCLK_IN1=0MHz TXCLK_IN2=0MHz TXCLK_IN3=0MHz TXCLK_IN4=0MHz	ROOM/COLD		200	µA
			HOT		12	mA
I_{DDS}	Standby I/O power supply current	V_{DD} = 3.6V HOST_CLK = 0MHz, TXCLK_IN1 = 0MHz,TXCLK2_IN = 0MHz, TXCLK_IN3 = 0MHz, TXCLK_IN4 = 0MHz			20	mA

14.6 DC Electrical Characteristics - Power Supply Operating Characteristics (pre- and post-radiation) * (Continued)

(V_{DD} = 3.3V ± 0.3V; V_{DDC} = 2.5V ± 0.2V) Unless otherwise noted, Tc is per the temperature ordered.

Symbol	Parameter	Condition		MIN	MAX	Unit
I_{DDCCM1}	Active core power supply current one SpW port Active (LVCMOS)	V_{DDC} = 2.7V	HOST_CLK=2.5MHz One TXCLK_IN = 10MHz		60	
			HOST_CLK=25MHz One TXCLK_IN = 100MHz		480	mA
			HOST_CLK=50MHz One TXCLK_IN = 200MHz		960	
I_{DDCCM4}	Active core power supply current four SpW ports Active (LVCMOS)	V_{DDC} = 2.7V	HOST_CLK=2.5MHz TXCLK_IN[1.4] = 10MHz		74	
			HOST_CLK=25MHz TXCLK_IN[1.4] = 100MHz		650	mA
			HOST_CLK=50MHz TXCLK_IN[1.4] = 200MHz		1275	
I_{DDCM1}	Active I/O power supply current one SpW port Active (LVCMOS)	V_{DD} = 3.6V	HOST_CLK=2.5MHz One TXCLK_IN = 10MHz		20	
			HOST_CLK=25MHz One TXCLK_IN = 100MHz		35	mA
			HOST_CLK=50MHz One TXCLK_IN = 200MHz		45	
I_{DDCM4}	Active I/O power supply current four SpW ports Active (LVCMOS)	V_{DD} = 3.6V	HOST_CLK=2.5MHz TXCLK_IN[1.4] = 10MHz		22	
			HOST_CLK=25MHz TXCLK_IN[1.4] = 100MHz		60	mA
			HOST_CLK=50MHz TXCLK_IN[1.4] = 200MHz		110	

* For devices procured with total ionizing dose tolerance guarantee, the post-radiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

14.7 AC Electrical Characteristics - Power Sequencing and Reset *

(V_{DD} = 3.3V ± 0.3V; V_{DDC} = 2.5V ± 0.2V) Unless otherwise noted, Tc is per the temperature ordered.

Symbol	Parameter	Condition	MIN	MAX	Unit
t_{VCD} [1]	V_{DD} valid to V_{DDC} delay	V_{DD}> 3.0V; V_{DDC}> 2.25V	0	-	ns
t_{DRST} [1]	Minimum number of full clock cycles (HOST_CLK) between Rising Edge of $\overline{RST}$ and inputs valid	-	3	-	HOST_CLK
t_{CRST} [1]	Minimum number of full clock cycles (HOST_CLK) that $\overline{RST}$ must remain low before $\overline{RST}$ can transition high	-	6	-	HOST_CLK

Note:

* For devices procured with total ionizing dose tolerance guarantee, the post-radiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1) Guaranteed by design.

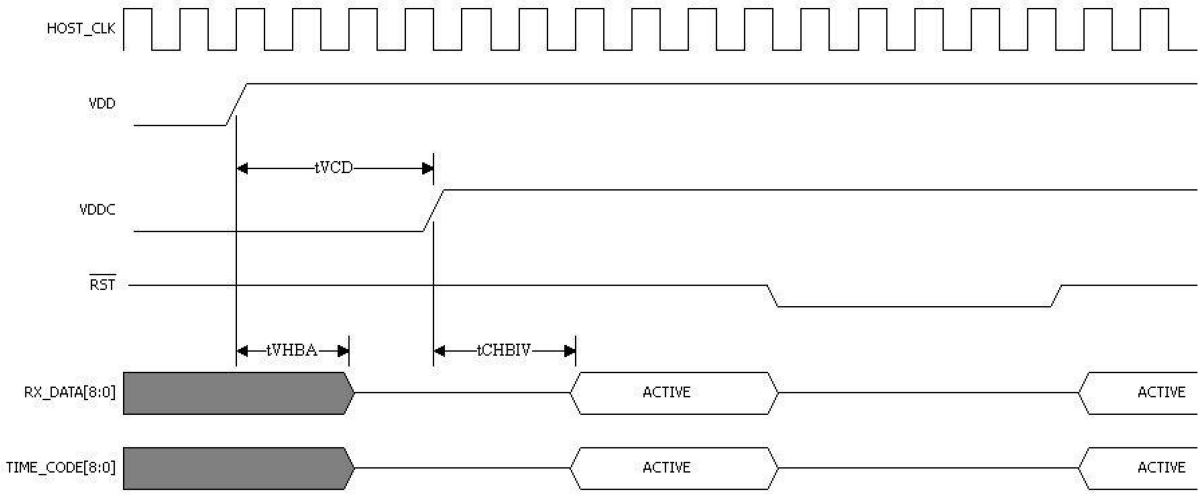


Figure 18. Power Sequencing and Reset Timing Diagram

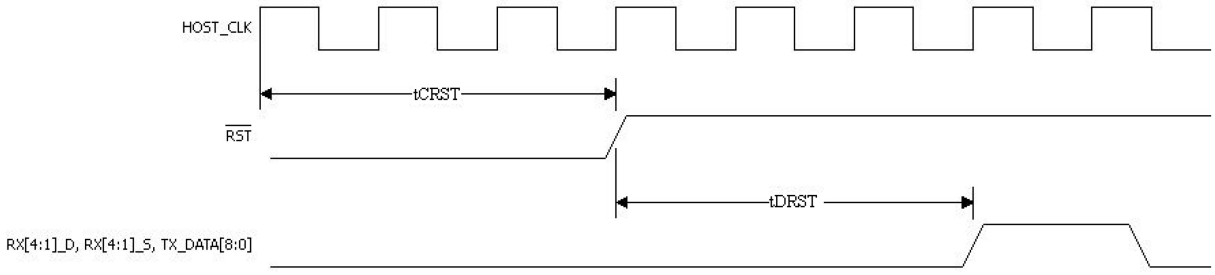


Figure 19. Reset Timing Diagram

14.8 AC Electrical Characteristics - LVDS Transmit Port [1,2] *

(V_{DD} = 3.3V ± 0.3V; V_{DDC} = 2.5V ± 0.2V) Unless otherwise noted, Tc is per the temperature ordered

Symbol	Parameter	MIN	MAX	Unit
t_{SKDD}	Differential Skew	---	500	ps
t_{RISED} [4]	Rise Time	---	2.2	ns
t_{FALLD} [4]	Fall Time	---	2.2	ns
$t_{DSSKEWLV}$	LVDS Data/Strobe Output Skew (Per Port)	---	1	ns

Notes:
*For devices procured with total ionizing dose tolerance guarantee, the post-radiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1) Generator waveform for all tests unless otherwise specified: f =1 MHz, Zo = 50, tr< 1ns, and tf< 1ns.
2) CL includes probe and jig capacitance.
3) Guaranteed by characterization.
4) Guaranteed by design.

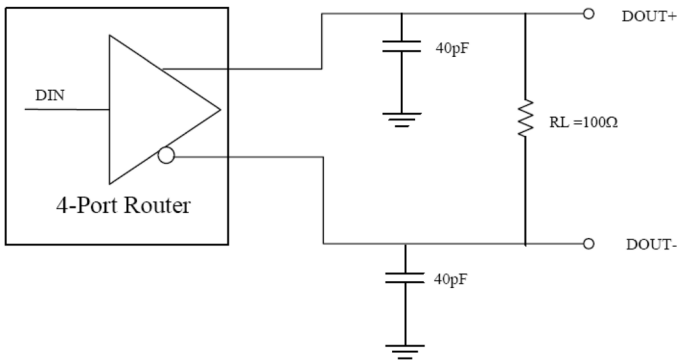


Figure 20. LVDS Driver Differential Skew, Rise and Fall Time Test Circuit

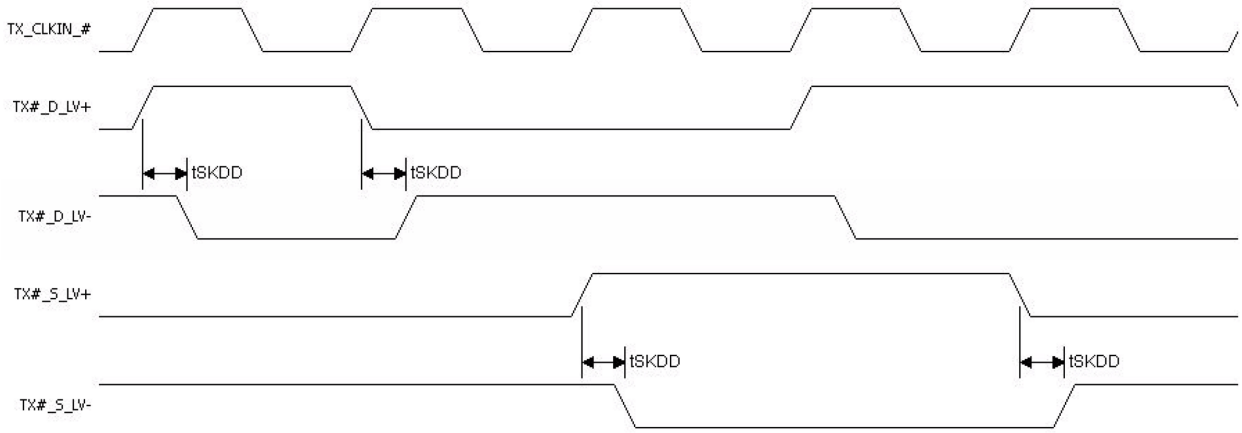


Figure 21. LVDS Driver tSKDD Timing Diagram

The LVDS Data Strobe Output Skew is between each signal in the differential signaling pair.

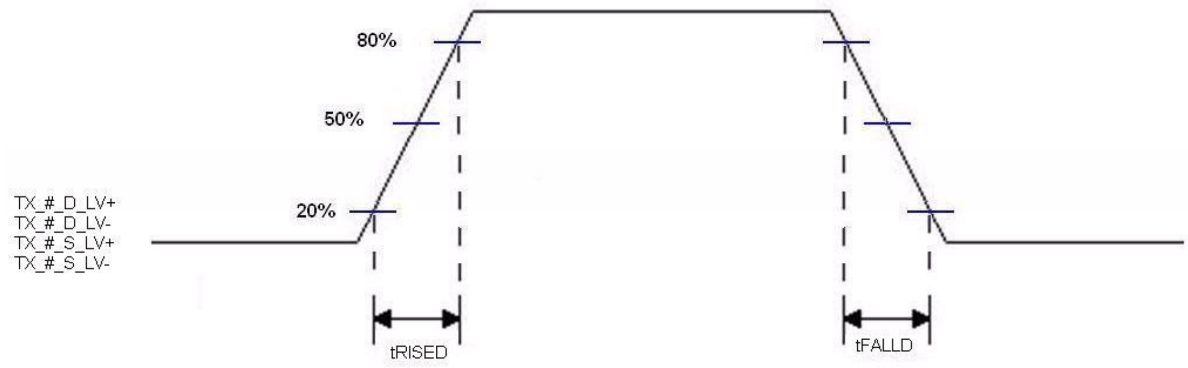


Figure 22. LVDS Driver Rise and Fall Timing Diagram

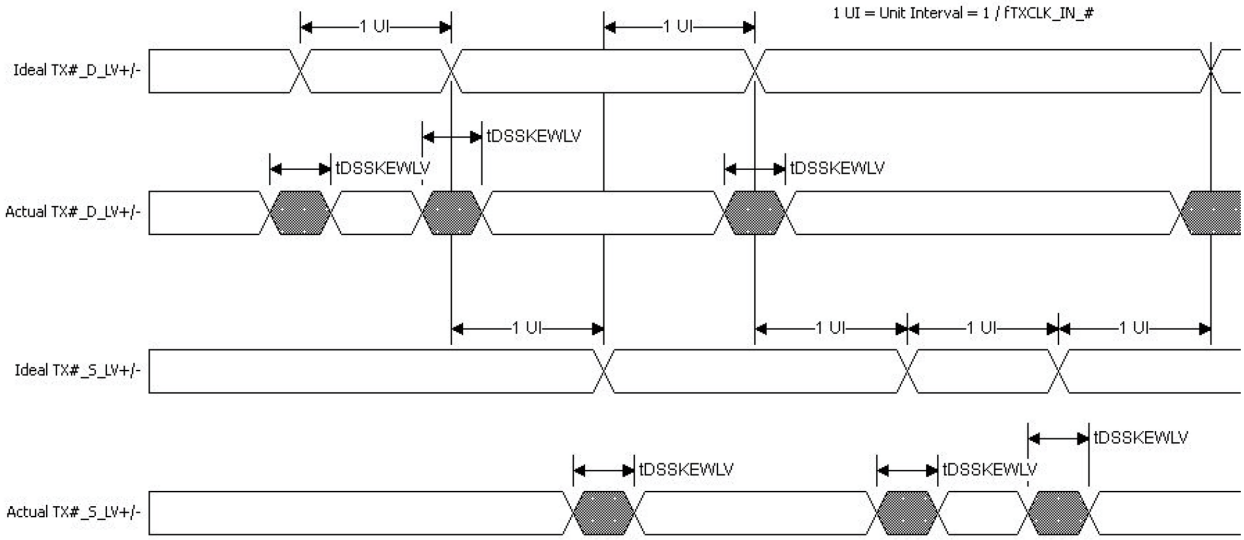


Figure 23. LVDS Driver Data/Strobe Output Skew

14.9 AC Electrical Characteristics - LVDS Receiver Port [1, 2] *

(V_{DD} = 3.3V ± 0.3V; V_{DDC} = 2.5V ± 0.2V) Unless otherwise noted, Tc is per the temperature ordered.

Symbol	Parameter	MIN	MAX	Unit
t_{DSSEP}	Minimum Data/Strobe Separation (Per Port)	3.5	---	ns

Notes:

*For devices procured with total ionizing dose tolerance guarantee, the post-radiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1) Generator waveform for all tests unless otherwise specified: f =1 MHz, Zo = 50, tr< 1ns, and tf< 1ns.
2) CL includes probe and jig capacitance.

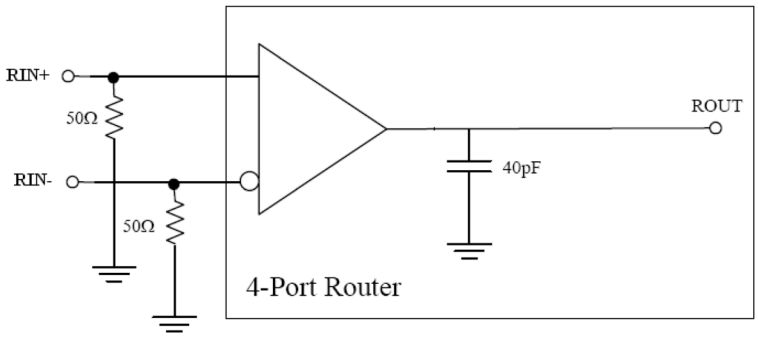


Figure 24. LVDS Receiver Equivalent Test Circuit

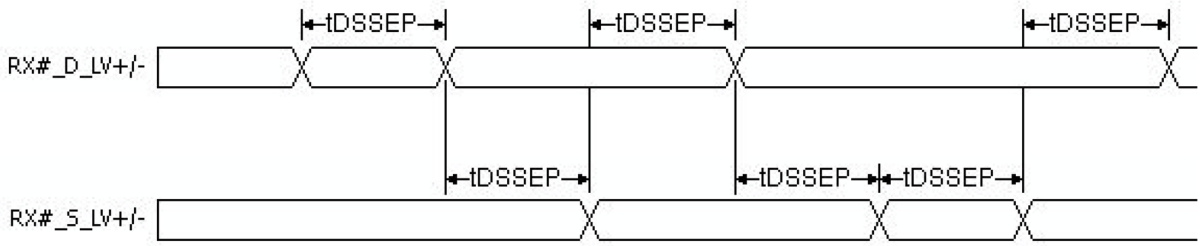


Figure 25. LVDS Receive Port Minimum Data/Strobe Separation

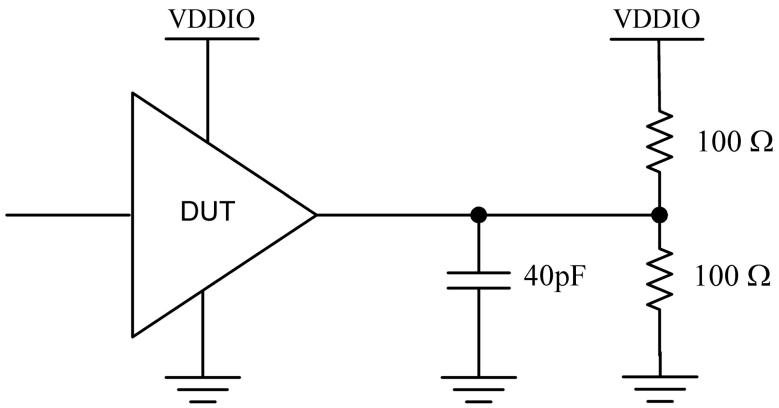


Figure 26. CMOS Equivalent Test Load

14.10 AC Electrical Characteristics - LVCMOS SpW Transmit Port *

(V_{DD} = 3.3V ± 0.3V; V_{DDC} = 2.5V ± 0.2V) Unless otherwise noted, Tc is per the temperature ordered.

Symbol	Parameter	MIN	MAX	Unit
$t_{DSSKEWCM}$	Data/Strobe Output Skew (Per Port)	---	1.5	ns
t_{TLHCM} [1]	LVCMOS SPW Transmit Output Rise Time	---	2.4	ns
t_{THLCM} [1]	LVCMOS SPW Transmit Output Fall Time	---	1.3	ns

Note:

*For devices procured with total ionizing dose tolerance guarantee, the post-radiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1) Guaranteed by design.

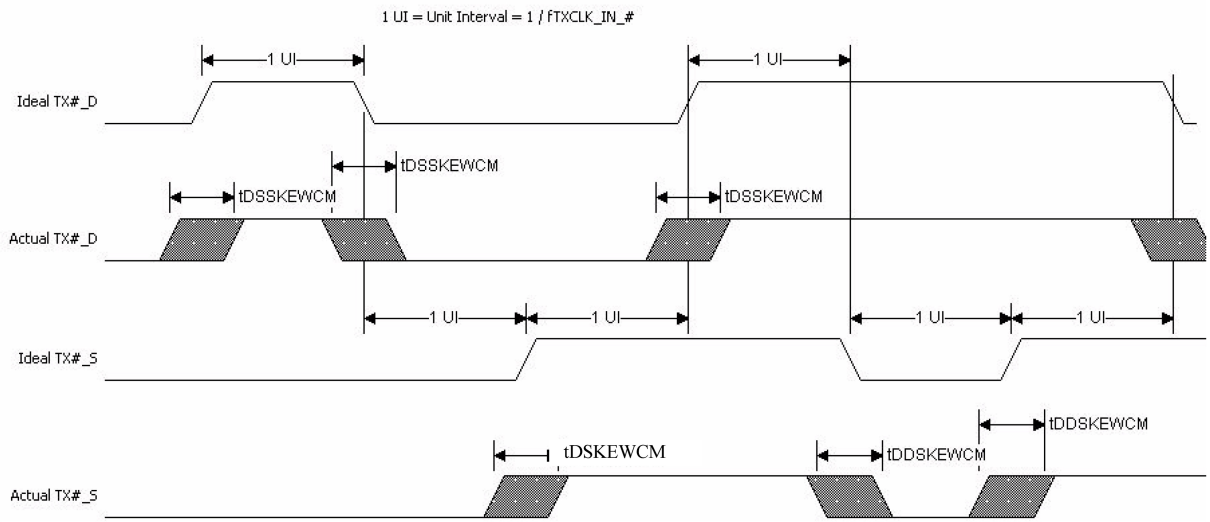


Figure 27. LVCMOS Transmit Port Data/Strobe Output Skew

14.11 AC Electrical Characteristics – LVCMOS SpW Receive Port *

(V_{DD} = 3.3V + 0.3V; V_{DDC} = 2.5V + 0.2V) Unless otherwise noted, Tc is per the temperature ordered.

Symbol	Parameter	MIN	MAX	Unit
$t_{DSSEPCM}$	Minimum Data/Strobe Separation (Per Port)	3.5		ns

Note:

*For devices procured with total ionizing dose tolerance guarantee, the post-radiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

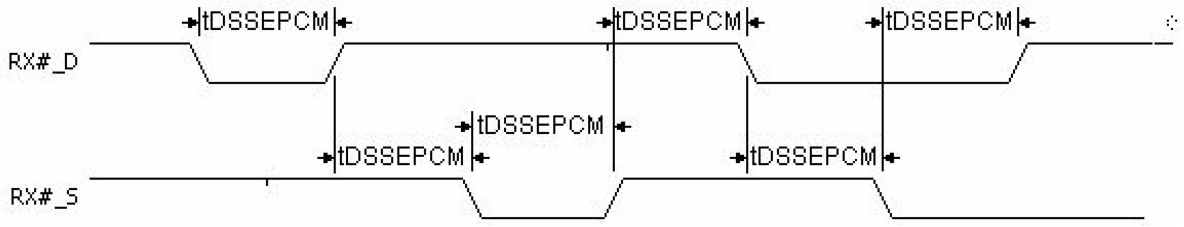


Figure 28. LVCMOS Receive Port Minimum Data/Strobe Separation

14.12 AC Electrical Characteristics - Host Clock and SpW Input Clocks *

(V_{DD} = 3.3V ± 0.3V; V_{DDC} = 2.5V ± 0.2V) Unless otherwise noted, Tc is per the temperature ordered.

Symbol	Parameter	MIN	MAX	Unit
f_{HOST} [1]	HOST_CLK frequency	2.5	50	MHz
$f_{TXCLKIN}$	SpaceWire ports Input clock frequencies TXCLK_IN_1, TXCLK_IN_2, TXCLK_IN_3, and TXCLK_IN_4	10	200	MHz

Note:

* For devices procured with total ionizing dose tolerance guarantee, the post-radiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1) HOST_CLK must run at 0.25X the fastest TXCLK_IN frequency.

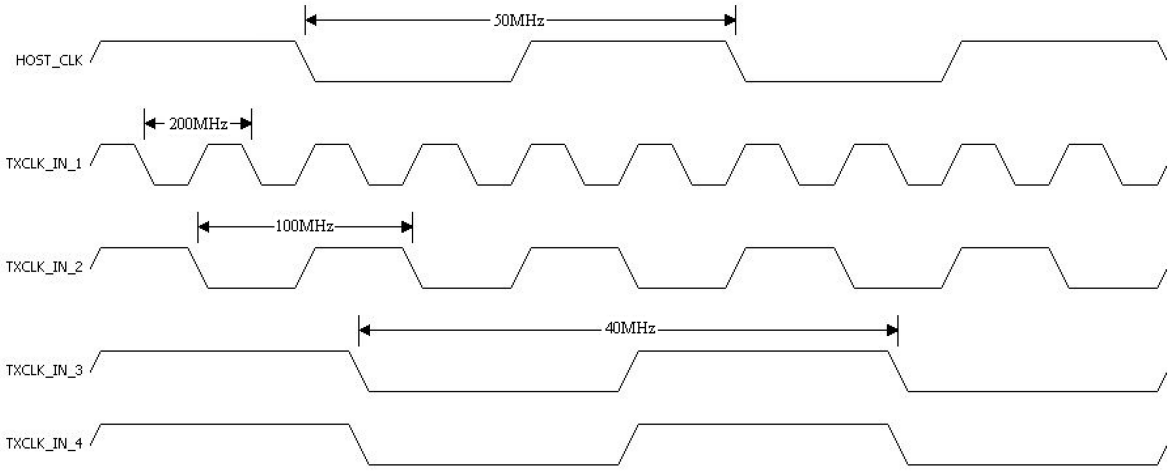


Figure 29. HOST_CLK max TXCLK_IN requirements

14.13 AC Electrical Characteristics - Time Code Interface *

(V_{DD} = 3.3V ± 0.3V; V_{DDC} = 2.5V ± 0.2V) Unless otherwise noted, Tc is per the temperature ordered.

Symbol	Parameter	MIN	MAX	Unit
t_{TCDS} [2]	Time Code Data Setup time to HOST_CLK Rising Edge and TICK_IN High	2	---	ns
t_{TCDH} [2]	Time Code Data Hold time from HOST_CLK Rising Edge and TICK_IN High	0	---	ns
t_{TIS}	TICK_IN Setup time to HOST_CLK Rising Edge and TIME_CODE Valid	2.5	---	ns
t_{TIH}	TICK_IN Hold time from HOST_CLK Rising Edge and TIME_CODE Valid	0	---	ns
t_{TCV} [2]	Time from HOST_CLK Rising Edge to TIME_CODE Transition	5.75[3]	15	ns
t_{THVH}	Time from HOST_CLK Rising Edge to TICK_OUT High	3	15	ns
t_{THVL}	Time from HOST_CLK Rising Edge to TICK_OUT Low	3	15	ns
t_{TOHL} [1, 2]	TICK_OUT High to Low (HOST_CLK)	---	1.5	ns
t_{TOLH} [1, 2]	TICK_OUT Low to High (HOST_CLK)	---	1.5	ns

Notes:

*For devices procured with total ionizing dose tolerance guarantee, the post-radiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1) Guaranteed by design.
2) Time code signals Time-Code6 and Time-Code7 are excluded.
3) Guaranteed by characterization.

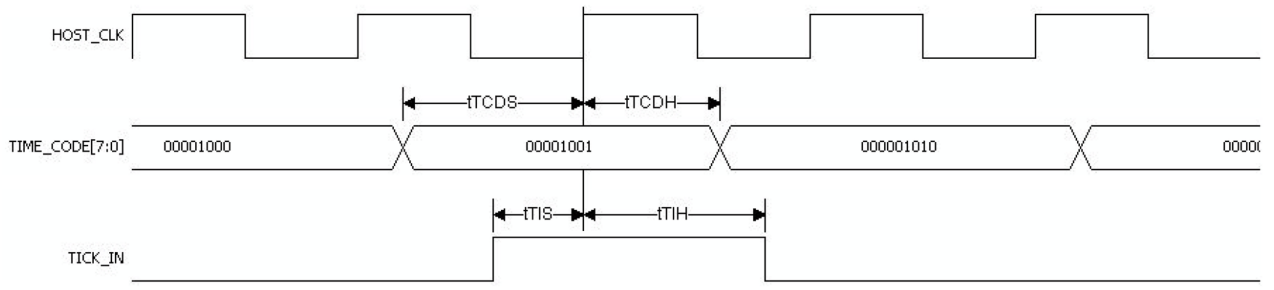


Figure 30. TICK_IN

The TICK_IN signal requests the transmission of a time code. The 8-bit TIME_CODE port sends the time code value. When the router is in the Run state and TICK_IN is asserted, the router will send a time-code immediately after the character currently being transmitted has finished.

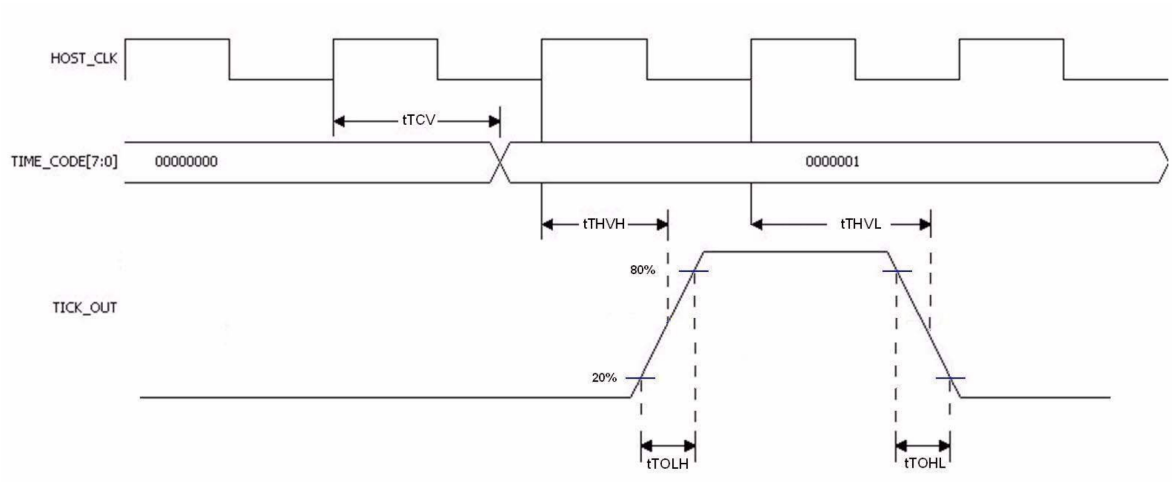


Figure 31. TICK_OUT Interface

TICK_OUT signals that a time code has arrived at a SpaceWire interface. TICK_OUT is asserted whenever the link interface is in the Run state and the receiver receives a valid time code. The 8-bit time code port TIME_CODE[7:0] will reflect the current value of the time code. A valid time code is a time code that is one more than the current value of the router's time-counter.

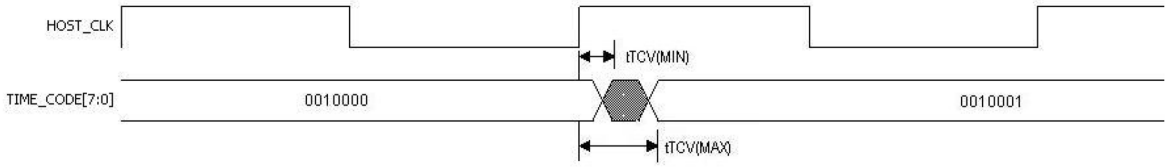


Figure 32. HOST_CLK to TIME_CODE Transition

14.14 AC Electrical Characteristics - Transmit FIFO *

(V_{DD} = 3.3V ± 0.3V; V_{DDC} = 2.5V ± 0.2V) Unless otherwise noted, Tc is per the temperature ordered.

Symbol	Parameter	MIN	MAX	Unit
t_{TXS}	Transmit Data Setup time to HOST_CLK Rising Edge ($\overline{TX\_PUSH}$ and $\overline{CSEL}$ Valid Low)	3	---	ns
t_{TXH}	Transmit Data Hold time from HOST_CLK Rising Edge ($\overline{TX\_PUSH}$ and $\overline{CSEL}$ Valid Low)	0	---	ns
$t_{TXPUSHS}$	Transmit PUSH Setup time to HOST_CLK Rising Edge and $\overline{CSEL}$ Low	6	---	ns
$t_{TXPUSHH}$	Transmit PUSH Hold time from HOST_CLK Rising Edge and $\overline{CSEL}$ Low	0	---	ns
$t_{CSPUSHS}$	Chip Select Setup time to HOST_CLK Rising Edge and $\overline{TX\_PUSH}$ Low	12	---	ns
$t_{CSPUSHH}$	Chip Select Hold time from HOST_CLK Rising Edge and $\overline{TX\_PUSH}$ Low	0	---	ns
$t_{ALM2FULL}$[1]	Almost Full to Full flag	8	---	# PUSHES
t_{TXAF}	Time from last Transmit PUSH to TX_AFULL	---	9.5	ns
t_{TXF}	Time from last Transmit Push to TX_FULL	---	9.5	ns

Notes:

*For devices procured with total ionizing dose tolerance guarantee, the post-radiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1) Guaranteed by design.

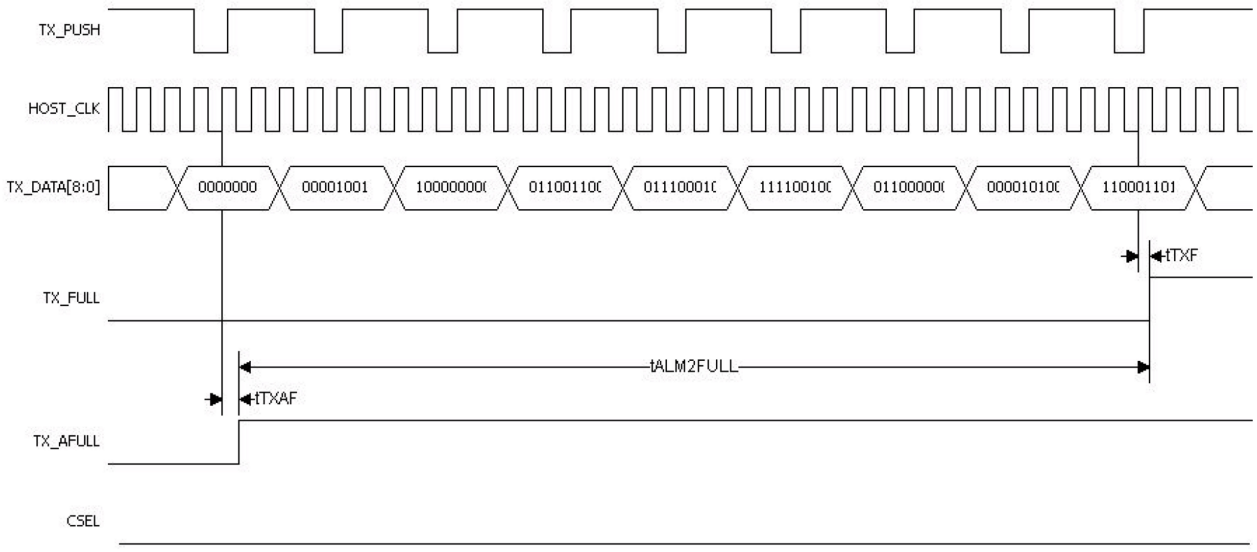


Figure 33. Transmit FIFO Almost Full Flag

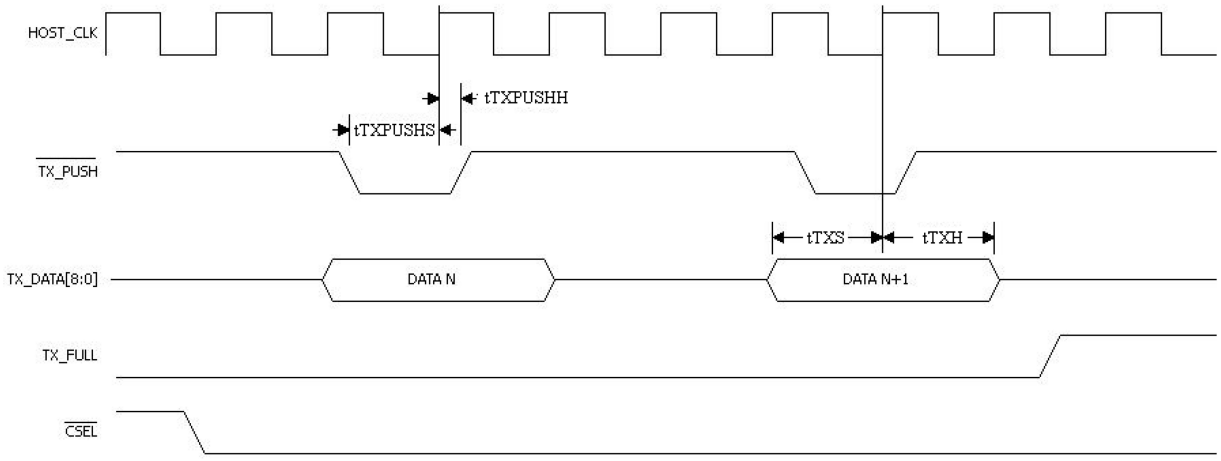


Figure 34. Transmit Port PUSH

Note:

1) This figure is for illustrative purposes. Max throughput on system port is 200Mbps.

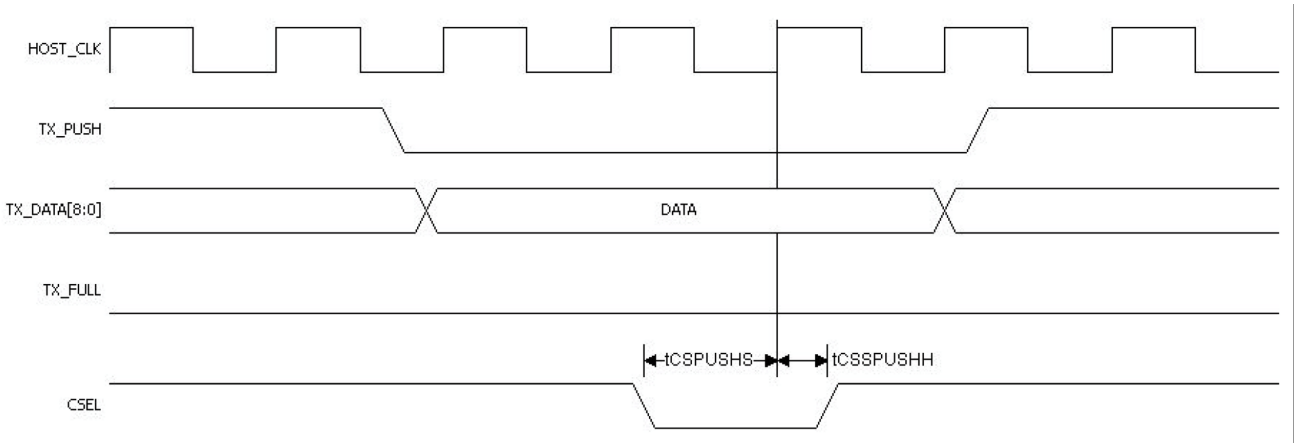


Figure 35. Transmit Port PUSH with Chip Select Transition

14.15 AC Electrical Characteristics - Receive FIFO *

(V_{DD} = 3.3V ± 0.3V; V_{DDC} = 2.5V ± 0.2V) Unless otherwise noted, Tc is per the temperature ordered.

Symbol	Parameter	MIN	MAX	Unit
t_{RXH}	Receive Data Transition time from HOST_CLK Rising Edge ($\overline{RX\_POP}$ and $\overline{CSEL}$ Valid Low)	3	12.25[2]	ns
t_{RXPOPS}	Receive POP Setup time to HOST_CLKRising Edge and $\overline{CSEL}$ Low	3	---	ns
t_{RXPOPH}	Receive POP Hold time from HOST_CLK Rising Edge and $\overline{CSEL}$ Low	0	---	ns
t_{CSPOPS}	Chip Select Setup time to HOST_CLK Rising Edge and $\overline{RX\_POP}$ Low	13	---	ns
t_{CSPOPH}	Chip Select Hold time from HOST_CLK Rising Edge and $\overline{RX\_POP}$ Low	0	---	ns
$t_{ALM2EMY}$ [1]	Almost Empty flag to Empty flag	8	---	# POPS
t_{RXAE}	Time from last Receive data POP to RX_AEMPTY	---	9.5	ns
t_{RXE}	Time from last Receive data POP to RX_EMPTY High	---	9.5	ns

Notes:

*For devices procured with total ionizing dose tolerance guarantee, the post-radiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

1) Guaranteed by design.
2) Guaranteed by characterization.

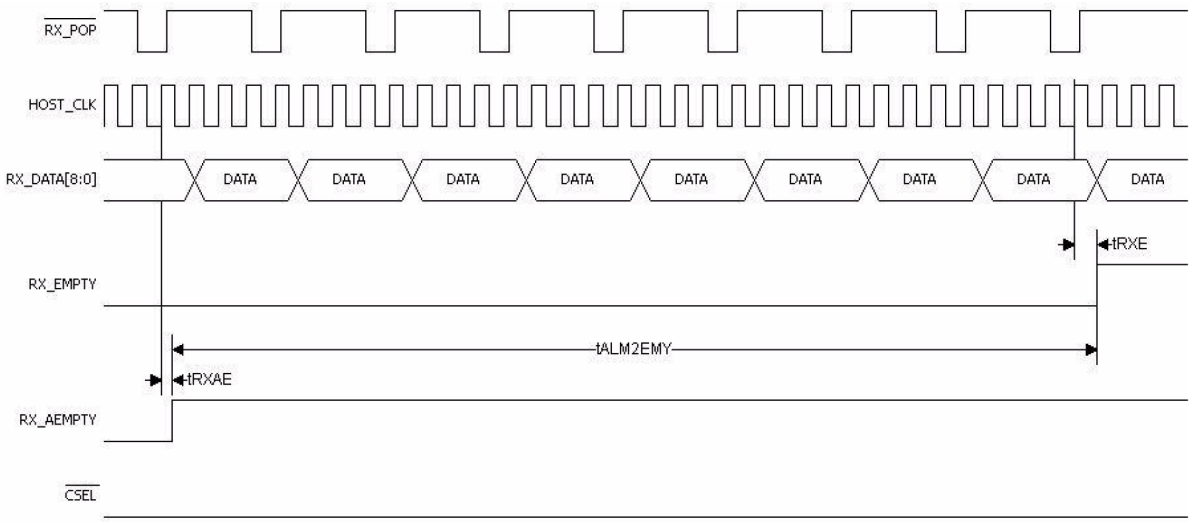


Figure 37. Receive FIFO Almost Empty Flag

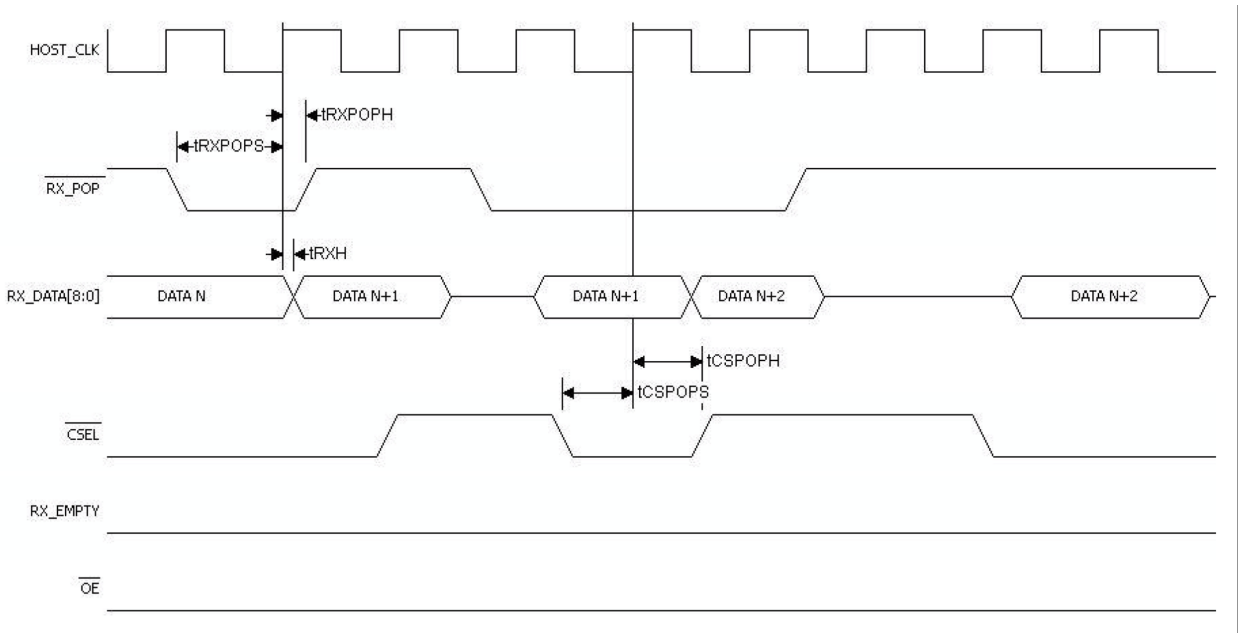


Figure 37. Receive Port POP

System port read timing specification, reading data out of System Port FIFO

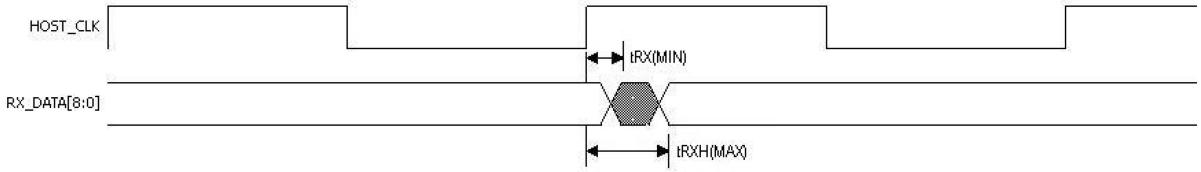


Figure 38. HOST_CLK to RX_DATA Transition

14.16 AC Electrical Characteristics - Control Inputs and Reset *

(V_{DD} = 3.3V + 0.3V; V_{DDC} = 2.5V + 0.2V) Unless otherwise noted, Tc is per the temperature ordered.

Symbol	Parameter	MIN	MAX	Unit
t_{RXOE}	Time from $\overline{OE}$ Low to valid Output Data (See Table 16)	---	10	ns
t_{RXCS}	Time from $\overline{CSEL}$ Low to valid Output Data (See Table 16)	---	10	ns
t_{RXOEZ}	Time from $\overline{OE}$ High to Tri-state (See Table 16)	---	10	ns
t_{RXCSZ}	Time from $\overline{CSEL}$ High to Tri-state (See Table 16)	---	10	ns

Note:
*For devices procured with total ionizing dose tolerance guarantee, the post-radiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured.

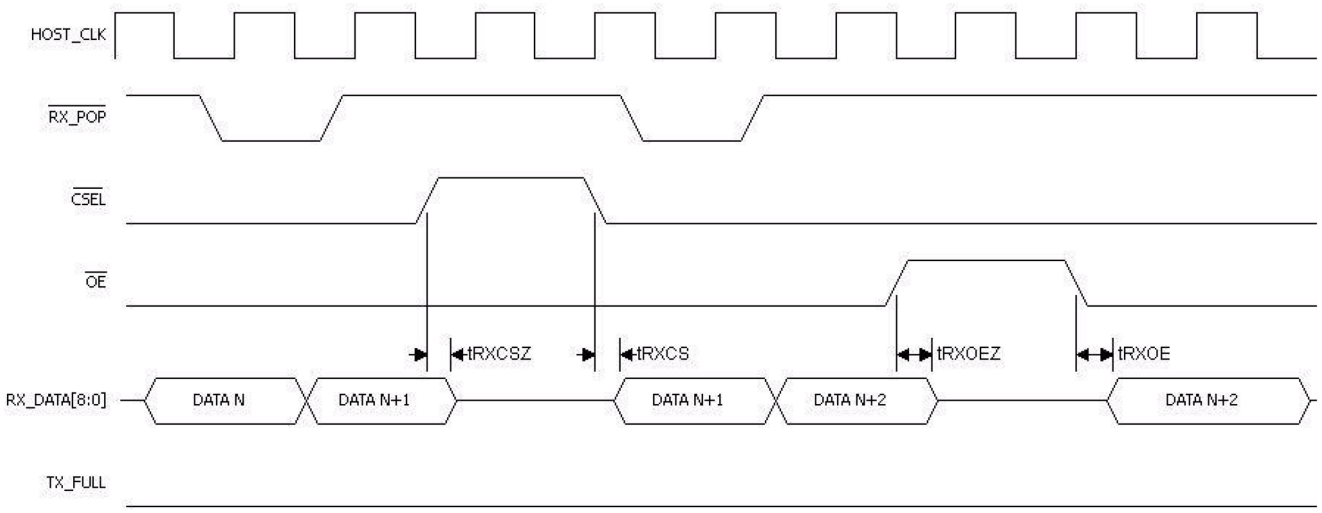


Figure 39. Control Inputs Timing Information

15.0 Packaging

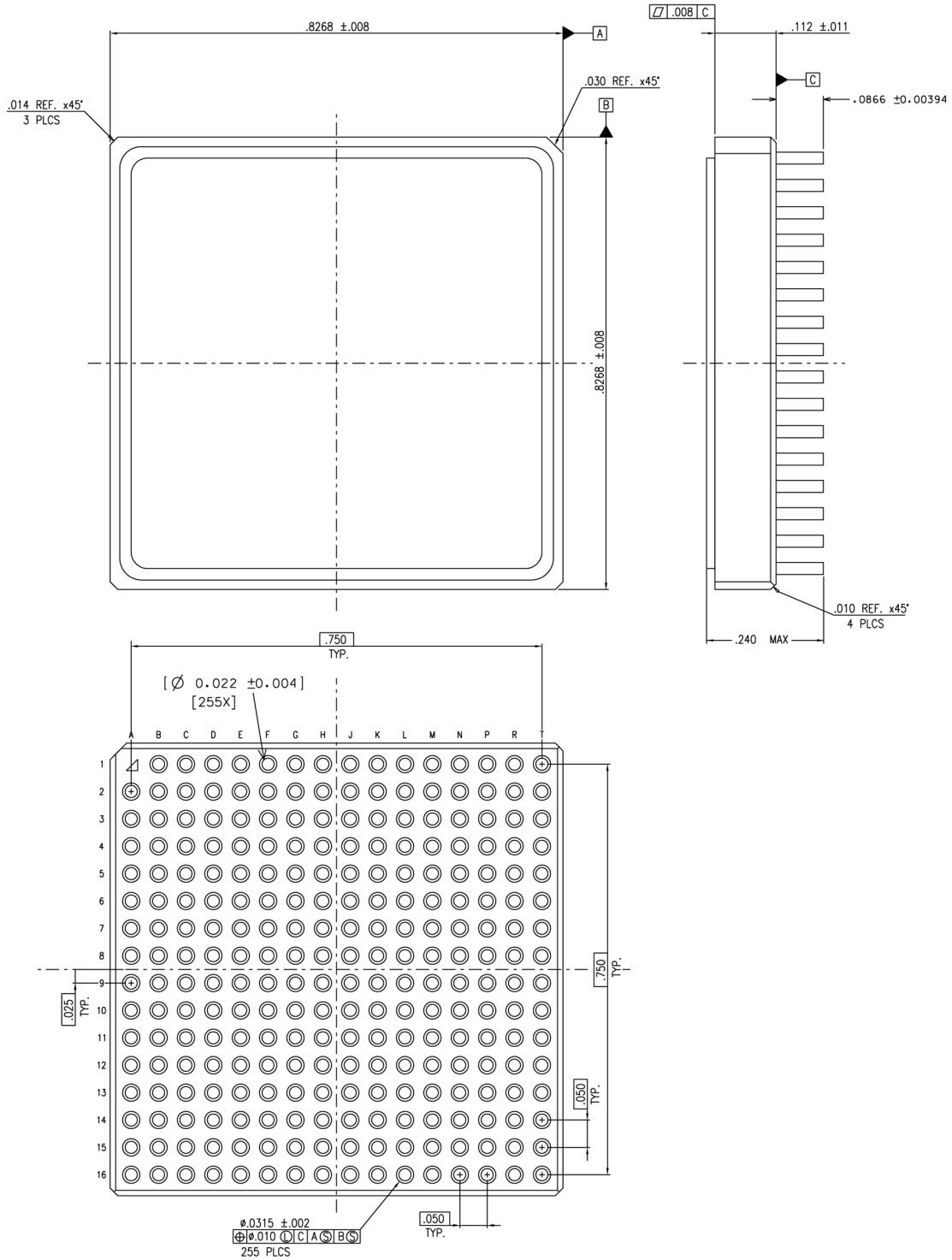


Figure 40. 255-CCGA

Notes:

1) Lid is connected to VSS
2) Units are in inches.

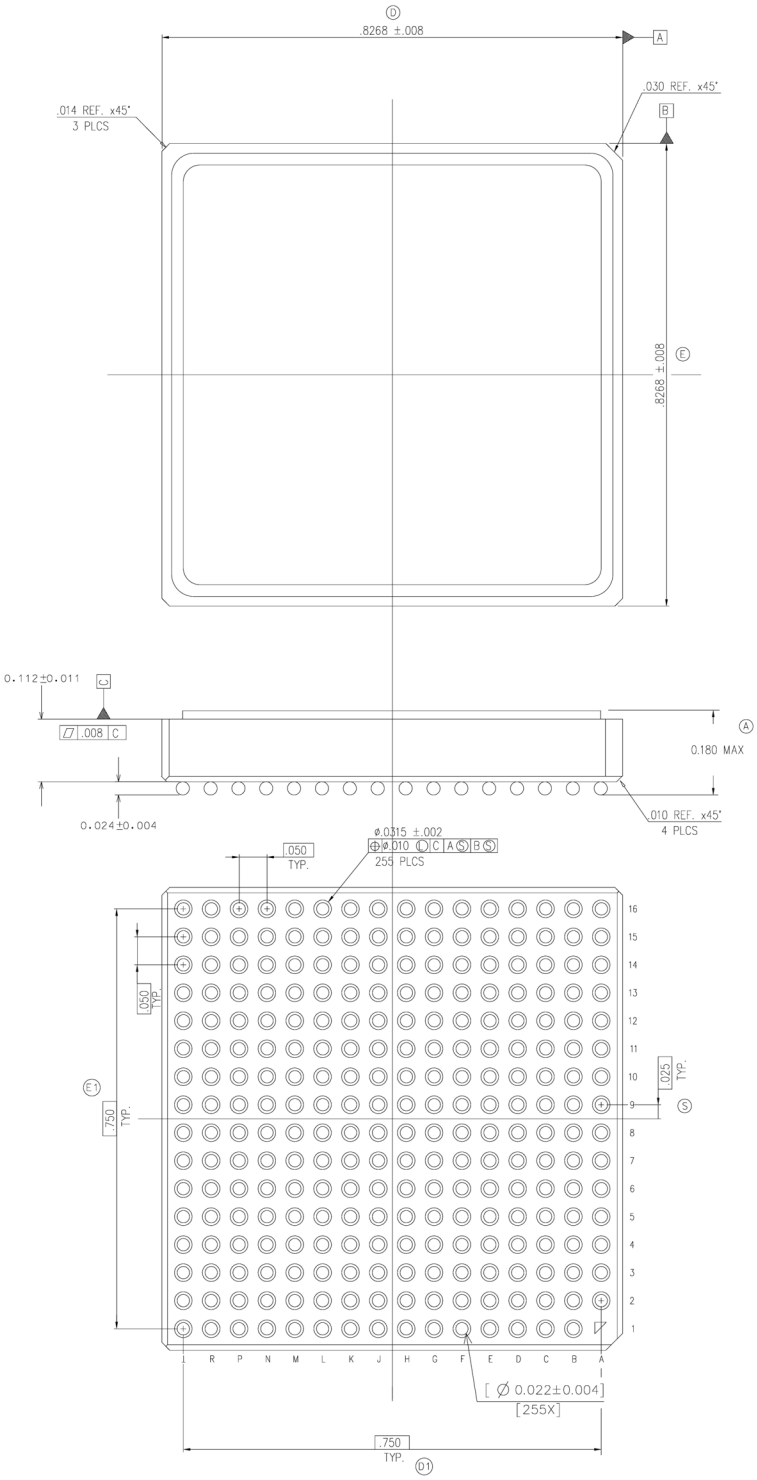


Figure 41. 255-CBGA

Notes:

1) Lid is connected to VSS
2) Units are in inches.

4-Port SpaceWire Router

UT200SpW4RTR

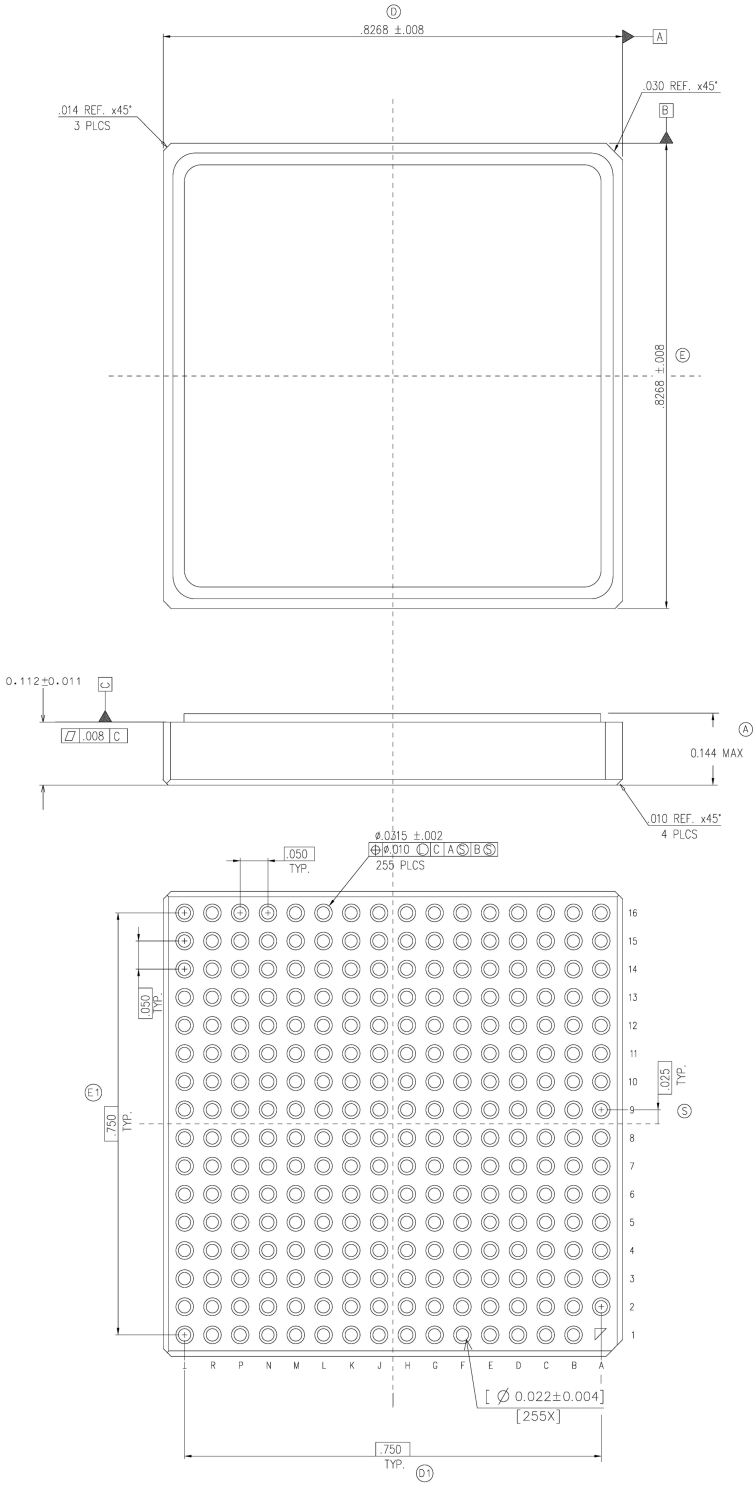


Figure 42. 255-CLGA

Notes:

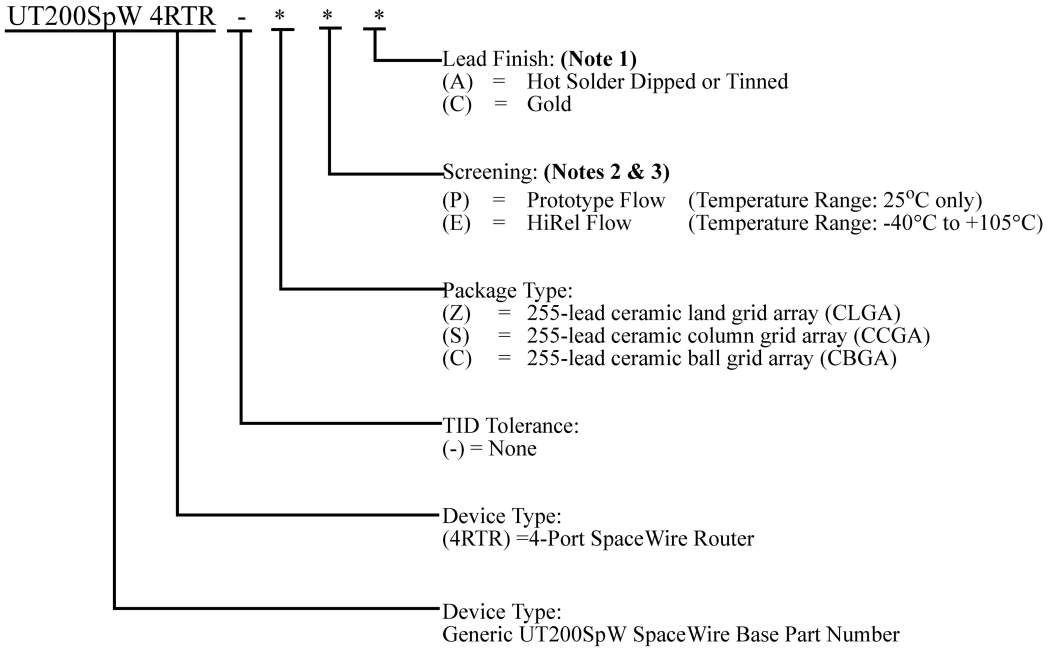
1) Lid is connected to VSS
2) Units are in inches.

4-Port SpaceWire Router

UT200SpW4RTR

Ordering Information

UT200SpW4RTR 4-Port SpaceWire Router:



Notes:

1) Lead finish (A or C) must be specified according to the table below.
2) Prototype flow per CAES Colorado Springs Manufacturing Flows Document. Tested at 25°C only. Radiation neither tested nor guaranteed.
3) HiRel Flow per CAES Colorado Springs Manufacturing Flows Document. Radiation neither tested nor guaranteed.

Package Option	Associated Lead Finish
(Z) 255 CLGA	(C) Gold
(S) 255 CCGA	(A) Hot Solder Dipped
(C) 255 CBGA	(A) Hot Solder Dipped

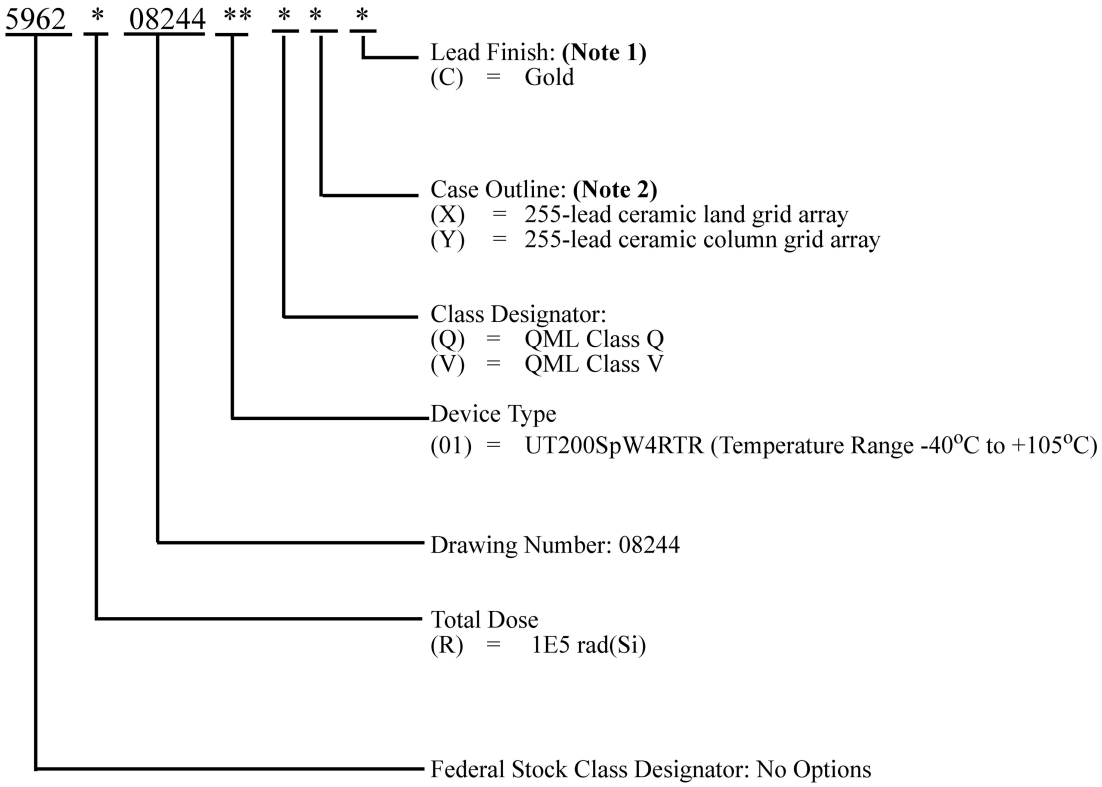
DATASHEET

RELEASED 4/08/13

4-Port SpaceWire Router

UT200SpW4RTR

4-Port SpaceWire Router: SMD



Notes:

1) Lead finish is "C" (gold) only.
2) Using an Altered Item Drawing (AID), CAES offers Column Attachment as an additional service for the Ceramic Land Grid Array (Case outline X). If needed, please ask for COLUMN ATTACHMENT when submitting your request for quotation.

DATASHEET

RELEASED 4/08/13

4-Port SpaceWire Router

UT200SpW4RTR

Datasheet Definitions

	DEFINITION
Advanced Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet **is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final**.
Preliminary Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

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