FRONTGRADE

DATASHEET

UT16MX116/117

Analog Multiplexer

2/1/2019

Version #: 1.0.0

Features

- 16-to-1 Analog Mux
- 100Ω Signal paths (typical)
- 5V single analog supply
- Rail-to-Rail signal handling
- Asynchronous $\overline{\text{RESET}}$ input
- SPI™/QSPI™ and MICROWIRE™ compatible serial interface (UT16MX117)
- Asynchronous parallel input Interface (UT16MX116)
- LVCMOS or CMOS compatible inputs (set by voltage of V_{DD_IO} pin)
- 2kV ESD Protection (per MIL-STD-883, Method 3015.7)
- Operational environment:
- Total ionizing dose: 300 krad(Si)
  — SEL immune to a LET of 110 MeV-cm²/mg
  — SEU immune to a LET of 62.3 MeV-cm²/mg
- Packaging: 28-lead Ceramic Flatpack
- Standard Microcircuit Drawing 5962-10237
- QML Q, QML V

Introduction

The UT16MX116/117 are low voltage analog multiplexers with a convenient LVCMOS (3.3V) or CMOS digital interface set by the voltage level of the V_{DD_IO} pin. The analog muxes have Break-Before-Make architecture with a low channel resistance. The muxes support rail-to-rail input signal levels. The multiplexer supports serial (SPI™), or asynchronous parallel interface.

The UT16MX116/117 operates with a single 5V (±10%) analog power supply. An external 3.3V digital voltage supply is required, for the digital circuitry. The digital I/O supply may be set to 3.3V ± 10% or 5V± 10% by the V_{DD_IO} pin.

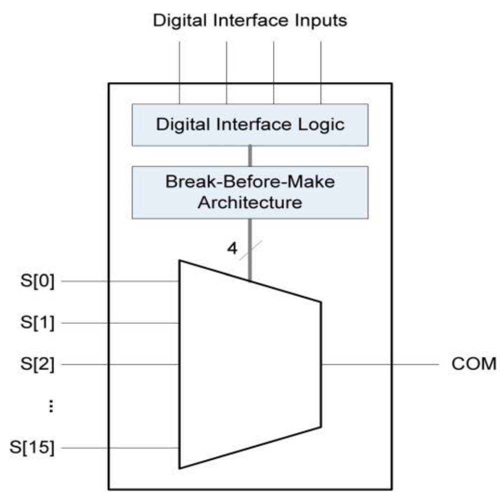

Figure 1: UT16MX116/117 Block Diagram

Functional Description

All mux decoding (whether for the UT16MX116 or UT16MX117 device) operation utilizes a Break-Before-Make process to prevent shorting between analog data inputs during address transitions.

UT16MX116:

The UT16MX116 utilizes a parallel interface which operates in asynchronous mode much like discrete logic switches. The *UT16MX116 requires the following operation in order to properly initialize the part following power-up: All address states for the A[3:0] address lines must be exercised following AVDD power-up to ensure correct addressing. Once this operation has been completed, normal asynchronous addressing can then be used to select the desired input channel (i.e. one of S[15:0]) to connect to the COM output. The S[15:0] analog channels are routed asynchronously via the binary decoding of A[3:0] static logic levels after initialization.* During operation, the connection between COM and the S[15:0] pins are steered, asynchronously, based on the binary decoding of the A[3:0] static logic levels. The address pins A[3:0] are required to hold static levels for proper mux operation. Any change in A[3:0] pins directs the COM connection to the appropriate S[x] input after approximately 100ns propagation delay (including the Break- Before-Make delay). All bits (A[3:0]) of any address change should be received by the UT16MX116 within 18 ns of the first bit change for proper operation. The asynchronous parallel interface mode requires $\overline{CS}$ to be low for accepting a change on the address pins A[3:0]. When $\overline{CS}$ is high, the UT16MX116 disables the address pins A[3:0], as well as holding the last valid address state, thereby mitigating against any single-event upsets or transients on the address bus.

UT16MX117:

The UT16MX117 utilizes a serial interface that supports the standard that is compatible with MICROWIRE™, SPI™, and QSPI™. The UT16MX117 SPI™ interface can be depicted as an 8-bit serial shift register controlled by $\overline{SS}$, clocked by the rising edge of SCLK. The 8-bit shift register is for compatibility purposes, even though this UT16MX117 serial address setting requires only 4 bits. The four LSB of the 8-bit shift register are the four bits decoding the mux address. When shifting data into the part, the MSB enters the part first. The four MSB may be set to zeroes, e.g., the 8-bit command "00001001" would set the mux to connect COM to S[9].The UT16MX117 is considered a slave SPI™ device with MOSI (Master Out Slave In) as the data input pin to the device. The data is shifted with D7 as the first bit into the shift register, and also the first bit out to the MISO (Master In Slave Out) output pin after eight clock cycles of SCLK. The signal on the $\overline{SS}$ pin defines the window when the address bits are shifted into the device. This occurs when signal on $\overline{SS}$ is low. Only when $\overline{SS}$ is high at the close of the shifting window, does the mux decoding get updated and COM is directed to the decoded S[x] input (after Break-Before-Make delay).

SPI™ Operations:

The SPI™ (Serial Peripheral Interface) is implemented as a synchronous 8-bit serial shift register controlled by four pins: MOSI, MISO, SCLK, and $\overline{SS}$. This is compatible with the SPI™/QSPI™ standard as defined by Motorola on the MC68HCxx line of microcontrollers. This SPI™ also conforms to the MICROWIRE™ interface, an SPI™ subset interface, as defined by National Semiconductor.

The UT16MX117 SPI™ is always a slave device, where MOSI, SCLK, and $\overline{SS}$ are controlled by a master device. MISO output is used as receiving slave data or to daisy chain several SPI™ devices in appropriate applications.

The MUX select functionality is controlled by the four LSB of the 8-bit SPI™ shift registers. When shifting, the first SCLK rising edge clocks in the MSB first. The first falling edge of the SCLK clocks out the 6th bit of the current values in the SPI™ registers, since the 7th bit already appears at the MISO at the start of a serial transmission before the first SCLK (Figures 5 and 6).

RESET Function (UT16MX117 Only):

The $\overline{RESET}$ pin is used to reset all internal logic circuits. $\overline{RESET}$ held low also keeps all COM and S[15:0] analog I/Os in a high impedance state. This is the recommended condition at system power-up.

Asserting $\overline{RESET}$ (active low) resets all of the internal address decoding registers to 0, thus steering the COM to connect to S[0] while in the high impedance state. When $\overline{RESET}$ is de-asserted (high), both COM and S[0] will come out of the high impedance state and COM will be driven by S[0].

Table 1: UT16MX116 Pin Description

Pin No.	Name	I/O	Type	Description
1	AV_{DD}	—	Power	Analog Positive Supply[1]
2	NC	—	—	No Connection
3	V_{DD_IO}	—	Power	Digital I/O Supply[1]
4-11	S[15:8]	Input	Analog	Muxed Inputs
12	GND	—	Power	Digital Ground
13	V_{DD}	—	Power	Digital Core Supply[1]
14	A3	Input	Digital	Parallel A3
15	A2	Input	Digital	Parallel A2
16	A1	Input	Digital	Parallel A1
17	A0	Input	Digital	Parallel A0
18	$\overline{CS}$	Input	Digital	Active Low Parallel Chip Select with Internal Pull-up
19-26	S[0:7]	Input	Analog	Muxed Inputs
27	AV_{SS}	—	Power	Analog Negative Supply
28	COM	Output	Analog	Muxed Output[2]

Notes:

1. For proper operation, V_{DD} and $V_{DD\text{-}IO}$ must be applied before or simultaneously with AV_{DD}.
2. Continuous operation with low load resistance is not recommended. (See Figure 9)

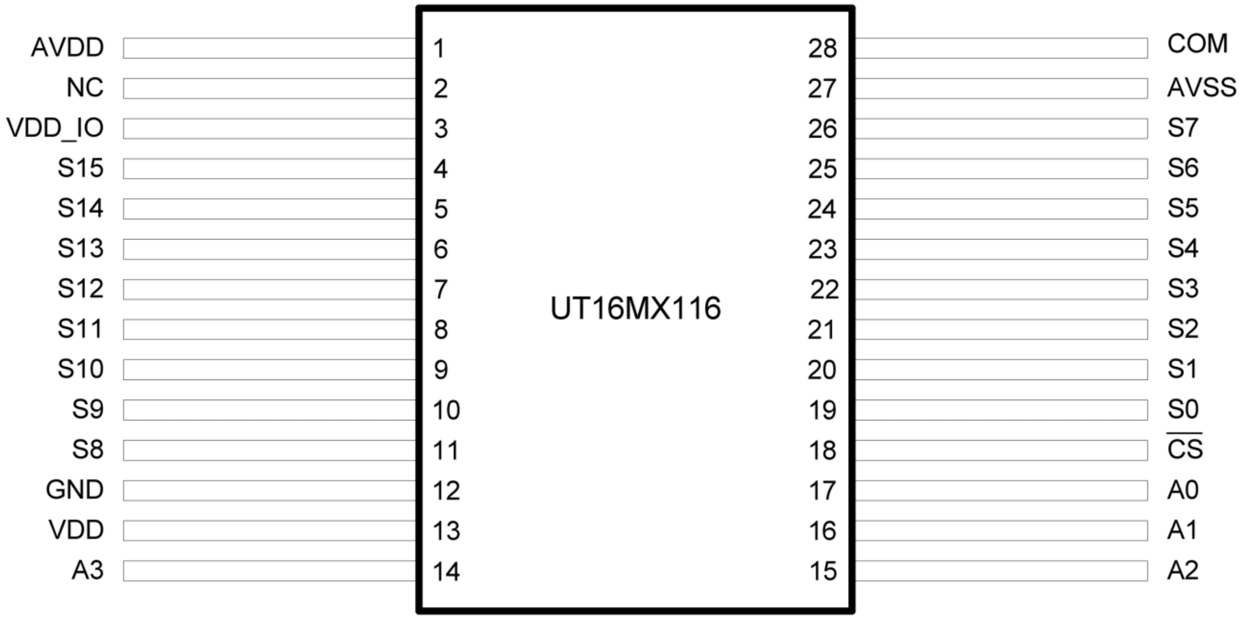

Figure 2: UT16MX116 Pinout

Table 2: UT16MX117 Pin Description

Pin No.	Name	I/O	Type	Description
1	AV_{DD}	—	Power	Analog Positive Supply[1]
2	$\overline{\text{RESET}}$	Input	Digital	Active Low Reset with Internal Pull-up
3	V_{DD_IO}	—	Power	Digital I/O Supply[1]
4-11	S[15:8]	Input	Analog	Muxed Inputs
12	GND	—	Power	Digital Ground
13	VDD	—	Power	Digital Core Supply[1]
14	NC	—	—	No Connection
15	SCLK	Input	Digital	SPI™ Clock
16	MOSI	Input	Digital	Master-out-Slave-in (Din)
17	MISO	Output	Digital	Master-in-Slave-out (Dout)
18	$\overline{\text{SS}}$	Input	Digital	Active Low SPI™ Shift Control with Internal Pull-up
19-26	S[0:7]	Input	Analog	Muxed Inputs
27	AV_{SS}	—	Power	Analog Negative Supply
28	COM	Output	Analog	Muxed Output[2]

Notes:

1. For proper operation, V_{DD} and $V_{DD\text{-}IO}$ must be applied before or simultaneously with AV_{DD}.
2. Continuous operation with low load resistance is not recommended. (See Figure 9)

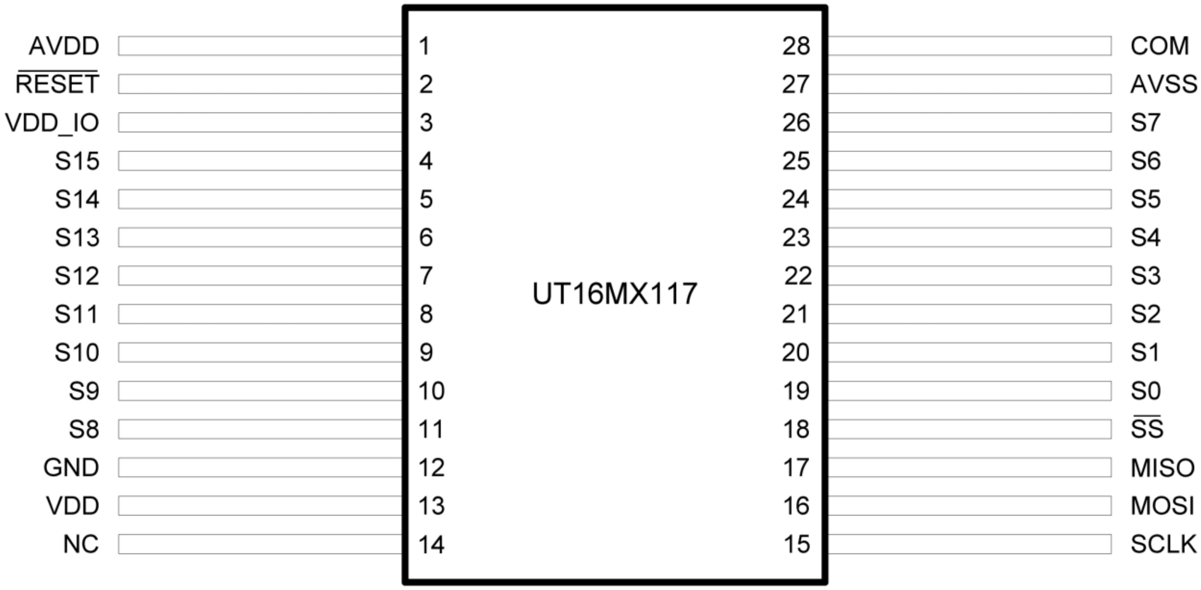

Figure 3: Figure 3. UT16MX117 Pinout

Table 3: UT16MX116 Truth Table

$\overline{CS}$	A3	A2	A1	A0	COM
1	X	X	X	X	Previous Decide State
0	0	0	0	0	S0
0	0	0	0	1	S1
0	0	0	1	0	S2
0	0	0	1	1	S3
0	0	1	0	0	S4
0	0	1	0	1	S5
0	0	1	1	0	S6
0	0	1	1	1	S7
0	1	0	0	0	S8
0	1	0	0	1	S9
0	1	0	1	0	S10
0	1	0	1	1	S11
0	1	1	0	0	S12
0	1	1	0	1	S13
0	1	1	1	0	S14
0	1	1	1	1	S15

Operational Environment

Parameter	Limit	Units
Total Ionizing Dose (TID)	300	krad(Si)
Single Event Latchup (SEL)	>110	MeV-cm²/mg
Single Event Upset Threshold (SEU)	>62.3	MeV-cm²/mg

Absolute Maximum Ratings[1]

Symbol	Parameter	Limits
AV_{DD}	Analog Positive Supply Voltage	7.5V
AV_{SS}	Analog Negative Supply Voltage	-0.3V
V_{DD_IO}	Digital I/O Supply Voltage (referenced to GND)	6.5V
V_{DD}	Digital Supply Voltage (referenced to GND)	4.5V
P_D	Static Power Dissipation	150 mW
T_J	Junction Temperature	-55°C to +130°C
T_{STG}	Storage Temperature	-65°C to +150°C
ESD_{HBM}	Electrostatic Discharge using Human Body Model	2kV

Note:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.

Recommended Operating Conditions

Symbol	Parameter	Limits
AV_{DD}	Analog Positive Supply Voltage	4.5V to 5.5V
AV_{SS}	Analog Negative Supply Voltage	0.0V
V_{DD_IO}	Digital I/O Supply Voltage (referenced to GND)	3.0V to 5.5V
V_{DD}	Digital Supply Voltage (referenced to GND)	3.0V to 3.6V
V_{IN}	Analog Switch Input Voltage	AV_{SS} to AV_{DD}
V_I	Digital Input Voltage	0V to V_{DD_IO}
T_C	Case Operating Temperature Range	-55°C to +125°C
T_J	Junction Operating Temperature [1]	-55°C to +130°C

Note:

1. Thermal resistance, Θ_{JC}, of junction-to-case is 4.8° C/W.

DC Electrical Characteristics [1]

(AV_{DD}=5.0V ± 0.5V, V_{DD}=3.3V ± 0.3V, V_{DD_IO}=3.0V to 5.5V, GND=0V; -55℃ ≤ T_C ≤ +125℃)

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
V_{IL}	Digital input low	V_{DD_IO} = 3.0V	-0.3		0.8	V
		V_{DD_IO}= 4.5V			1.35	V
V_{IH}	Digital input high	V_{DD_IO} = 3.0V	2.0			V
		V_{DD_IO} = 4.5V	3.15			V
V_{OL}	Digital output low (UT16MX117)	V_{DD_IO} = 3.0V I_{OL} = 100µA			0.2	V
		V_{DD_IO} = 3.0V I_{OL} = 2mA			0.4	V
		V_{DD_IO} = 4.5V I_{OL} = 2mA			0.5	V
V_{OH}	Digital output high (UT16MX117)	V_{DD_IO} = 3.0V I_{OH} = -100µA	2.8			V
		V_{DD_IO} = 3.0V I_{OH} = -2mA	2.4			V
		V_{DD_IO} = 4.5V I_{OH} = -2mA	3.7			V
R_{ON}	On resistance	V_{IN}= AV_{SS} to AV_{DD} V_{COM} = V_{IN} - 0.3V	40	145	300	Ω
I_{OFF}	Analog I/O leakage current (switch off)2	AV_{DD} = 5.5V V_{DD} = 3.6V V_{DD_IO} = 5.5V V_{IN} = AV_{SS} or AV_{DD}	-1.6		1.6	µA
I_{IL}	Digital input current low LVCMOS / CMOS inputs Inputs with pull-up	V_{DD_IO} = 5.5V V_{IL} = GND	-1 -380		1.0 -20	µA µA
I_{IH}	Digital input current high LVCMOS / CMOS inputs Inputs with pull-up	V_{DD_IO} = 5.5V V_{IH} = V_{DD_IO}	-1.0 -25		1.0 25	µA µA

DC Electrical Characteristics [1] (Cont'd)

(AV_{DD}=5.0V ± 0.5V, V_{DD}=3.3V ± 0.3V, V_{DD_IO}=3.0V to 5.5V, GND=0V; -55℃ ≤ T_C ≤ +125℃)

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
Q_{IDD}	Quiescent analog supply current	AV_{DD} = 5.5V V_{DD} = 3.6V V_{DD_IO} = 5.5V V_{IH} = V_{DD_IO} V_{IL} = GND			10	µA
$Q_{IDD\_IO\_CMOS}$	Quiescent digital I/O supply current (CMOS)	AV_{DD} = 5.5V V_{DD} = 3.6V V_{DD_IO} = 5.5V V_{IH} = V_{DD_IO} V_{IL} = GND			2.2	mA
$Q_{IDD\_IO\_LVCMOS}$	Quiescent digital I/O supply current (LVCMOS)	AV_{DD} = 5.5V V_{DD} = 3.6V V_{DD_IO} = 3.6V V_{IH} = V_{DD_IO} V_{IL} = GND			2.0	µA
Q_{IDD_VDD}	Quiescent digital supply current	AV_{DD} = 5.5V V_{DD} = 3.6V V_{DD_IO} = 5.5V VIH = V_{DD_IO} VIL = GND			40	µA

Notes:

1. For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25℃ per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured (see ordering information).
2. This parameter cannot be tested on COM for the UT16MX116 device because the pin is continuously on.

AC Electrical Characteristics [1, 2]

(AV_{DD}=5.0V ± 0.5V, V_{DD}=3.3V ± 0.3V, V_{DD_IO}=3.0V to 5.5V, GND=0V-55℃ ≤ T_C ≤ +125℃)

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
C_{IN}	Input analog capacitance (switch off)[3]	F_{IN}=1MHz @ 0V		10	20	pF
$C_{IN\_DIGITAL}$	Input digital capacitance[3]	F_{IN}=1MHz @ 0V		46	55	pF
C_{OUT}	Output capacitance at COM[3]	F_{IN}=1MHz @ 0V		28	40	pF
O_{ISO}	Off isolation feed through attenuation (switch off)[4]	R_L=600Ω C_L=50pF F_{IN}=1kHz sine wave			-80	dB
BW	Bandwidth (frequency response)[4]	R_{SOURCE} = 50Ω R_L = 2.2MΩ C_L = 12pF V_{IN} = 1Vp-p	51			MHz
X_{TALK2}	Cross talk (between any two channels)[4]	R_L=1k Ω C_L=50pF F_{IN}=1kHz sine wave			-80	dB
t_S	Settling time of output at COM within 1% of final output voltage[4]	Within 1% of final output voltage RL=100kΩ CL=50pf			120	ns
T_{HD}	Total Harmonic Distortion[4]	R_L=1k Ω CL=50pF F_{IN}=1MHz sine wave V_{IN}=5Vp-p			5.0	%

Notes:

1. For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25℃ per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured (see ordering information).
2. Continuous operation with low load resistance is not recommended. (See Figure 9)
3. Parameters guaranteed by characterization.
4. Parameters guaranteed by design.

Timing Characteristics (UT16MX116)[1, 2]

(AV_{DD}=5.0V ± 0.5V, V_{DD}=3.3V ± 0.3V, V_{DD_IO}=3.0V to 5.5V, GND=0V-55℃ ≤ T_C ≤ +125℃)

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
t_{PROP_S}	Propagation delay of analog input (S[x]) to analog output (COM) measured at 50%	R_T=50Ω C_L=50pF See Figures 8&10			25	ns
t_{PROP_D}	Propagation delay of any changes in the digital inputs (A[3:0], $\overline{CS}$, $\overline{SS}$) affecting the analog output (COM)	R_T=50 Ω CL=50pF See Figures 4&10	25		140	ns
t_{MUX}	Mux decoding time	R_T=50Ω C_L=50pF See Figures 4&10			50	ns
t_{BBM}	Break-Before-Make-Delay	R_T=50Ω C_L=50pF See Figures 4&10	15		90	ns
t_{AS1}	The minimum amount of time required for the address signals (A[3:0]) to be stable before the falling edge of $\overline{CS}$[3]	See Figure 4	3.0			ns
t_{AS2}	The minimum amount of time required for the address signals (A[3:0]) to be stable after the rising edge of $\overline{CS}$[3]	See Figure 4	5.0			ns

Notes:

1. For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25℃ per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured (see ordering information).
2. Continuous operation with low load resistance is not recommended. (See Figure 9)
3. Parameters guaranteed by design.

Timing Characteristics (UT16MX117) [1, 2]

(AV_{DD}=5.0V ± 0.5V, V_{DD}=3.3V ± 0.3V, V_{DD_IO}=3.0V to 5.5V, GND=0V; -55°C ≤ T_C ≤ +125°C)

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
t_{PROP_S}	Propagation delay of analog input (S[x]) to analog output (COM) measured at 50%	R_T=50Ω CL=50pF See Figures 8&10			25	ns
t_{PROP_D}	Propagation delay of any changes in the digital inputs (A[3:0], $\overline{CS}$, $\overline{SS}$) affecting the analog output (COM)	R_T=50Ω C_L=50pF See Figures 5&10	25		140	ns
t_{MUX}	Mux decoding time	R_T=50Ω C_L=50pF See Figures 5&10			50	ns
t_{BBM}	Break-Before-Make-Delay	RT=50Ω C_L=50pF See Figures 5&10	15		90	ns
t_{PZLH}	Output enable time from HiZ to low or high once $\overline{RESET}$ is pulled low	R_T=50Ω C_L=50pF See Figures 7&10			90	ns
t_{PLHZ}	Output disable time from low or high to HiZ once $\overline{RESET}$ is pulled high	R_T=50Ω C_L=50pF See Figures 7&10			55	ns
f_{SCLK}	SCLK frequency	See Figure 5			2.0	MHz
t_H	SCLK high time	See Figure 5	190			ns
t_L	SCLK low time	See Figure 5	190			ns
t_{SSU}	First SCLK setup time (for shifting window)	See Figure 5	6.0			ns
t_{SSH}	Last SCLK hold time (for shifting window)	See Figure 5	10			ns
t_{SU}	Data in (MOSI) setup time wrt rising edge SCLK	See Figure 5	3.0			ns
t_{HD}	Data in (MOSI) hold time wrt rising edge SCLK	See Figure 5	5.0			ns
t_{DO}	Data out (MISO) valid (after falling edge of SCLK)	C_L=50pF See Figure 5			43	ns
t_{DR}	Data out (MISO) rise time	10-90% V_{DD_IO} CL=50pF			70	ns
t_{DF}	Data out (MISO) fall time	10-90% V_{DD_IO} CL=50pF			70	ns

Notes:

1. For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured (see ordering information).
2. Continuous operation with low load resistance is not recommended. (See Figure 9).

Timing Diagrams

Multiplexer Asynchronous Parallel Timing (UT16MX116)

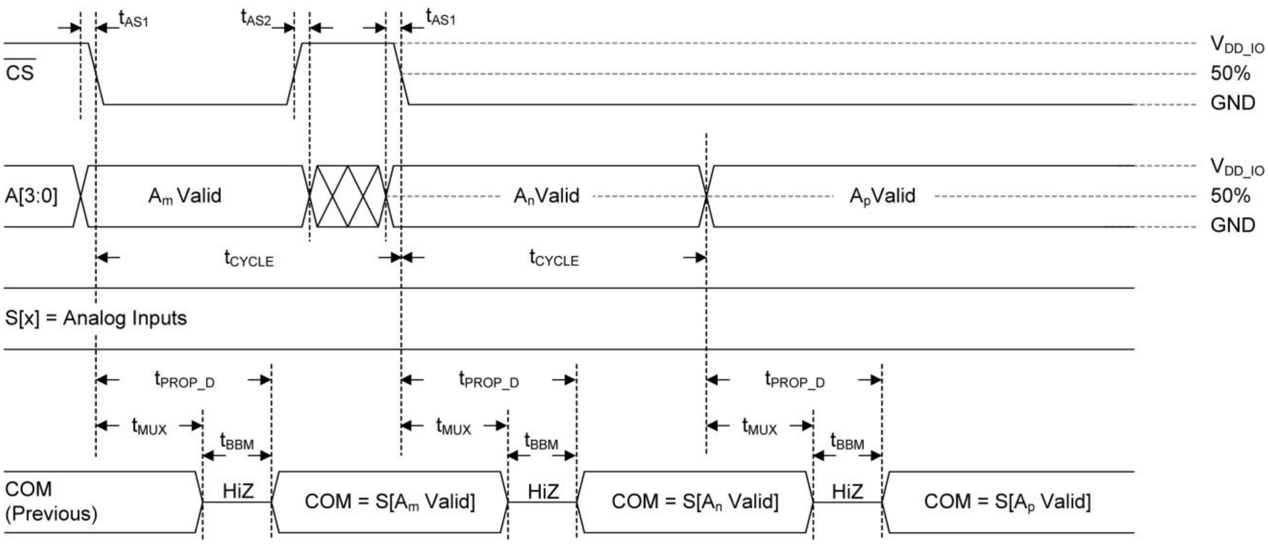

Figure 4: gUT16MX116 Timing Diagram

Notes:

1. $\overline{CS}$ may be held in a continuous low state, holding $\overline{CS}$ high provides protection for false address change.
2. t_{CYCLE} is the minimum cycle time between the falling edges of $\overline{CS}$ and/or any address changes. If t_{CYCLE} is shorter than t_{PROP_D}, an addressing error may occur.
3. All bits (A[3:0]) of any address change should be received by the UT16MX116 within 18ns of the first bit change for proper operation.

Multiplexer Serial Timing (UT16MX117)

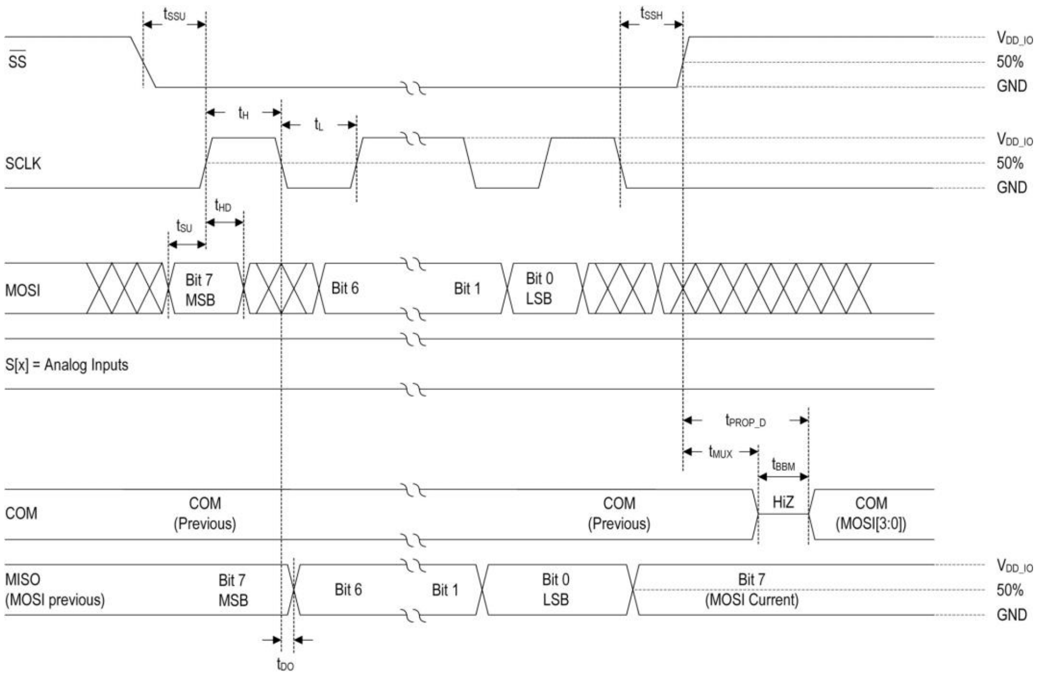

Figure 5: UT16MX117 Timing Diagram

SPI™ Protocol (UT16MX117)

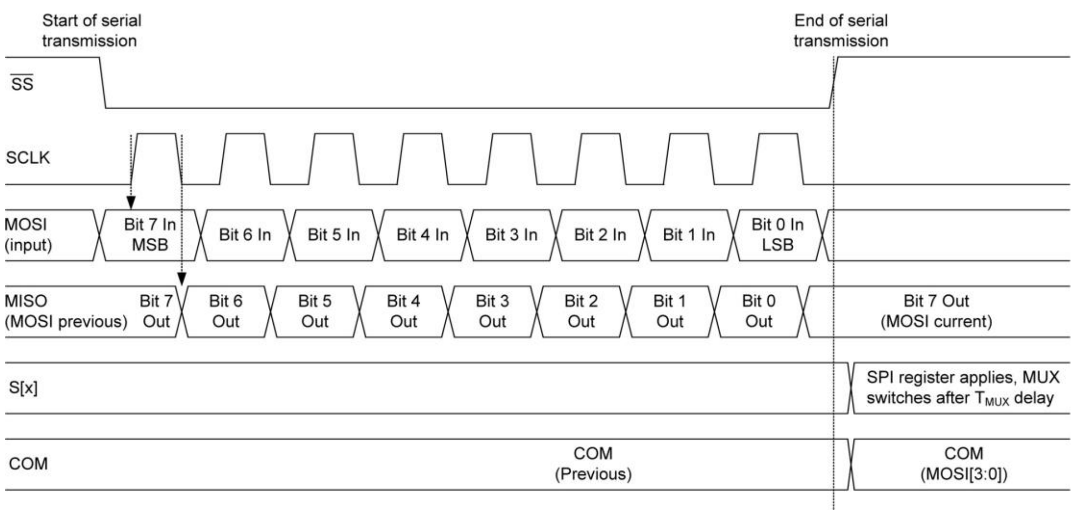

Figure 6: SPI™ Protocol Timing

Note:

1. See figure 5, Multiplexer Serial Timing (UT16MX117), for detailed timing.

Multiplexer RESET Enable/Disable Timing (UT116MX117)

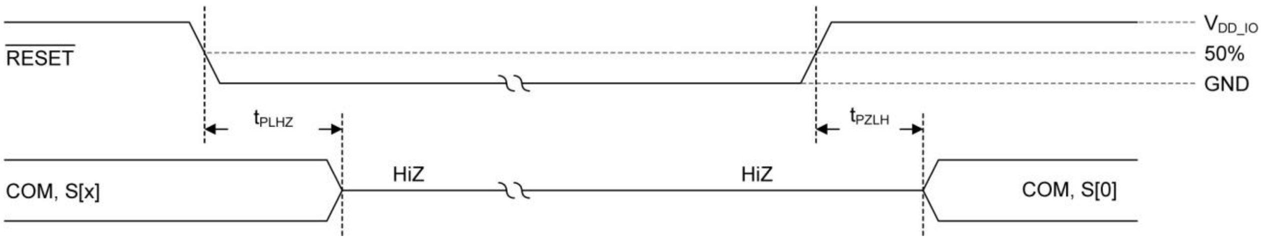

Figure 7: RESET Timing Diagram (UT116MX117 only)

Note:

1. S[x] represents the analog signal channel connected to COM prior to the falling edge of RESET.

Multiplexer Analog Timing (UT16MX116/117)

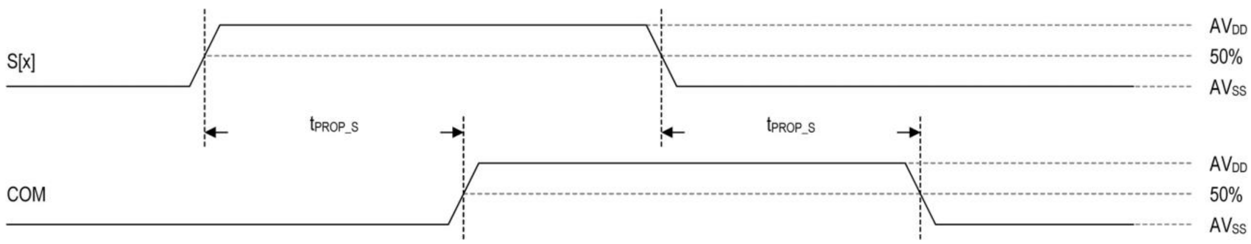

Figure 8: Analog Timing Diagram (Used for UT16MX116/117)

Note:

1. S[x] represents the analog signal channel connected to COM while in active mode of all device types with the address already set and all digital inputs held constant.

Minimum Multiplexer Total Path Resistance (UT16MX116/117)

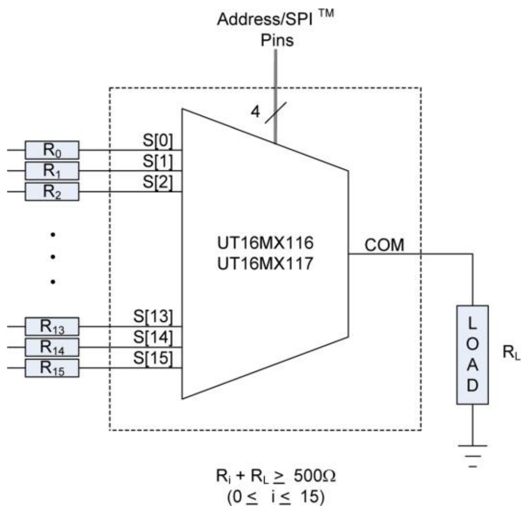

Figure 9: Minimum Total Path Resistance for Continuous DC Operation on Any Single Channel

Note:

1. Continuous DC operation on any single channel where $R_i + R_L < 500\Omega$ may affect device reliability and performance. Frontgrade does not guarantee product reliability and performance where $R_i + R_L < 500\Omega$ and the device operates continuously in a DC bias configuration.

Multiplexer Load Conditions for Test (UT16MX116/117)

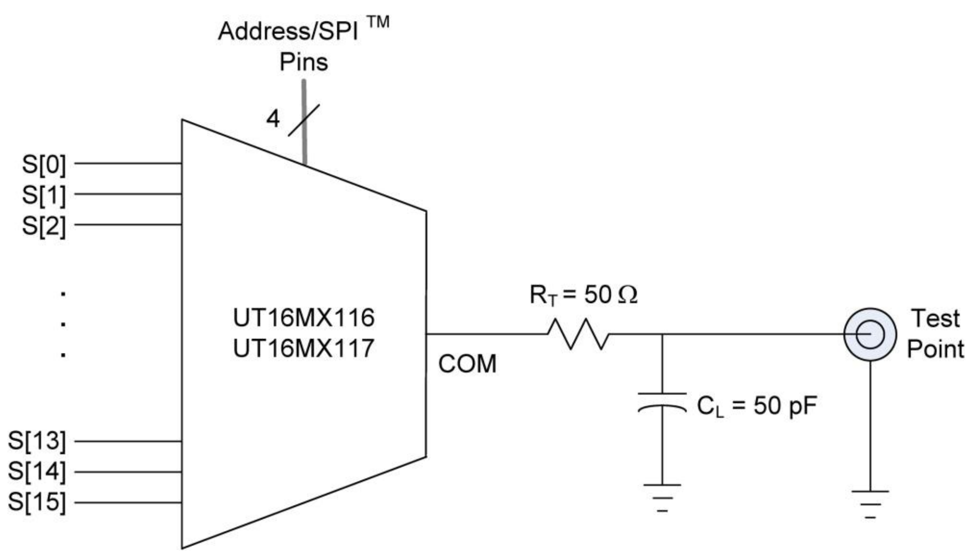

Figure 10: UT16MX116/117 Test Circuit

Packaging

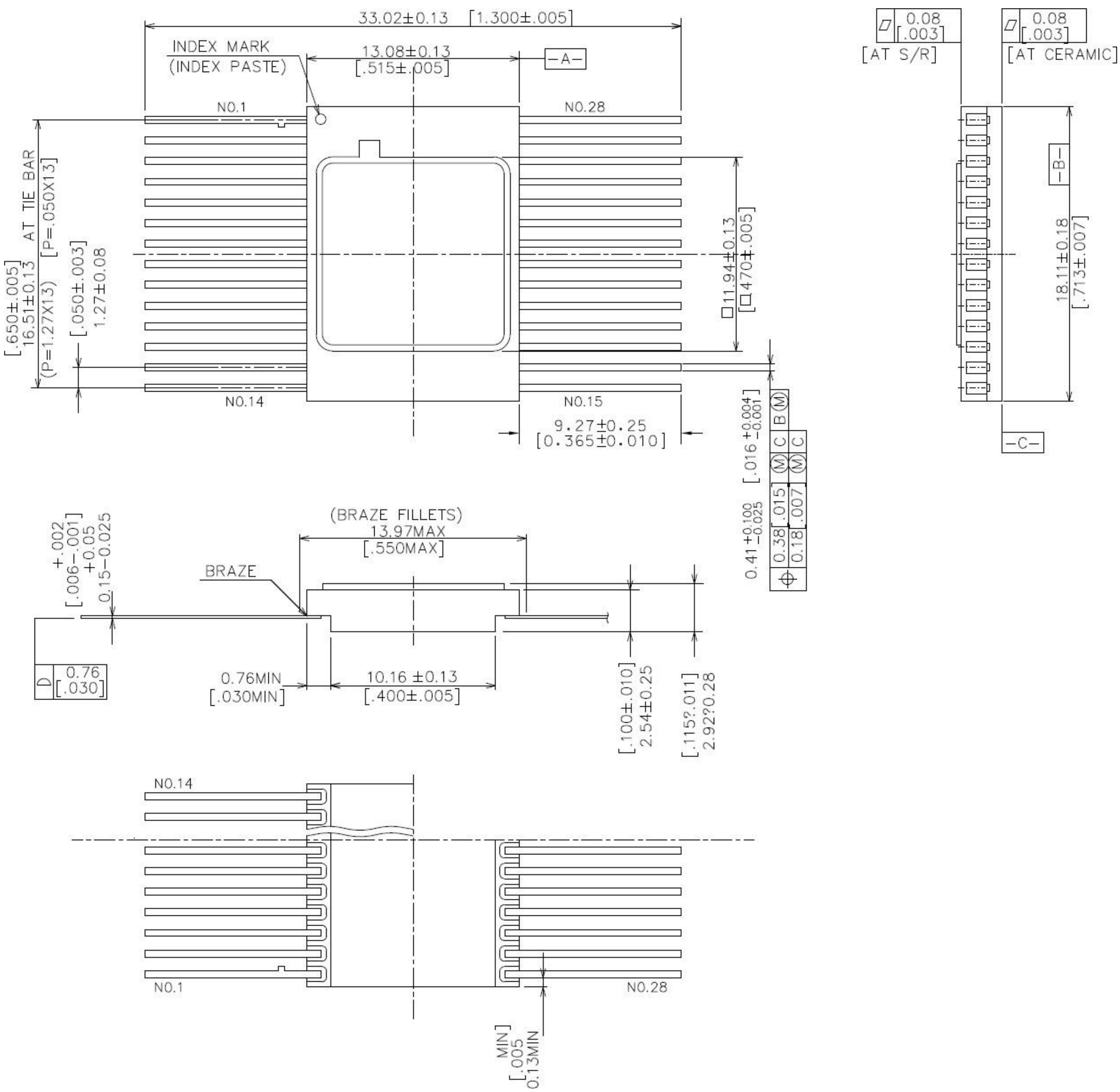

Figure 11: 28-Lead Ceramic Flat Package

Notes:

1. Gold plated 100 to 225 microinches over electroplated nickel 100 to 350 microinches per mil-prf-38535.
2. Seal ring is electrically connected to VSS.

Trademarks:

SPI™ /QSPI™ are trademarks of Motorola, Inc. MICROWIRE™ is a trademark of National Semiconductor

Ordering Information

Frontgrade Part Numbering Ordering Information

UTxxxx ** * * * *

Lead Finish: (Note: 1)
(C) = Gold

Screening Level: (Notes: 2, 3)
(P) = Prototype Flow
(C) = HiRel Flow

Package Type:
(X) = 28-pin CFP Ceramic Flatpack

TID Tolerance:
(-) = None

Device Type:
(16) = Asynchronous Parallel
(17) = Serial (SPI™)

Generic part number: (16MX1) = 16:1 MUX

Notes:

1. Lead finish is "C" (Gold) only.
2. Prototype flow per CAES Manufacturing Flows Document. Tested at 25℃ only. Lead finish is Gold "C" only. Radiation neither tested nor guaranteed.
3. HiRel Flow per CAES Manufacturing Flows Document.

SMD Part Number Ordering Information

5962 * *** ** * * ***

Lead Finish: (Note: 1)
(C) = Gold

Case Outline:
(X) = 28-pin CFP Ceramic Flatpack

Class Designator:
(Q) = QML Class Q
(V) = QML Class V

Device Type:
(01) = Serial (SPI™)
(03) = Asynchronous Parallel

Drawing Number:
(10237)

Total Dose:
(R) = 100 krad(Si)
(F) = 300 krad(Si)

Federal Stock Class Designator

Notes:

1. Lead finish is "C" (Gold) only.

Revision History

Date	Revision #	Author	Change Description	Page #
2-29		BM	UT16MX116 requires the following operation in order to properly initialize the part following power- up: All address states for the A[3;0] address lines must be exercised following AVDD power-up to ensure correct addressing. Once this operation has been completed, normal asynchronous addressing can then be used to select the desired input channel (i.e. one of S[15:0]) to connect to the COM output. The S[15:0] analog channels are routed asynchronously via the binary decoding of A[3:0] static logic levels after initialization.	2

Datasheet Definitions

	Definition
Advanced Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the **datasheet is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final.**
Preliminary Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.