

UT16MX113/114/115

Features

- 16-to-1 Analog Mux
- 100Ω Signal paths (typical)
- 5V single analog supply
- Rail-to-Rail signal handling
- Asynchronous $\overline{\text{RESET}}$ input
- SPI™/QSPI™ and MICROWIRE™ compatible serial interface (UT16MX115)
- Asynchronous parallel input Interface (UT16MX113)
- Synchronous parallel input Interface (UT16MX114)
- LVCMOS/LVTTL compatible inputs
- 2kV ESD Protection (per MIL-STD-883, Method 3015.7)
- Operational environment:
 - Total ionizing dose: 300 krad(Si)
 - SEL immune to a LET of 110 MeV-cm²/mg
 - SEU immune to a LET of 62.3 MeV-cm²/mg
- Packaging: 28-lead Ceramic Flatpack
- Standard Microcircuit Drawing 5962-10236
 - QML Q, QML V

Introduction

The UT16MX113/114/115 are low voltage analog multiplexers with a convenient LVCMOS (3.3V) or CMOS digital interface. The analog muxes have Break- Before-Make architecture with a low channel resistance. The muxes support rail-to-rail input signal levels. The multiplexer supports serial (SPI™), or parallel (asynchronous or synchronous) interface.

The UT16MX113/114/115 operates with a single 5V ($\pm 10\%$) analog power supply. An external 3.3V digital voltage supply is required, for the digital circuitry and the digital I/O.

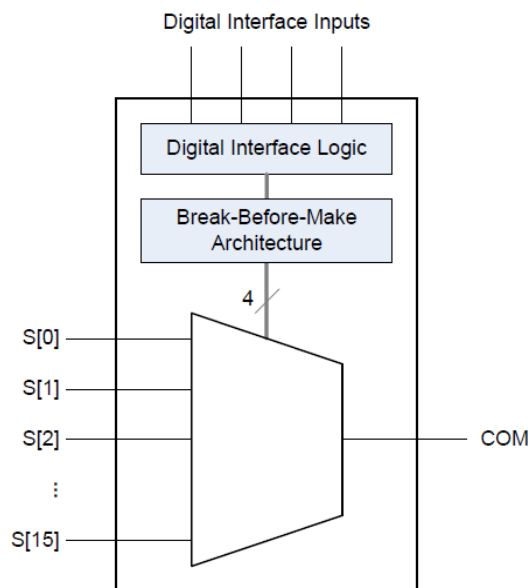


Figure 1. UT16MX113/114/115 Block Diagram

UT16MX113/114/115

Functional Description

All mux decoding (whether for the UT16MX113, UT16MX114, or UT16MX115 device) operation utilizes a Break-Before-Make process to prevent shorting between analog inputs during address transitions.

UT16MX113:

The UT16MX113 utilizes a parallel interface which operates in asynchronous mode much like discrete logic switches. The UT16MX113 requires the following operation in order to properly initialize the part following power-up: All address states for the A[3:0] address lines must be exercised following AVDD power-up to ensure correct addressing. Once this operation has been completed, normal asynchronous addressing can then be used to select the desired input channel (i.e. one of S[15:0]) to connect to the COM output. The S[15:0] analog channels are routed asynchronously via the binary decoding of A[3:0] static logic levels after initialization. The address pins A[3:0] are required to hold static levels for proper mux operation. Any change in A[3:0] pins directs the COM connection to the appropriate S[x] input after approximately 100ns propagation delay (including the Break-Before-Make delay). All bits (A[3:0]) of any address change should be received by the UT16MX113 within 18 ns of the first bit change for proper operation. The asynchronous parallel interface mode requires \overline{CS} to be low for accepting a change on the address pins A[3:0]. When \overline{CS} is high, the UT16MX113 disables the address pins A[3:0], as well as holding the last valid address state, thereby mitigating against any single-event upsets or transients on the address bus.

UT16MX114:

The UT16MX114 utilizes a parallel interface which operates in a synchronous mode which utilizes the PLATCH input as the latching clock. Upon rising edge of PLATCH, logic level at the A[3:0] pins will be registered and retained internally to decode the mux. Based on the values of the A[3:0] pins, COM is connected to the appropriate S[x] input after approximately 100ns propagation delay (including the Break-Before-Make delay).

UT16MX115:

The UT16MX115 utilizes a serial interface that supports the standard that is compatible with MICROWIRE™, SPI™, and QSPI™. The UT16MX115 SPI™ interface can be depicted as an 8-bit serial shift register controlled by \overline{SS} , clocked by the rising edge of SCLK. The 8-bit shift register is for compatibility purposes, even though this UT16MX115 serial address setting requires only 4 bits. The four LSB of the 8-bit shift register are the four bits decoding the mux address. When shifting data into the part, the MSB enters the part first. The four MSB may be set to zeroes, e.g., the 8-bit command "00001001" would set the mux to connect COM to S[9].

The UT16MX115 is considered a slave SPI™ device with MOSI (Master Out Slave In) as the data input pin to the device. The data is shifted with D7 as the first bit into the shift register, and also the first bit out to the MISO (Master In Slave Out) output pin after eight clock cycles of SCLK. The signal on the \overline{SS} pin defines the window when the address bits are shifted into the device. This occurs when signal on \overline{SS} is low. Only when \overline{SS} is high at the close of the shifting window, does the mux decoding get updated and COM is directed to the decoded S[x] input (after Break-Before-Make delay).

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SPI™ Operations:

The SPI™ (Serial Peripheral Interface) is implemented as a synchronous 8-bit serial shift register controlled by four pins: MOSI, MISO, SCLK, and \overline{SS} . This is compatible with the SPI™/QSPI™ standard as defined by Motorola on the MC68HCxx line of microcontrollers. This SPI™ also conforms to the MICROWIRE™ interface, an SPI™ subset interface, as defined by National Semiconductor.

The UT16MX115 SPI™ is always a slave device, where MOSI, SCLK, and \overline{SS} are controlled by a master device. MISO output is used as receiving slave data or to daisy chain several SPI™ devices in appropriate applications.

The MUX select functionality is controlled by the four LSB of the 8-bit SPI™ shift registers. When shifting, the first SCLK rising edge clocks in the MSB first. The first falling edge of the SCLK clocks out the 6th bit of the current values in the SPI™ registers, since the 7th bit already appears at the MISO at the start of a serial transmission before the first SCLK (Figures 7 and 8).

Reset Function (UT16MX114/115 Only):

The \overline{RESET} pin is used to reset all internal logic circuits. \overline{RESET} held low also keeps all COM and S[15:0] analog I/Os in a high impedance state. This is the recommended condition at system power-up.

Asserting \overline{RESET} (active low) resets all of the internal address decoding registers to 0, thus steering the COM to connect to S[0] while in the high impedance state. When \overline{RESET} is de-asserted (high), both COM and S[0] will come out of the high impedance state and COM will be driven by S[0].

Table 1: UT16MX113 Pin Description

Pin No.	Name	I/O	Type	Description
1	AV _{DD}	--	Power	Analog Positive Supply ¹
2	NC	--	--	No Connection
3	NC	--	--	No Connection
4-11	S[15:8]	Input	Analog	Muxed Inputs
12	GND	--	Power	Digital Ground
13	V _{DD}	--	Power	Digital Positive Supply ¹
14	A3	Input	Digital	Parallel A3
15	A2	Input	Digital	Parallel A2
16	A1	Input	Digital	Parallel A1
17	A0	Input	Digital	Parallel A0
18	\overline{CS}	Input	Digital	Active Low Parallel Chip Select with Internal Pull-up
19-26	S[0:7]	Input	Analog	Muxed Inputs
27	AV _{SS}	--	Power	Analog Negative Supply
28	COM	Output	Analog	Muxed Output ²

Notes:

- 1) For proper operation, V_{DD} must be applied before or simultaneously with AV_{DD}.
- 2) Continuous operation with low load resistance is not recommended. (See Figure 11)

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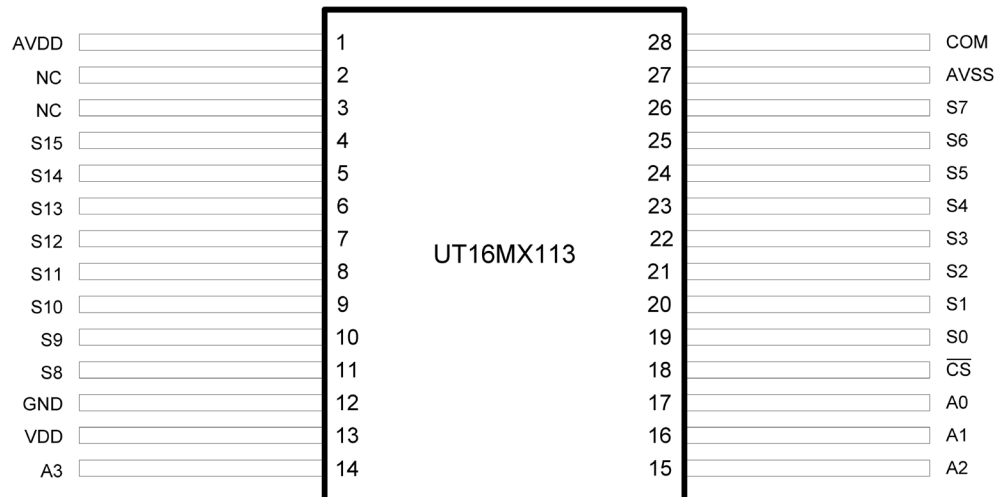


Table 2: UT16MX114 Pin Description

Pin No.	Name	I/O	Type	Description
1	AV _{DD}	--	Power	Analog Positive Supply ¹
2	RESET	Input	Digital	Active Low Reset with Internal Pull-up
3	PLATCH	Input	Digital	Parallel Latch with Internal Pull-down
4-11	S[15:8]	Input	Analog	Muxed Inputs
12	GND	--	Power	Digital Ground
13	V _{DD}	--	Power	Digital Positive Supply ¹
14	A3	Input	Digital	Parallel A3
15	A2	Input	Digital	Parallel A2
16	A1	Input	Digital	Parallel A1
17	A0	Input	Digital	Parallel A0
18	NC	--	--	No Connection
19-26	S[0:7]	Input	Analog	Muxed Inputs
27	AV _{SS}	--	Power	Analog Negative Supply
28	COM	Output	Analog	Muxed Output ²

Notes:

- 1) For proper operation, V_{DD} must be applied before or simultaneously with AV_{DD}.
- 2) Continuous operation with low load resistance is not recommended. (See Figure 11).

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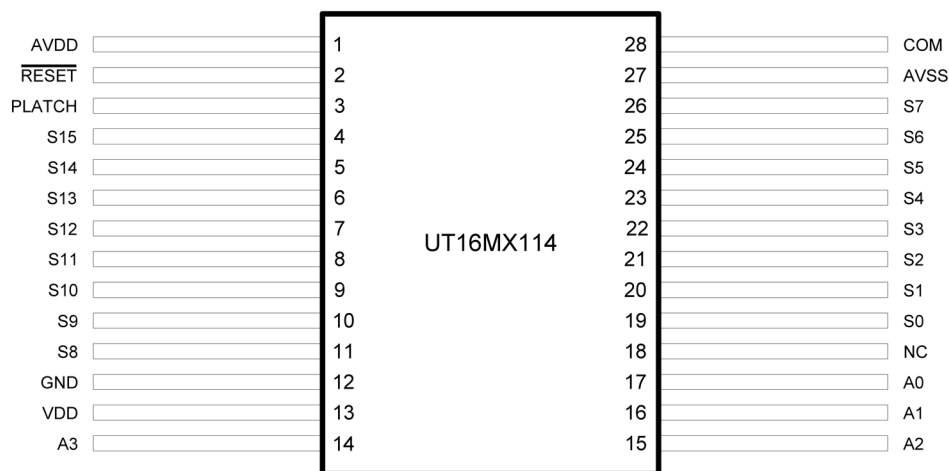


Figure 3. UT16MX114 Pinout

Table 3: UT16MX115 Pin Description

Pin No.	Name	I/O	Type	Description
1	AV _{DD}	--	Power	Analog Positive Supply ¹
2	RESET	Input	Digital	Active Low Reset with Internal Pull-up
3	NC	--	--	No Connection
4-11	S[15:8]	Input	Analog	Muxed Inputs
12	GND	--	Power	Digital Ground
13	V _{DD}	--	Power	Digital Positive Supply ¹
14	NC	--	--	No Connection
15	SCLK	Input	Digital	SPI™ Clock
16	MOSI	Input	Digital	Master-out-Slave-in (Din)
17	MISO	Output	Digital	Master-in-Slave-out (Dout)
18	SS	Input	Digital	SPI™ Shift Control with Internal Pull-up
19-26	S[0:7]	Input	Analog	Muxed Inputs
27	AV _{SS}	--	Power	Analog Negative Supply
28	COM	Output	Analog	Muxed Output ²

Notes:

- 1) For proper operation, V_{DD} must be applied before or simultaneously with AV_{DD}.
- 2) Continuous operation with low load resistance is not recommended. (See Figure 11)

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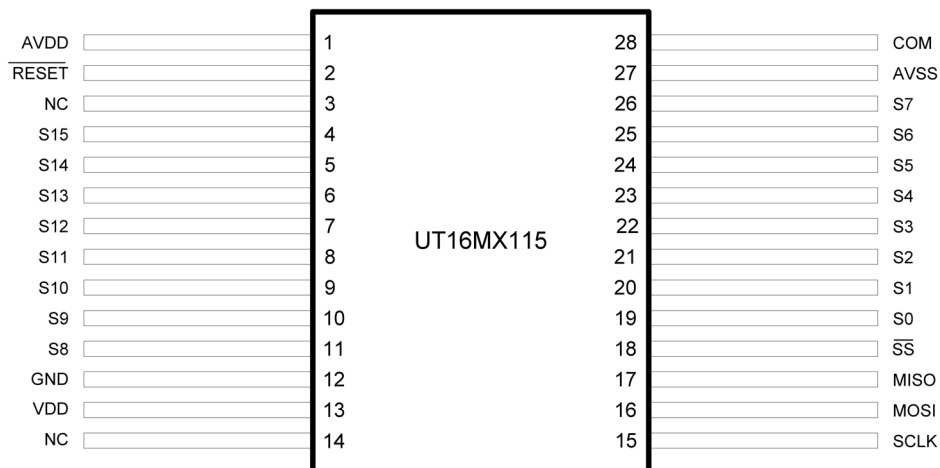


Table 4: UT16MX113 Truth Table

\overline{CS}	A3	A2	A1	A0	COM
1	X	X	X	X	Previous Decide State
0	0	0	0	0	S0
0	0	0	0	1	S1
0	0	0	1	0	S2
0	0	0	1	1	S3
0	0	1	0	0	S4
0	0	1	0	1	S5
0	0	1	1	0	S6
0	0	1	1	1	S7
0	1	0	0	0	S8
0	1	0	0	1	S9
0	1	0	1	0	S10
0	1	0	1	1	S11
0	1	1	0	0	S12
0	1	1	0	1	S13
0	1	1	1	0	S14
0	1	1	1	1	S15

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Table 5: UT16MX114 Truth Table

RESET	PLATCH	A3	A2	A1	A0	COM
0	X	X	X	X	X	Tri-State (S[15:0] and COM)
1	Rising Edge	0	0	0	0	S0
1	Rising Edge	0	0	0	1	S1
1	Rising Edge	0	0	1	0	S2
1	Rising Edge	0	0	1	1	S3
1	Rising Edge	0	1	0	0	S4
1	Rising Edge	0	1	0	1	S5
1	Rising Edge	0	1	1	0	S6
1	Rising Edge	0	1	1	1	S7
1	Rising Edge	1	0	0	0	S8
1	Rising Edge	1	0	0	1	S9
1	Rising Edge	1	0	1	0	S10
1	Rising Edge	1	0	1	1	S11
1	Rising Edge	1	1	0	0	S12
1	Rising Edge	1	1	0	1	S13
1	Rising Edge	1	1	1	0	S14
1	Rising Edge	1	1	1	1	S15

Operational Environment

Parameter	Limit	Units
Total Ionizing Dose (TID)	300	krad(Si)
Single Event Latchup (SEL)	>110	MeV-cm ² /mg
Single Event Upset Threshold (SEU)	>62.3	MeV-cm ² /mg

Absolute Maximum Ratings¹

Symbol	Parameter	Limits
AV _{DD}	Analog Positive Supply Voltage	7.5V
AV _{SS}	Analog Negative Supply Voltage	-0.3V
V _{DD}	Digital Supply Voltage (referenced to GND)	4.5V
P _D	Static Power Dissipation	150 mW
T _J	Junction Temperature	-55°C to +130°C
T _{STG}	Storage Temperature	-65°C to +150°C
ESD _{HBM}	Electrostatic Discharge using Human Body Model	2kV

Notes:

- 1) Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.

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Recommended Operating Conditions

Symbol	Parameter	Limits
AV _{DD}	Analog Positive Supply Voltage	4.5V to 5.5V
AV _{SS}	Analog Negative Supply Voltage	0.0V
V _{DD}	Digital Supply Voltage (referenced to GND)	3.0V to 3.6V
V _{IN}	Analog Switch Input Voltage	AV _{SS} to AV _{DD}
V _I	Digital Input Voltage	0V to V _{DD}
T _C	Case Operating Temperature Range	-55°C to +125°C
T _J	Junction Operating Temperature ¹	-55°C to +130°C

Note:

1) Thermal resistance, Θ_{JC} , of junction-to-case is 4.8°C/W.

DC Electrical Characteristics¹

(AV_{DD}=5.0V ± 0.5V, V_{DD}=3.3V ± 0.3V, GND=0V; -55°C ≤ T_C ≤ +125°C)

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
V _{IL}	Digital input low	V _{DD} = 3.0V	-0.3		0.8	V
V _{IH}	Digital input high	V _{DD} = 3.0V	2.0			V
V _{OL}	Digital output low (UT16MX115)	V _{DD} = 3.0V I _{OL} = 100μA			0.2	V
		V _{DD} = 3.0V I _{OL} = 2mA			0.4	V
V _{OH}	Digital output high (UT16MX115)	V _{DD} = 3.0V I _{OH} = -100μA	2.8			V
		V _{DD} = 3.0V I _{OH} = -2mA	2.4			V
R _{ON}	On resistance	V _{IN} = AV _{SS} to AV _{DD} V _{COM} = V _{IN} - 0.3V	40	145	300	Ω
I _{OFF}	Analog I/O leakage current (switch off) ²	AV _{DD} = 5.5V V _{DD} = 3.6V V _{IN} = AV _{SS} or AV _{DD}	-1.6		1.6	μA
I _{IL}	Digital input current low	V _{DD} = 3.6V V _{IL} = GND	-1.0		1.0	μA
	LVC MOS / LV TTL inputs		-380		-20	μA
	Inputs with pull-up Inputs with a pull-down		-5.0		5.0	μA
I _{IH}	Digital input current high	V _{DD} = 3.6V V _{IH} = V _{DD}	-1.0		1.0	μA
	LVC MOS / LV TTL inputs		-60		60	μA
	Inputs with pull-up ³ Inputs with a pull-down		20		380	μA
Q _{IDD}	Quiescent analog supply current	AV _{DD} = 5.5V V _{DD} = 3.6V V _{IH} = V _{DD} V _{IL} = GND			10	μA
Q _{IDD_VDD}	Quiescent digital supply current	AV _{DD} = 5.5V			250	μA

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		$V_{DD} = 3.6V$ $V_{IH} = V_{DD}$ $V_{IL} = GND$				
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Notes:

- 1) For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured (see ordering information).
- 2) This parameter cannot be tested on COM for the UT16MX113 device because the pin is continuously on.
- 3) This parameter tested with PLATCH held low on the UT16MX114 device.

AC Electrical Characteristics ^{1,2}

($AV_{DD}=5.0V \pm 0.5V$, $V_{DD}=3.3V \pm 0.3V$, $GND=0V$; $-55^{\circ}C \leq T_C \leq +125^{\circ}C$)

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
C_{IN}	Input capacitance (switch off) ³	$F_{IN}=1MHz @ 0V$		40	50	pF
$C_{IN_DIGITAL}$	Input digital capacitance ³	$F_{IN}=1MHz @ 0V$		46	55	pF
C_{OUT}	Output capacitance at COM ³	$F_{IN}=1MHz @ 0V$		68	80	pF
O_{ISO}	Off isolation feed through attenuation (switch off) ⁴	$R_L=600\Omega$ $C_L=50pF$ $F_{IN}=1kHz$ sine wave			-80	dB
BW	Bandwidth (frequency response) ⁴	$R_{SOURCE} = 50\Omega$ $R_L = 2.2M\Omega$ $C_L = 12pF$ $V_{IN} = 1Vp-p$	51			MHz
X_{TALK2}	Cross talk (between any 2 channels) ⁴	$R_L=1k\Omega$ $C_L=50pF$ $F_{IN}=1kHz$ sine wave			-80	dB
t_s	Settling time of output at COM within 1% of final output voltage ⁴	Within 1% of final output voltage $R_L=100k\Omega$ $C_L=50pF$			120	ns
THD	Total Harmonic Distortion ⁴	$R_L=1k\Omega$ $C_L=50pF$ $F_{IN}=1MHz$ sine wave $V_{IN}=5Vp-p$			5.0	%

Notes:

- 1) For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured (see ordering information).
- 2) Continuous operation with low load resistance is not recommended. (See Figure 11)
- 3) Parameters guaranteed by characterization.
- 4) Parameters guaranteed by design.

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Digital Timing Characteristics (UT16MX113)^{1,2}

($V_{DD}=5.0V \pm 0.5V$, $V_{DD}=3.3V \pm 0.3V$, $GND=0V$; $-55^{\circ}C \leq T_C \leq +125^{\circ}C$)

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
t_{PROP_S}	Propagation delay of analog input (S[x]) to analog output (COM) measured at 50%	$R_T=50\Omega$ $C_L=50pF$ See Figures 10 & 12			25	ns
t_{PROP_D}	Propagation delay of any changes in the digital inputs (A[3:0], \overline{CS} , PLATCH, \overline{SS}) affecting the analog output (COM)	$R_T=50\Omega$ $C_L=50pF$ See Figures 5 & 12	25		140	ns
t_{MUX}	Mux decoding time	$R_T=50\Omega$ $C_L=50pF$ See Figures 5 & 12			50	ns
t_{BBM}	Break-Before-Make-Delay	$R_T=50\Omega$ $C_L=50pF$ See Figures 5 & 12	15		90	ns
t_{AS1}	The minimum amount of time required for the address signals (A[3:0]) to be stable before the falling edge of \overline{CS}^3	See Figure 5	3.0			ns
t_{AS2}	The minimum amount of time required for the address signals (A[3:0]) to be stable after the rising edge of \overline{CS}^3	See Figure 5	5.0			ns

Notes:

- 1) For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured (see ordering information).
- 2) Continuous operation with low load resistance is not recommended. (See Figure 11)
- 3) Guaranteed by design.

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Digital Timing Characteristics (UT16MX114)^{1,2}

($V_{DD}=5.0V \pm 0.5V$, $V_{DD}=3.3V \pm 0.3V$, $GND=0V$; $-55^{\circ}C \leq T_C \leq +125^{\circ}C$)

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
t_{PROP_S}	Propagation delay of analog input (S[x]) to analog output (COM) measured at 50%	$R_T = 50\Omega$ $C_L = 50pF$ See Figures 10 & 12			25	ns
t_{PROP_D}	Propagation delay of any changes in the digital inputs (A[3:0], \overline{CS} , PLATCH, \overline{SS}) affecting the analog output (COM)	$R_T = 50\Omega$ $C_L = 50pF$ See Figures 6 & 12	25		140	ns
t_{MUX}	Mux decoding time	$R_T = 50\Omega$ $C_L = 50pF$ See Figures 6 & 12			50	ns
t_{BBM}	Break-Before-Make-Delay	$R_T = 50\Omega$ $C_L = 50pF$ See Figures 6 & 12	15		90	ns
t_{PZLH}	Output enable time from HiZ to low or high once \overline{RESET} is pulled high	$R_T = 50\Omega$ $C_L = 50pF$ See Figures 9 & 12			90	ns
t_{PLHZ}	Output disable time from low or high to HiZ once \overline{RESET} is pulled low	$R_T = 50\Omega$ $C_L = 50pF$ See Figures 9 & 12			55	ns
t_{LSU}	Address setup time wrt rising edge PLATCH	$R_T = 50\Omega$ $C_L = 50pF$ See Figures 6 & 12	5.0			ns
t_{LHD}	Address hold time wrt rising edge PLATCH	$R_T = 50\Omega$ $C_L = 50pF$ See Figures 6 & 12	10			ns

Notes:

- 1) For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured (see ordering information).
- 2) Continuous operation with low load resistance is not recommended. (See Figure 11)

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Digital Timing Characteristics (UT16MX115)^{1,2}

($V_{DD}=5.0V \pm 0.5V$, $V_{DD}=3.3V \pm 0.3V$, $GND=0V$; $-55^{\circ}C \leq T_C \leq +125^{\circ}C$)

Symbol	Parameter	Condition	MIN	TYP	MAX	Unit
t_{PROP_S}	Propagation delay of analog input (S[x]) to analog output (COM) measured at 50%	$R_T=50\Omega$ $C_L=50pF$ See Figures 10 & 12			25	ns
t_{PROP_D}	Propagation delay of any changes in the digital inputs (A[3:0], \overline{CS} , PLATCH, \overline{SS}) affecting the analog output (COM)	$R_T=50\Omega$ $C_L=50pF$ See Figures 7 & 12	25		140	ns
t_{MUX}	Mux decoding time	$R_T=50\Omega$ $C_L=50pF$ See Figures 7 & 12			50	ns
t_{BBM}	Break-Before-Make-Delay	$R_T=50\Omega$ $C_L=50pF$ See Figures 7 & 12	15		90	ns
t_{PZLH}	Output enable time from HiZ to low or high once \overline{RESET} is pulled high	$R_T=50\Omega$ $C_L=50pF$ See Figures 9 & 12			90	ns
t_{PLHZ}	Output disable time from low or high to HiZ once \overline{RESET} is pulled low	$R_T=50\Omega$ $C_L=50pF$ See Figures 9 & 12			55	ns
f_{SCLK}	SCLK frequency	See Figure 7			2.0	MHz
t_H	SCLK high time	See Figure 7	190			ns
t_L	SCLK low time	See Figure 7	190			ns
t_{SSU}	First SCLK setup time (for shifting window)	See Figure 7	7.0			ns
t_{SSH}	Last SCLK hold time (for shifting window)	See Figure 7	10			ns
t_{SU}	Data In (MOSI) setup time wrt rising edge SCLK	See Figure 7	3.0			ns
t_{HD}	Data In (MOSI) hold time wrt rising edge SCLK	See Figure 7	5.0			ns
t_{DO}	Data out (MISO) valid (after falling edge of SCLK)	$C_L=50pF$ See Figure 7			43	ns
t_{DR}	Data out (MISO) rise time	10-90% V_{DD} $C_L=50pF$			30	ns
t_{DF}	Data out (MISO) fall time	10-90% V_{DD} $C_L=50pF$			20	ns

Notes:

- 1) For devices procured with a total ionizing dose tolerance guarantee, the post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to the maximum TID level procured (see ordering information).
- 2) Continuous operation with low load resistance is not recommended. (See Figure 11)

Analog Multiplexer

UT16MX113/114/115

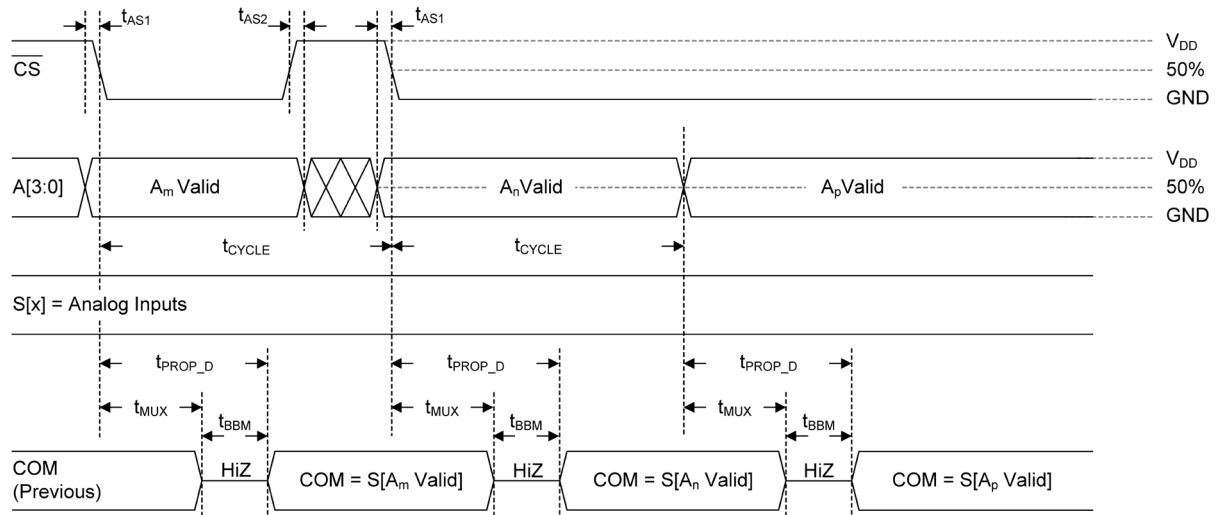
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Timing Diagrams

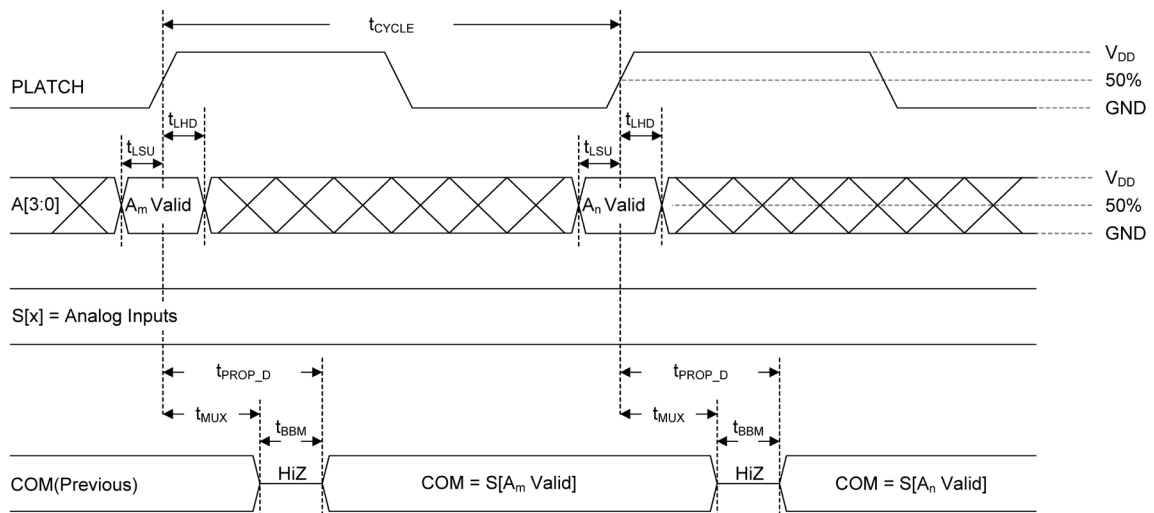
Multiplexer Asynchronous Parallel Timing (UT16MX113)



Notes:

- 1) \overline{CS} may be held in a continuous low state, holding \overline{CS} high provides protection for false address change.
- 2) t_{CYCLE} is the minimum cycle time between the falling edges of \overline{CS} and/or any address changes. If t_{CYCLE} is shorter than t_{PROP_D} , an addressing error may occur.
- 3) All bits ($A[3:0]$) of any address change should be received by the UT16MX113 within 18ns of the first bit change for proper operation.

Multiplexer Synchronous Parallel Timing (UT16MX114)



Notes:

- 1) When $PLATCH$ is in a high or low state, it provides protection for false address change.
- 2) t_{CYCLE} must not be less than the maximum value of t_{PROP_D} .

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Multiplexer Serial Timing (UT16MX115)

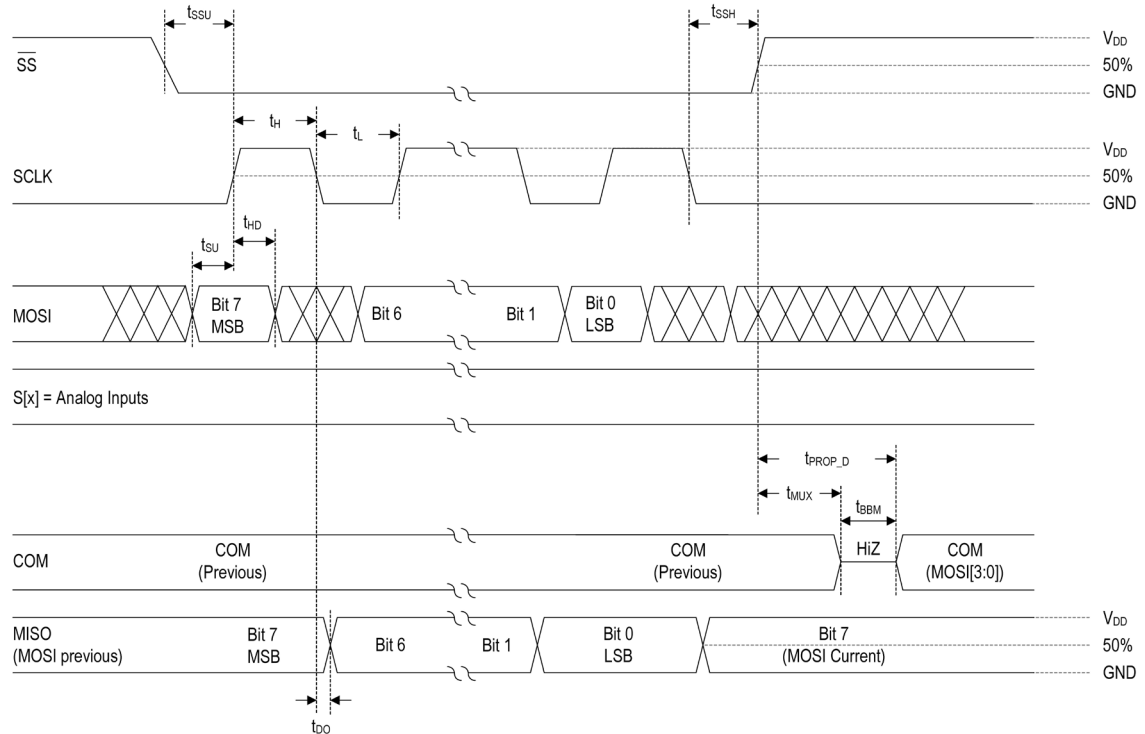


Figure 7. UT16MX115 Timing Diagram

Multiplexer Load Conditions for Test (UT16MX113/114/115)

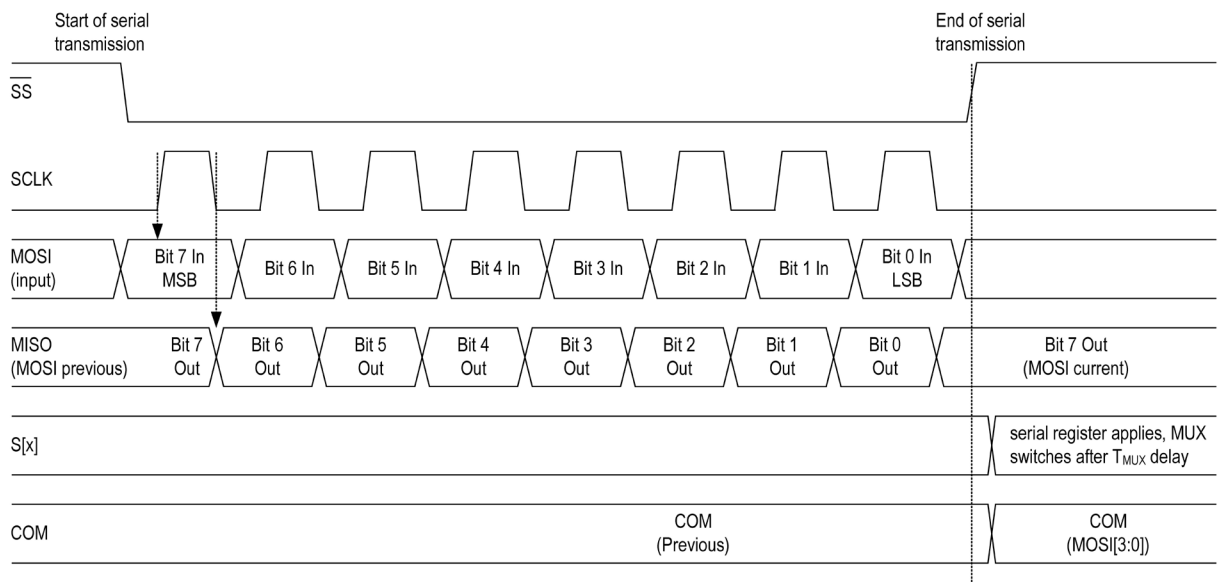


Figure 8. SPI™ Protocol

Note:

- 1) See FIGURE 7. Multiplexer serial timing (UT16MX115), for detailed timing.

UT16MX113/114/115

Multiplexer $\overline{\text{RESET}}$ Enable/Disable Timing (UT16MX114/115)

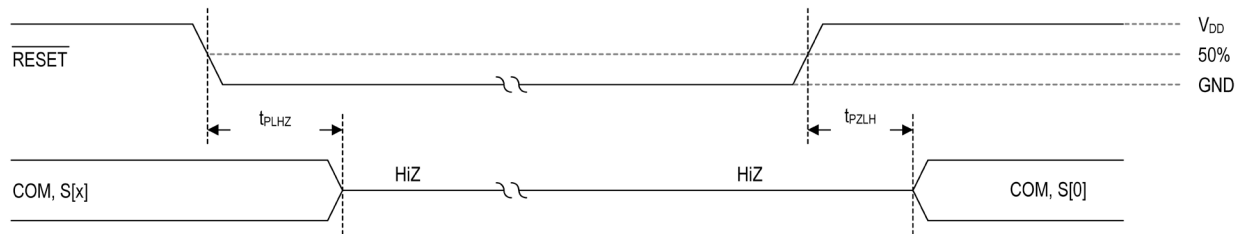


Figure 9: $\overline{\text{RESET}}$ Timing Diagram (Used for UT16MX114/115 only)

Note:

- 1) S[x] represents the analog signal channel connected to COM prior to the falling edge of $\overline{\text{RESET}}$.

Multiplexer Analog Timing (UT16MX113/114/115)

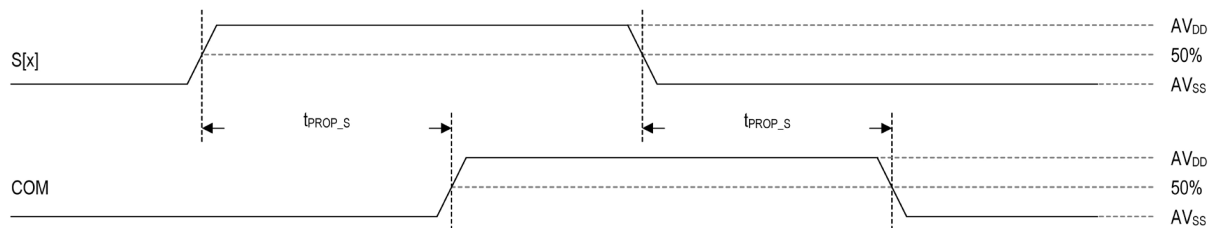


Figure 10. Analog Timing Diagram (Used for UT16MX113/114/115)

Note:

- 1) S[x] represents the analog signal channel connected to COM while in active mode of all device types with the address already set and all digital inputs held constant.

UT16MX113/114/115

Minimum Multiplexer Total Path Resistance (UT16MX113/114/115)

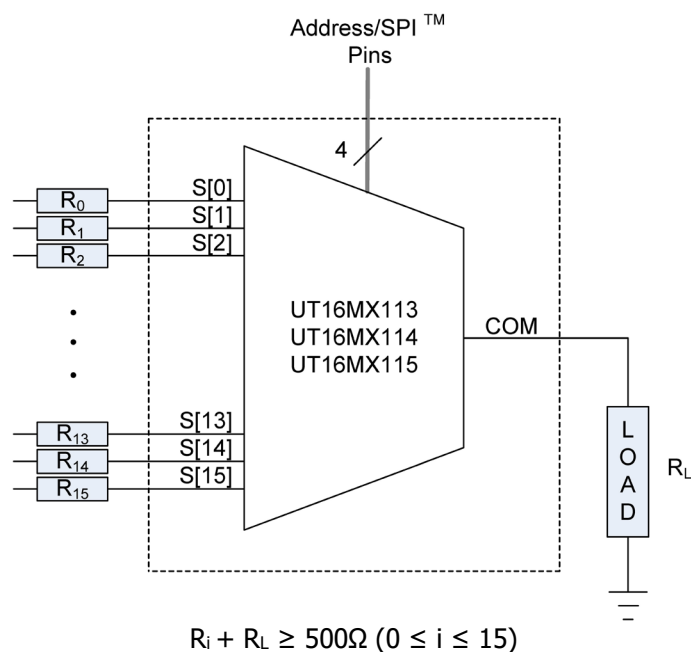


Figure 11. Minimum Total Path Resistance for Continuous DC Operation on Any Single Channel

Note:

- 1) Continuous DC operation on any single channel where $R_i + R_L < 500\Omega$ will degrade device reliability and performance.

Multiplexer Load Conditions for Test (UT16MX113/114/115)

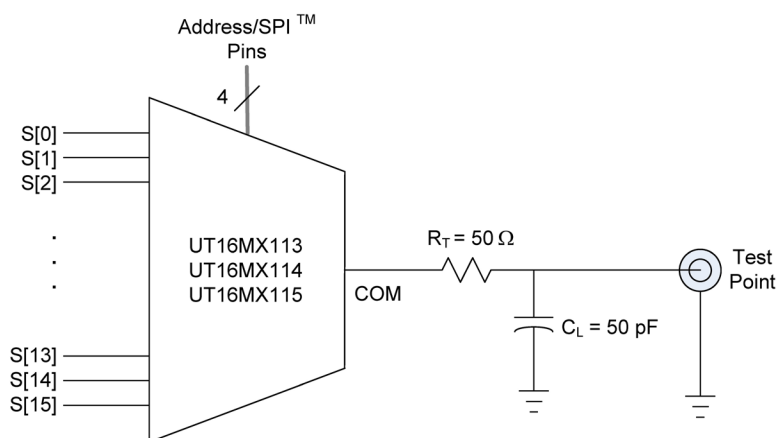
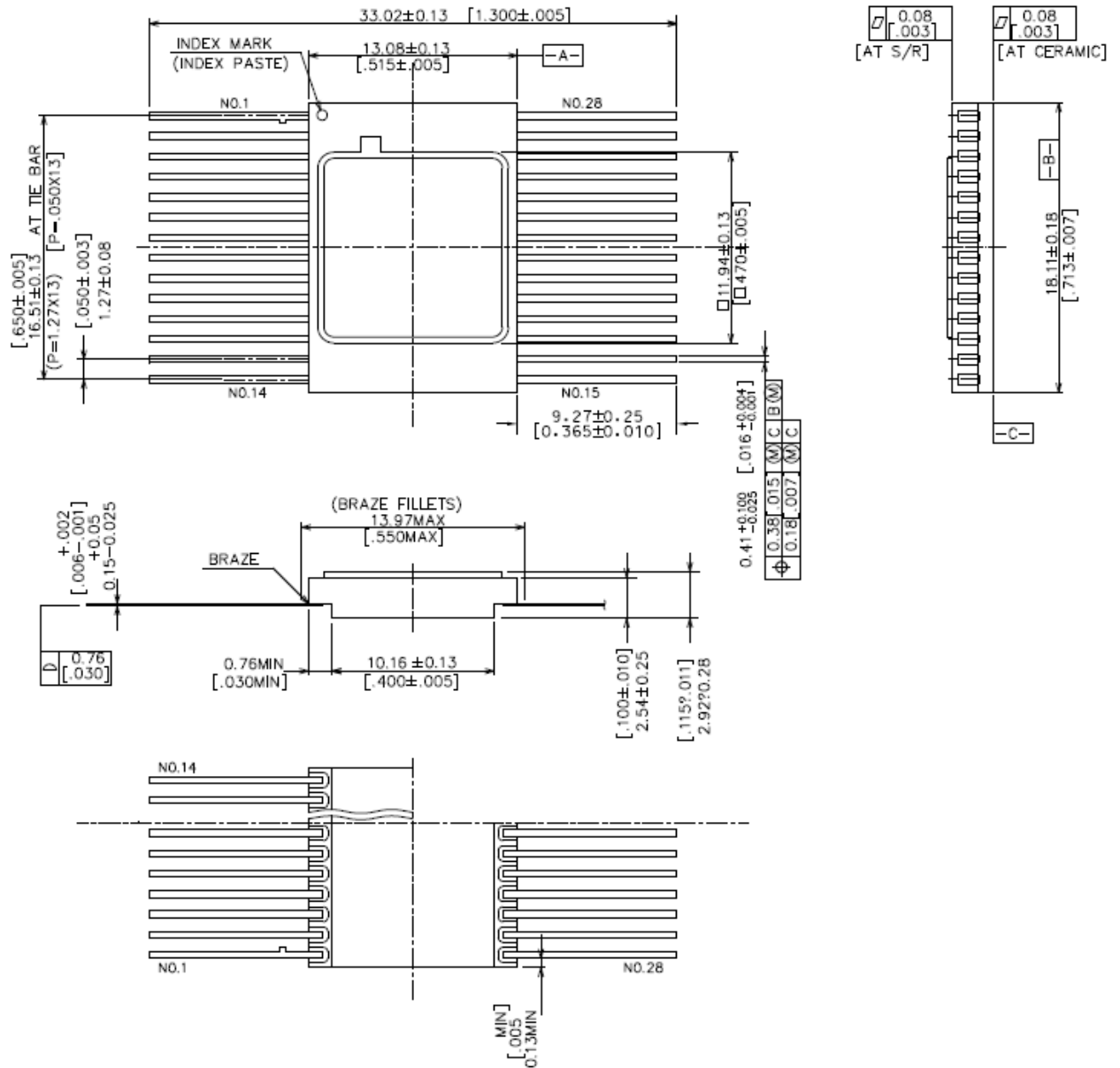


Figure 12. UT16MX113/114/115 Test Circuit

Analog Multiplexer

UT16MX113/114/115

Packaging



Notes:

- 1) Gold plated 100 to 225 microinches over electroplated nickel 100 to 350 microinches per MIL-PRF-38535
- 2) Seal ring is electrically connected to VSS

Analog Multiplexer

UT16MX113/114/115

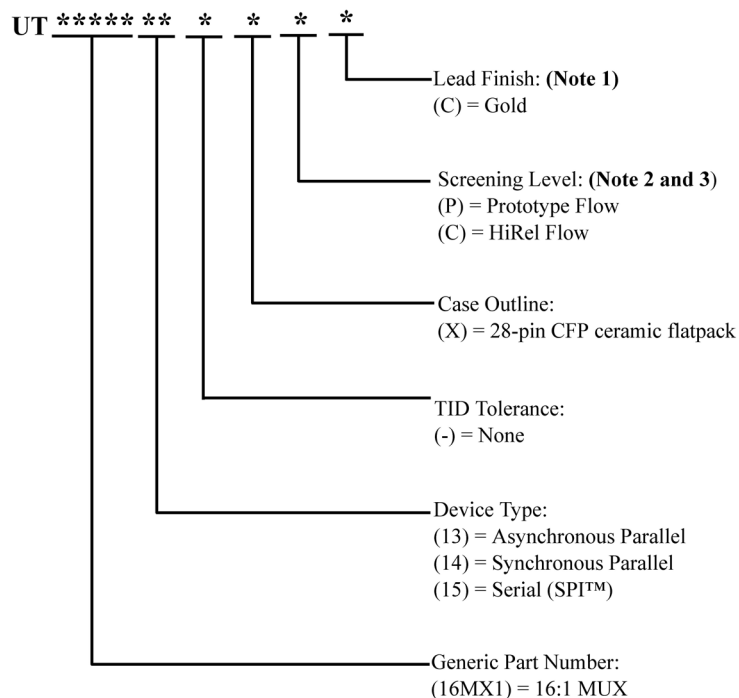
Trademarks:

SPI™ /QSPI™ are trademarks of Motorola, Inc.

MICROWIRE™ is a trademark of National Semiconductor

Ordering Information

UT16MX113/114/115 Analog Multiplexer

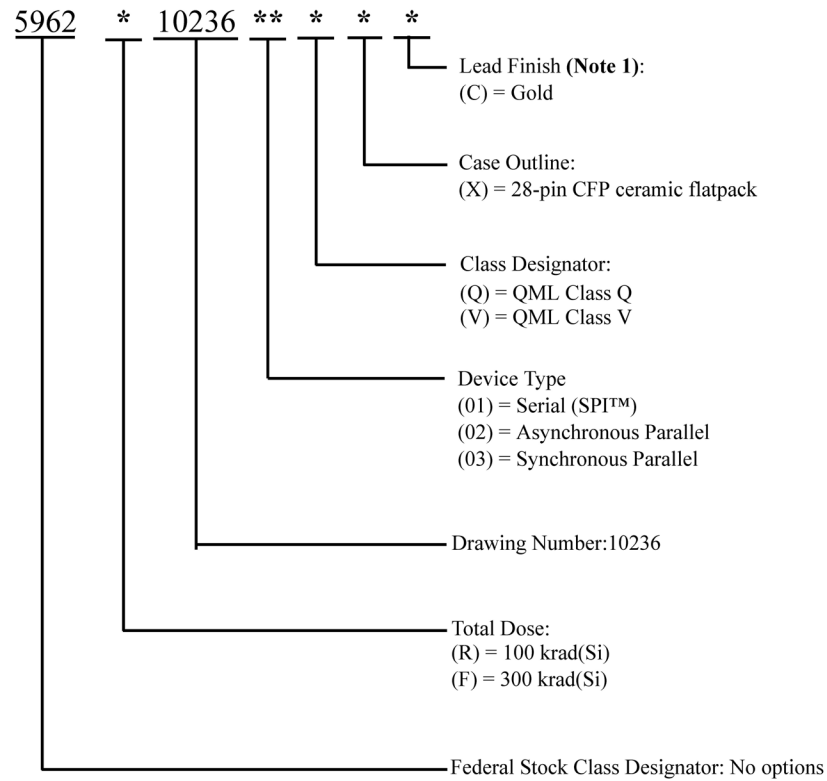


Notes:

- 1) Lead finish is "C" (Gold) only.
- 2) Prototype flow per CAES Manufacturing Flows Document. Tested at 25°C only. Lead finish is Gold "C" only. Radiation neither tested nor guaranteed.
- 3) HiRel Flow per CAES Manufacturing Flows Document.

UT16MX113/114/115

UT16MX113/114/115 Analog Multiplexer: SMD

**Note:**

- 1) Lead finish is "C" (Gold) only.

Datasheet Revision History

2-29	Page 2: Functional Description edits UT16MX113: <u>UT16MX113 requires the following operation in order to properly initialize the part following power-up: All address states for the A[3:0] address lines must be exercised following AVDD power-up to ensure correct addressing. Once this operation has been completed, normal asynchronous addressing can then be used to select the desired input channel (i.e. one of S[15:0]) to connect to the COM output. The S[15:0] analog channels are routed asynchronously via the binary decoding of A[3:0] static logic levels after initialization.</u>	BM
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Analog Multiplexer

UT16MX113/114/115

Datasheet Definitions

	DEFINITION
Advanced Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet is subject to change . Specifications can be TBD and the part package and pinout are not final .
Preliminary Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

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