Octal Bus Transceiver, Bidirectional Voltage Level Shifter

RHD5980

Features

- Bidirectional Voltage translator with two separate supply rails.
- Radiation performance
 - Total dose: >1 Mrad(Si); Dose rate = 50-300 rad(Si)/s
 - ELDRS Immune
 - SEL Immune >100 MeV-cm²/mg
 - Neutron Displacement Damage >10¹⁴ neutrons/cm²
- Full military temperature range
- Designed for aerospace and high reliability space applications
- Packaging Hermetic ceramic SOIC
 - 24-pin, .614"L x .300"W x .120"Ht
 - Weight 2.0 grams max
- Radiation Hardness Assurance Plan: DLA Certified to MIL-PRF-38534, Appendix G.

General Description

The RHD5980 is a radiation hardened, Octal Level Shifter in a 24-pin SOIC package. The RHD5980 design uses specific circuit topology and layout methods to mitigate total ionizing dose effects and single event latchup. These characteristics make the RHD5980 especially suited for the harsh environment encountered in Deep Space missions. It is guaranteed operational from -55°C to +125°C. Available screened in accordance with MIL-PRF-38534 Class K, the RHD5980 is ideal for demanding military and space applications.

Organization and Application

The RHD5980 Octal Level Shifter is a radiation hard replacement for the industry standard Bidirectional Voltage Translators. It is capable of level shifting from the A-to-B or B-to-A input ports for nominal logic voltages on either port of 5.0 or 3.3 volts.

The RHD5980 can level shift from 5.0V to 3.3V or 3.3V to 5.0V, and also buffer from 5.0V to 5.0V or 3.3V to 3.3V. Ports A and B can be inputs or outputs depending on the value of DIR_AB_H.

Control inputs are the standard tri-state enable (OE_L active low) and direction control DIR_AB_H where a HIGH logic steers data from A-to-B and active LOW steers the data from B-to-A.

The control inputs are powered from V_{CCA} and accept inputs at the A bus logic levels (either 3.3V or 5.0V). All delay parameters are less than 30nS over full -55°C to +125°C military temperature range and logic levels. All bus and control inputs have Schmitt trigger buffers to implement low-to-high transition at approximately 60% of the corresponding logic supply and high-to-low transition at approximately 40% providing considerable noise immunity for slow input signals.

The devices will not latch with SEU events to above 100 MeV-cm²/mg. Total dose degradation is minimal to above 1 Mrad(Si). Displacement damage environments to neutron fluence equivalents in the mid 10¹⁴ neutrons per cm² range are readily tolerated. There is no sensitivity to low-dose rate (ELDRS) effects. SEU effects are application dependent.



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Absolute Maximum Ratings

Parameter	Range	Units
Case Operating Temperature Range	-55 to +125	°C
Storage Temperature Range	-65 to +150	°C
Junction Temperature	+150	°C
Supply Voltage +V _{CCA} , +V _{CCB}	+7.0	V
Input Voltage	V _{CC} +0.4 GND -0.4	V V
Lead Temperature (soldering, 10 seconds)	300	°C
Power @ 25°C	250	mW
Thermal Resistance, Junction-to-Case, ⊕JC	5	°C/W

Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress rating only; functional operation beyond the "Operation Conditions" is not recommended and extended exposure beyond the "Operation Conditions" may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Typical	Units
+V _{CCA} , +V _{CCB}	Power Supply Voltage	3.3 to 5.0	V

Electrical Performance Characteristics

(TC = -55°C TO +125°C, V_{CCA} = 5.5 V, V_{CCB} = 3.6 V -- Unless Otherwise Specified)

Parameter	Symbol	Conditions		MIN	MAX	Units
	PORT A					
Quiescent Supply Current	I _{CCA}	V _{IN} = 5.5 V or GND, No Load			20	uA
Quiescent Supply Current Delta	ΔI_{CCA}	One input at 3.4 V, Other inputs at 5.5 V or GND			1.5	mA
High Level Output Voltage		T 100 - A	V _{CCA} = 4.5 V	4.3		V
Thigh Level output voltage	W	I _{OH} = -100 uA	$V_{CCA} = 5.5 \text{ V}$	5.3		
	V _{OH}		$V_{CCA} = 4.5 \text{ V}$	3.7		
		$I_{OH} = -12 \text{ mA}$	$V_{CCA} = 5.5 \text{ V}$	4.7		
Low Level Output Voltage		$I_{OL} = 100 \text{ uA}$	$V_{CCA} = 4.5 \text{ V}$		0.2	- V
Low Level Galpat Voltage	V		$V_{CCA} = 5.5 \text{ V}$		0.2	
Vol	VOL	I 12 A	$V_{CCA} = 4.5 \text{ V}$		0.55	
		$I_{OL} = 12 \text{ mA}$ $V_{CCA} = 5$			0.55	
Three-state I/O Leakage Current High 2/	I _{IOH}	V _{IN} = 5.5 V		-500	500	nA
Three-state I/O Input Leakage Current Low 2/	I _{IOL}	$V_{IN} = GND$		-500	500	nA



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Electrical Performance Characteristics (Cont.)

($T_C = -55$ °C TO +125°C, $V_{CCA} = 5.5$ V, $V_{CCB} = 3.6$ V -- Unless Otherwise Specified)

Parameter	Symbol	Conditions		MIN	MAX	Units
PORT B						
Quiescent Supply Current	I_{CCB}	V _{IN} = 3.6 V or GND, No Load			15	uA
Quiescent Supply Current Delta	ΔI_{CCB}	One input at 2.7 V to 3.6 V - 0.6 V, Other inputs at 2.7 V to 3.6 V or GND			50	uA
		I _{OH} = -100 uA	$V_{CCB} = 2.7 \text{ V to } 3.6 \text{ V}$	V _{CCB} -0.2		
High Level Output Voltage	V_{OH}		$V_{CCB} = 2.7 \text{ V}$	2.2		V
		$I_{OH} = -12 \text{ mA}$	$V_{CCB} = 3.0 \text{ V}$	2.4		
		I _{OH} = 100 uA	$V_{CCB} = 2.7 \text{ V to } 3.6 \text{ V}$		0.2	
Low Level Output Voltage	V_{OL}	I _{OH} = 12 mA	$V_{CCB} = 2.7 \text{ V}$		0.55	V
		10H = 12 IIIA	$V_{CCB} = 3.0 \text{ V}$		0.55	
Three-state I/O Leakage Current High 2/	${ m I}_{ m IOH}$	V _{IN} = 3.6 V		-500	500	nA
Three-state I/O Input Leakage Current Low 2/	${ m I}_{ m IOL}$	$V_{IN} = GND$		-500	500	nA
		Switching				
Pro[agation Delay Time A to	t_{PHL}	$V_{CCA} = 4.5 \text{ V to } 5.5 \text{ V, } V_{CCB} = 2.7 \text{ V to } 3.6 \text{ V, } C_L = 50 \text{pF}$		1	20	ns
В	t_{PLH}			1	20	ns
Propagation Delay Time B	t _{PHL}			1	20	ns
to A	t _{PLH}			1	20	ns
Propagation Delay Time,	t_{PZL}			1	30	ns
Output Enabled OE_L to A	t _{PZH}			1	30	ns
Propagation Delay Time,	t _{PZL}			1	30	ns
Output Enabled OE_L to B	t _{PZH}			1	30	ns
Propagation Delay Time, Output Disabled	t_{PLZ}			1	30	ns
OE_L to A	•			1	30	ns
Propagation Delay Time,	t_{PLZ}	1		1	30	ns
Output Disabled OE_L to B	t _{PHZ}			1	30	ns

Notes:

- 1) Specification derated to reflect Total Dose exposure to 1 Mrad(Si) @ 25°C.
- 2) These parameters for Tc = -55°C are guaranteed by design, characterization, or correlation to other test parameters.



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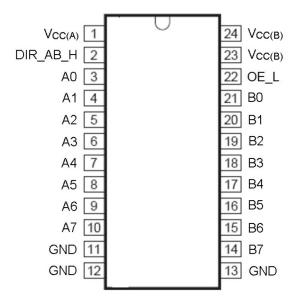


Figure 1: Package Pin-Out

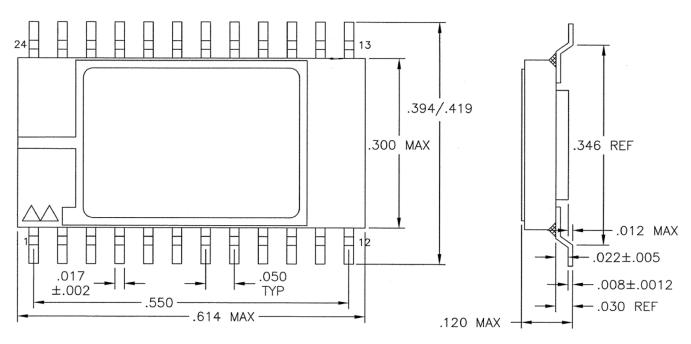


Figure 2: Package Outline

Note: Package and lid are electrically isolated from signal pads.



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Ordering Information

Model	DLA SMD #	Screening	Package
RHD5980-7	-	Commercial Flow, +25°C testing only	
RHD5980-201-1S	5962-1222601KXC	In accordance with DLA SMD	24
RHD5980-201-2S	5962-1222601KXA	In accordance with DLA SIND	24-pin SOIC Package
RHD5980-901-1S	5962H1222601KXC	In accordance with DLA Certified RHA	Jose Facility
RHD5980-901-2S	5962H1222601KXA	Program Plan to RHA Level "H", 1 Mrad(Si)	

Revision History

Date	Revision	Change Description
03/28/2016	В	Import into CAES format





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Datasheet Definitions

Datastreet Definitions				
	DEFINITION			
Advanced Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet is subject to change. Specifications can be TBD and the part package and pinout are not final .			
Preliminary Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.			
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.			

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