DATASHEET

REV C: 3/15/21

SCD5958

8-Channel Multiplexed, 14-Bit, Analog-to-Digital Converter

RHD5958

Features

- Single power supply operation 5.0V or Dual power supply for 3.3V I/O
- Radiation performance
  - Total dose: > 100 krad(Si); Dose rate = 50-300 rad(Si)/s
  - ELDRS Immune
  - SEL Immune > 100 MeV-cm^2/mg
  - Neutron Displacement Damage > 10^{14} neutrons/cm^2
- 8-Channel Input Multiplexer
- Successive Approximation A-to-D
- Level Shifting Digital Output Drivers allow interfaces to 5.0 or 3.3 volt logic
- Tri-State digital outputs
- Power Down (Sleep) mode
- Single or continuous conversion
- 20us conversion period (20 clocks @ 1MHz Clock rate)
- Multiplexer address is latched on first clock rising edge of a cycle
- Busy and End-of-Conversion status outputs
- Full military temperature range
- Designed for aerospace and high reliability space applications
- Packaging – Hermetic Ceramic
  - 40 leads, 0.600"Sq x 0.120"Ht quad flat pack
  - Weight - 6 grams max
- **Radiation Hardness Assurance Plan: DLA Certified to MIL-PRF-38534, Appendix G.**

General Description

The RHD5958 is a radiation hardened, single supply, 8-Channel Multiplexed Analog-to-Digital converter in a 40-pin Ceramic Quad Flat Package. The RHD5958 design uses specific circuit topology and layout methods to mitigate total ionizing dose effects and single event latchup. It is guaranteed operational from -55°C to +125°C. Available screened in accordance with MIL-PRF-38534 Class K, the RHD5958 is ideal for demanding military and space applications.

Organization and Application

The RHD5958 takes 8 analog sensor signals and using 3 address inputs and an enable input, selects one of the 8 analog inputs and performs a 14-bit successive approximation analog-to-digital conversion in a nominal period of 20 clock cycles (20uS nominal). The 14-bit digital output has a tri-state control allowing the connection of multiple RHD5958s. This provides the ability to interface many sensor voltage readings to the digital processor data bus. The full-scale range is determined by reference input voltages. The input impedance of the reference/span terminals is typically a constant 4K ohms.

Gain compression will occur near either power supply extremes but can be avoided if the references are more than 200mV away from the respective supply terminals. The input span can be less than 4 volts at the expense of ultimate resolution

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The analog channel's input impedance is primary capacitance (20pF typical). The input voltage charges a Sample-&-Hold hold capacitor through transmission gates. The input bandwidth is determined by the slew rate of the hold amplifier and is adequate to allow input sampling in three clock periods (3uS nominal). The ultimate bandwidth is determined by the aperture uncertainty associated with the closing of the sample gate (approximately 5nS). The converter bandwidth is then determined by the sampling Nyquist frequency rather than the input signal; change rate (dv/dt) and the LSB weight in volts as would be the case if there were no Sample-&-Hold.

Start-Convert (STCNV_H), Busy (BUSY_L) and End-Of-Convert (EOC_H) status and control lines are provided. The converter will operate in either continuous or single conversion modes. To operate in continuous mode, STCNV_H should be tied to BUSY_L. The digital output register changes at the end of a conversion and is latched when EOC_H is asserted High. The output data will remain latched until the next conversion is complete and will be updated when EOC_H is asserted High. The output circuitry operates from a voltage independent of the remainder of the chip such that I/O is compatible with digital systems from, less than 3.3 volts, to 5 volts.

The converter divides the reference voltage into 16 segments with a linear weighted resistor network. The voltage on any segment is passed to a linear 10-bit DAC for interpolation. The sampled input voltage is compared to the output of the two stage DAC for a 14-bit successive approximation conversion.

All inputs are protected to both power supply rails by semiconductor diodes. Inputs should be constrained to V_{CC}+0.4 and GND-0.4 to avoid forward biasing protection paths. See figure 1.

The devices will not latch with SEU events to above 100 MeV-cm^2/mg. Displacement damage environments to neutron fluence equivalents in the mid 10^{14} neutrons per cm^2 range are readily tolerated. There is no sensitivity to low-dose rate (ELDRS) effects. SEU effects are application dependent.

Notes:

1) The STCNV_H is a dynamic input and should not be tied to a static voltage. See application note.
2) The input signals should be low pass filtered to reduce high frequency noise
3) If Sleep mode is enabled (EN_H=0), when waking up (EN_H=1), the unit has to complete an entire conversion cycle so the digital logic is in the proper state.
   Ex. If using a 1MHz clock; after EN_H=1 and 20us after STCNV_H is applied.

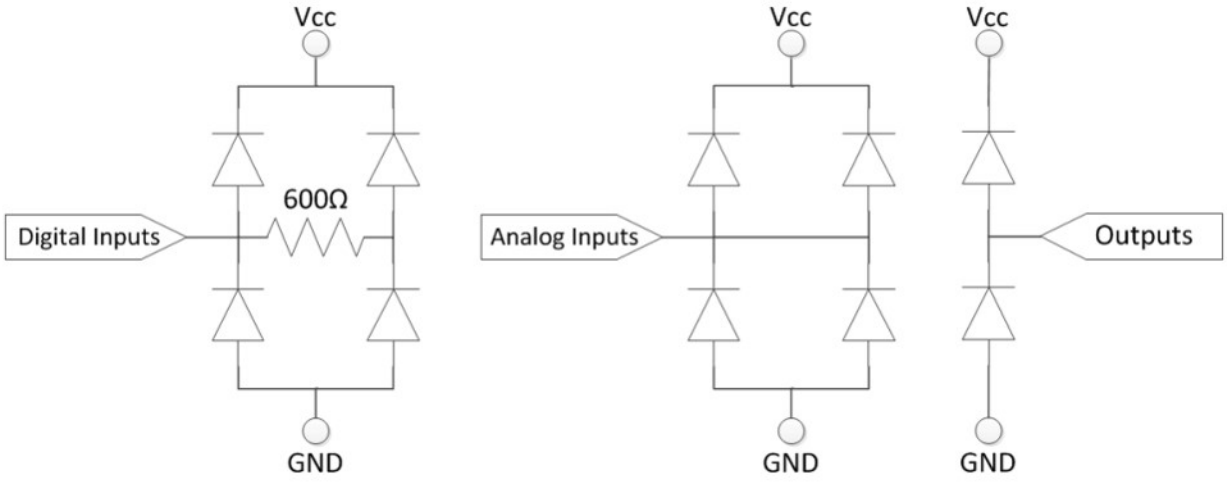

Figure 1: Diode Protection Circuits Diagram

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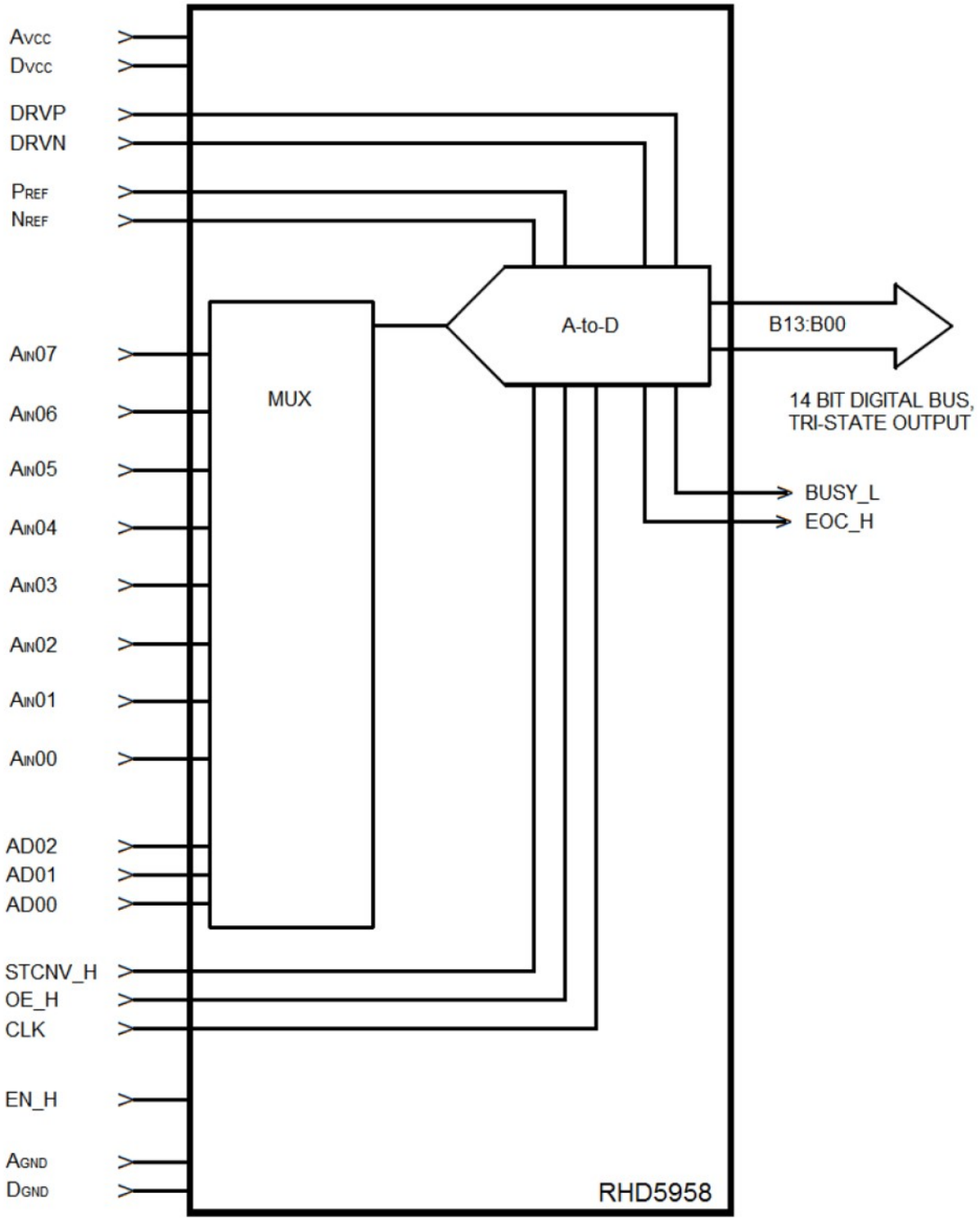

Figure 2: Block Diagram

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Absolute Maximum Ratings

Parameter	Range	Units
Case Operating Temperature Range	-55 to +125	°C
Storage Temperature Range	-65 to +150	°C
Junction Temperature	+150	°C
Supply Voltage V_{CC} - GND	+7.0	V
Input Voltage, PREF, NREF	V_{CC} +0.4 GND -0.4	V
Lead Temperature (soldering, 10 seconds)	300	°C
Thermal Resistance, Junction to Case, Θjc	2.0	°C/W

Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress rating only; functional operation beyond the "Operation Conditions" is not recommended and extended exposure beyond the "Operation Conditions" may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Typical	Units
$+A_{VCC}$	Analog Power Supply Voltage	5.0	V
$+D_{VCC}$	Digital Power Supply Voltage	5.0	V
DRVP	Digital Output High Reference Level	3.3 to 5.0	V
DRVN	Digital Output Low Reference Level	0	V
PREF	High Analog Reference Voltage	4.5	V
NREF	Low Analog Reference Voltage	0.5	V

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Electrical Performance Characteristics

(Tc = -55°C to +125°C, $+A_{VCC}$ = +5.0 V, $+D_{VCC}$ = +5.0 V, +DRVP = +5.0 V, unless stated otherwise)

Parameter	Symbol	Conditions	MIN	MAX	Units
Analog Supply Current Quiescent 1/	AI_{CCQ}	$V_{EN} = D_{VCC}$, $V_{OE} = D_{VCC}$, CLK = D_{GND}	-	10	mA
Analog Supply Current Active 1/	AI_{CCA}	$V_{EN} = D_{VCC}$, $V_{OE} = D_{VCC}$	-	10	mA
Analog Supply Current Sleep 1/	AI_{CCS}	$V_{EN} = D_{GND}$, $V_{OE} = D_{GND}$	-	4	mA
Digital Supply Current Quiescent 1/	DI_{CCQ}	$V_{EN} = D_{VCC}$, $V_{OE} = D_{VCC}$, CLK = D_{GND}	-	1	mA
Digital Supply Current Active 1/	DI_{CCA}	$V_{EN} = D_{VCC}$, $V_{OE} = D_{VCC}$	-	2	mA
Digital Supply Current Sleep 1/	DI_{CCS}	$V_{EN} = D_{GND}$, $V_{OE} = D_{GND}$	-	1	mA
Digital Output Supply Current Quiescent 1/	$05I_{CCQ}$	$V_{EN} = D_{VCC}$, $V_{OE} = D_{VCC}$, CLK = D_{GND}, C_L = 50 pF	-	0.1	mA
Digital Output Supply Current Active 1/	$05I_{CCA}$	$V_{EN} = D_{VCC}$, $V_{OE} = D_{VCC}$, C_L = 50 pF	-	1	mA
Digital Output Supply Current Sleep 1/	$05I_{CCD}$	$V_{EN} = D_{VCC}$, $V_{OE} = D_{GND}$, C_L = 50 pF	-	1	mA
Full-scale Input Range 1/	V_{IN}		V_{NREF}	V_{PREF}	V
Input Capacitance 2/	C_{IN}	T_C = +25°C	-	50	pF
Analog Reference Impedance 1/	Z_{REF}	PREF to NREF	2	6	KΩ
High Analog Reference Voltage	V_{PREF}	DVRP = 5.0 V 1/	V_{NREF}	5.0	V
		DVRP = 3.3 V 2/			
Low Analog Reference Voltage	V_{NREF}	DVRP = 5.0 V 1/	0	V_{PREF}	
		DVRP = 3.3 V 2/			
Channel Isolation 2/	ISO	T_C = +25°C	80	-	dB

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Electrical Performance Characteristics

(T_C = -55°C to+125°C, +A_{VCC} = +5.0 V, +D_{VCC} = +5.0 V, +DRVP = +5.0 V, unless stated otherwise)

Parameter	Symbol	Conditions		MIN	MAX	Units
Integral Nonlinearity 1/	INL	PREF-NREF = 4.0 V		-48	48	LSBs
Differential Nonlinearity 1/	DNL	PREF-NREF = 4.0 V		-8.2	8.2	LSBs
Offset Error 1/	O_E	PREF-NREF = 4.0 V		-1	1	%FSR
Gain Error 1/	A_E	PREF-NREF = 4.0 V		-2	2	%FSR
Clock Frequency 1/	f_C	PREF-NREF = 5.0 V		-	1	MHz
Maximum Sampling Rate 2/	$f_{SAMPLE\ (MAX)}$	f_C = 1 MHZ, 20 clocks per conversion		-	50	kSPS
High Input Leakage Current (AIN00-AIN07) 1/ 4/	$I_{INLK_{HI}}$	Input under test = A_{VCC}, V_{EN} = DV_{CC}	+25°C	-5	5	nA
			+125°C	-50	50	
Low Input Leakage Current (AIN00-AIN07) 1/ 4/	$I_{INLK_{LO}}$	Input under test = A_{GND}, V_{EN} = DV_{CC}	+25°C	-5	5	nA
			+125°C	-50	50	
Digital High Level Input Voltage EN_H, STCNV_H, OE_H, CLK, (AD00-AD02)	V_{IH}	DVRP = 5.0 V 1/		3.5	-	V
		DVRP = 3.3 V 2/		2.31	-	
Digital Low Level Input Voltage EN_H, STCNV_H, OE_H, CLK, (AD00-AD02)	V_{IL}	DVRP = 5.0 V 1/		-	1.5	V
		DVRP = 3.3 V 2/		-	0.99	
Digital High Level Input Current EN_H, STCNV_H, OE_H, CLK, (AD00-AD02) 1/ 3/	I_{IH}	Digital input under test = 5.0 V All other digital inputs = D_{GND}	+25°C	-5	5	nA
			+125°C	-50	50	
Digital Low Level Input Current EN_H, STCNV_H, OE_H, CLK, (AD00-AD02) 1/ 3/	I_{IL}	All digital inputs = D_{GND}	+25°C	-5	5	nA
			+125°C	-50	50	
Digital High Level Output Voltage (B00-B13) 1/	V_{OH}	DVRP = 5.0 V, V_{EN} = D_{VCC}, I_{OH} = -4.0 mA		4.2	-	V
		DVRP = 3.3 V, V_{EN} = D_{VCC}, I_{OH} = -4.0 mA		2.7	-	
Digital Low Level Output Voltage (B00-B13) 1/	V_{OL}	DVRP = 5.0 V, V_{EN} = D_{VCC}, I_{OL} = +4.0 mA	-55°C, +25°C	-	0.6	V
			+125°C	-	0.8	
		DVRP = 3.3 V, V_{EN} = D_{VCC}, I_{OL} = +4.0 mA	-55°C, +25°C	-	0.6	
			+125°C	-	0.8	
Digital High Level Output Current (B00-B13) 1/	$I_{OH\ (SOURCE)}$	DVRP = 5.0 V, V_{EN} = V_{IH}		-	-4.0	mA
		DVRP = 3.3 V, V_{EN} = V_{IH}		-	-4.0	
Digital Low Level Output Current (B00-B13) 1/	$I_{OL\ (SINK)}$	DVRP = 5.0 V, V_{EN} = V_{IH}		-	4.0	
		DVRP = 3.3 V, V_{EN} = V_{IH}		-	4.0	
High Output Leakage Current (B00-B13) 1/ 4/	$I_{OUTLK_{HI}}$	V_{OE} = D_{GND}	+25°C	-5	5	nA
			+125°C	-50	50	
Low Output Leakage Current (B00-B13) 1/ 4/	$I_{OUTLK_{LO}}$	V_{OE} = D_{GND}	+25°C	-5	5	nA
			+125°C	-50	50	

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Notes:

1) Specification derated to reflect Total Dose exposure to 100 krad(Si) @ +25°C.
2) Not tested. Shall be guaranteed by design, characterization, or correlation to other test parameters.
3) These parameters for Tc = -55°C are guaranteed by design, characterization, or correlation to other test parameters.
4) This test condition was used during Radiation Lot Acceptance Testing (RLAT), but not production tested

Switching Characteristics

(T_C = -55°C to +125°C, +A_{VCC} = +5.0 V, +D_{VCC} = +5.0 V)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
STCNV_H to CLK Setup	t_{ST-CLK}	DVRP = 5.0v, Freq = 1MHz	20	-	900	ns
ADDRESS to CLK Setup 1/	$t_{ADR-CLK}$	DVRP = 5.0v, Freq = 1MHz	20	-	14,000	ns
CLK to BUSY_L High	$t_{CLK-BUSY\_H}$	DVRP = 5.0v, Freq = 1MHz, C= 30pF, No Load	10	50	150	ns
CLK to BUSY_L Low	$t_{CLK-BUSY\_L}$	DVRP = 5.0v, Freq = 1MHz, C= 30pF, No Load	10	50	150	ns
CLK to EOC_H High	$t_{CLK-EOC\_H}$	DVRP = 5.0v, Freq = 1MHz, C= 30pF, No Load	10	50	150	ns
CLK to EOC_H Low	$t_{CLK-EOC\_L}$	DVRP = 5.0v, Freq = 1MHz, C= 30pF, No Load	10	50	150	ns
EOC_H to OUTPUT DATA 2/	$t_{EOC-DATA}$	DVRP = 5.0v, Freq = 1MHz, C = 30pF, R_L = 4mA	5	10	25	ns
		DVRP = 3.3v, Freq = 1MHz, C = 30pF, R_L = 4mA				
CLK period	t_{CLK}	DVRP = 3.3v - 5.0v	1	-	-	us
CLK Pulse Width	t_{CLK_H}, t_{CLK_L}	DVRP = 3.3v - 5.0v	50	-	-	ns
CLK rise/fall time	$t_{CLK\_R/F}$	DVRP = 3.3v - 5.0v	-	-	15	ns
OE_H to OUTPUT DATA			-	-	25	ns

Notes:

1) The address is latched after the 3rd clock but should be held for at least 6 clock cycles after the STCNV_H is clocked in for margin, to ensure the Sample-and-Hold gate is closed. The Sample-and-Hold gate closes between 3 to 5 clock cycles. The max limit is associated with Continuous Mode operation.
2) Data is latched on the rising edge of EOC_H

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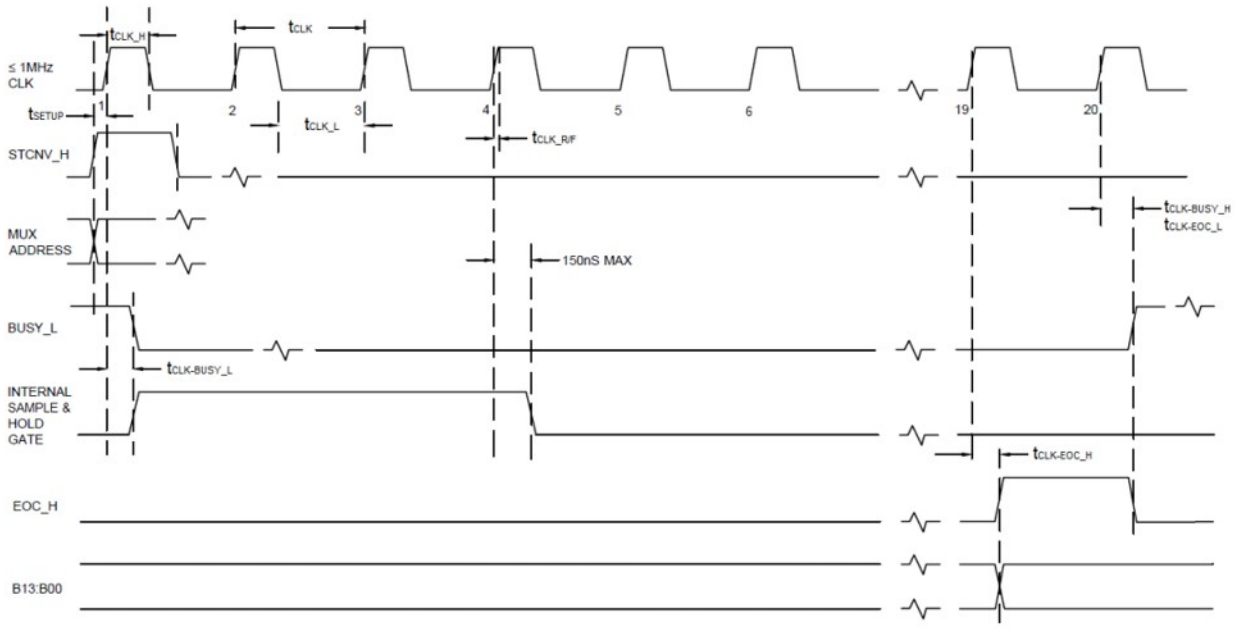

Figure 3: Basic Timing Diagram

Pin #	Signal	Definition	Pin #	Signal	Definition
1	A_{VCC}	Analog Supply Voltage	21	B10	Digital Output 10
2	D_{VCC}	Digital Supply Voltage	22	B11	Digital Output 11
3	AD02	Multiplexer Address 02	23	B12	Digital Output 12
4	AD01	Multiplexer Address 01	24	B13	Digital Output 13
5	AD00	Multiplexer Address 00	25	EOC_H	End of Convert
6	CASE	Case Ground	26	BUSY_L	Busy
7	STCNV_H	Start Conversion	27	DRVN	Digital Output Low Reference Level
8	EN_H	Multiplexer Enable	28	DRVP	Digital Output High Reference Level
9	OE_H	Output Enable	29	D_{GND}	Digital Supply Return
10	CLK	Clock Input	30	A_{GND}	Analog Supply Return
11	B00	Digital Output 00	31	PREF	High Analog Reference Voltage
12	B01	Digital Output 01	32	AIN07	Analog Multiplexer Input 07
13	B02	Digital Output 02	33	AIN06	Analog Multiplexer Input 06
14	B03	Digital Output 03	34	AIN05	Analog Multiplexer Input 05
15	B04	Digital Output 04	35	AIN04	Analog Multiplexer Input 04
16	B05	Digital Output 05	36	AIN03	Analog Multiplexer Input 03
17	B06	Digital Output 06	37	AIN02	Analog Multiplexer Input 02
18	B07	Digital Output 07	38	AIN01	Analog Multiplexer Input 01
19	B08	Digital Output 08	39	AIN00	Analog Multiplexer Input 00
20	B09	Digital Output 09	40	NREF	Low Analog Reference Voltage

Figure 4: Package Pin-Out and Signal Definition

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Truth Table (AIN00 – AIN07)

AD02	AD01	AD00	EN_H	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	AIN00
L	L	H	H	AIN01
L	H	L	H	AIN02
L	H	H	H	AIN03
H	L	L	H	AIN04
H	L	H	H	AIN05
H	H	L	H	AIN06
H	H	H	H	AIN07

Figure 5: Truth Table

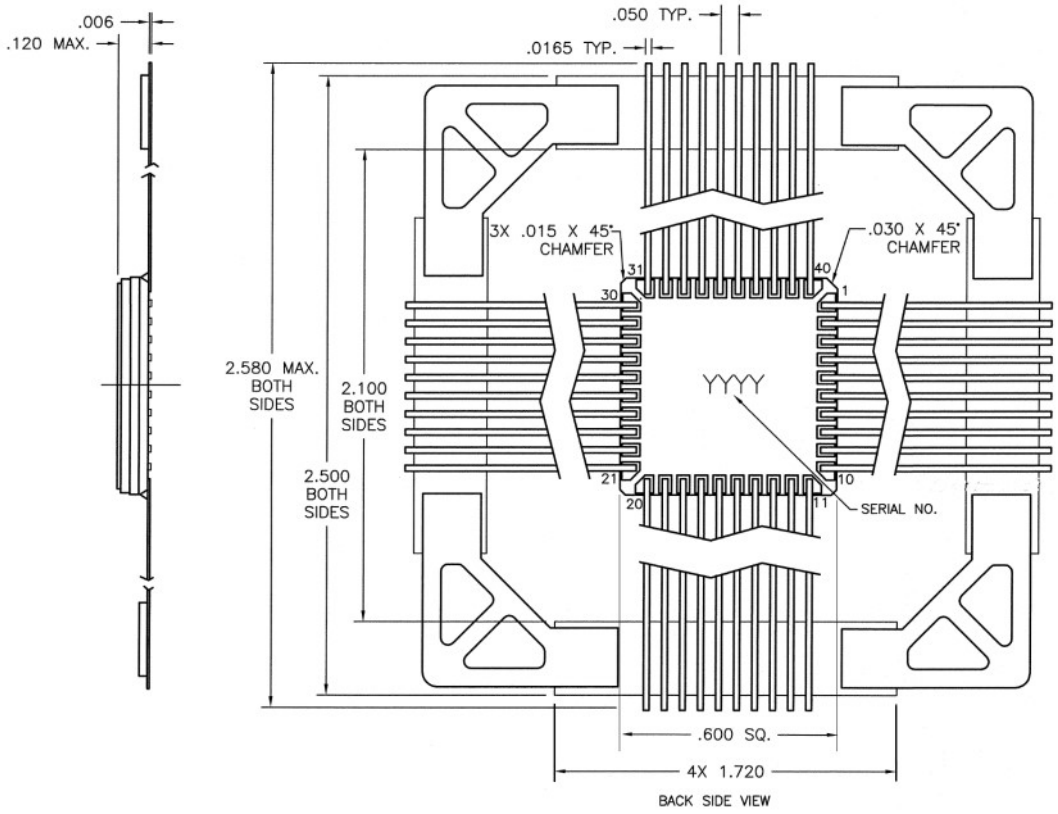

Figure 6: Package Outline

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Application Notes

1) How to hook this part up.

a) Single Conversion Mode

I. Power:
   1) The Analog power AV_{CC} should be 5V with 10uF and 0.1uF bypass and returned to a quiet ground via Agnd.
   2) The Digital power DV_{CC} should also be 5V with 10uF and 0.1uF bypass and returned to a ground other than the quiet ground via Dgnd.
   3) The output drive power DVRP can be either 5V or 3.3V and returned to a ground other than the quiet ground via DVRN. NOTE: This is the supply for the output drivers and there will be noise spikes on the return.
      a) When operating into a 3.3V device, set DVRP to 3.3V for internal level shifting.
      b) When operating into TTL or 5 volt logic, set DVRP to 5V for no level shifting.

II. References:
   1) The PREF can be any voltage from the NREF value to V_{CC}. It is best to operate with PREF at least 0.25V away from V_{CC} to avoid gain compression, but it is feasible to operate PREF at V_{CC}.
   The impedance of the reference (PREF –to-NREF) is typ 3K and min 2K ohms
   2) The NREF can be any voltage from the Ground to the PREF value. It is best to operate with NREF at least 0.25V away from Ground to avoid gain compression, but it is feasible to operate NREF at Ground.

III. Analog Input Channels
   1) Leads 1,2,35-48 (Analog input 1-16) can be connected directly to the analog voltage sensors to be monitored.
   2) It is advisable to add a low pass filter on each channel to filter out high frequency noise if full 14 Bit operation is required

IV. Digital Outputs
   1) Leads 14-27 (Bits 0-13) can be connected directly to an FPGA.

V. Multiplexer Address Lines
   1) Leads 6-9 (Address 0-3) can be connected to a controller to select the proper input to be sampled.
   2) The address lines are active high.

VI. Control Inputs
   1) Clock:
      a) Best operation with a 50% duty cycle but can vary ±10%
      b) Operating Frequency: Max 1MHz, Minimum frequency is determined by the droop rate of the internal Sample/Hold switch, which is in characterization.
      c) Active High, CMOS levels
   2) Enables:
      a) EN_H:
         I. Active High, CMOS levels
         II. A low will place the unit in a sleep mode for low current draw. Nominal current is drawn when the unit is active.
      b) OE_H:
         I. Active High, CMOS levels
         II. A low will cause the outputs to be in Tri-State mode.

3) Start Convert:
   a) STCNV_H:
      - Active High, CMOS levels.
      - The input must be pulsed Low/High/Low to and coincident with a rising clock edge to start a conversion cycle of 20 clocks.

VII. Control Outputs:
1) End of Conversion Cycle
   a) EOC_H
      I. Active High, CMOS levels
      II. This flag will be set high upon the completion of a 20 clock conversion cycle for only ONE CLOCK cycle.
      III. Denotes that the conversion data is available on the digital output lines B00-B13
   b) BUSY_L
      I. Active Low, CMOS levels
      II. This flag is set low during the first clock cycle after a conversion cycle has been initiated.
      III. The flag will be set high again ONE Clock cycle after the EOC_H pulse.

b) Continuous Mode

i. Same as for single convert mode except:

1) Connect the BUSY_L output directly to the STCNV_H input.
   a) When a conversion cycle is completed, the BUSY_L transitions from Low-to-High initiating the next conversion cycle. Once the cycle commences, the BUSY_L returns low which resets for the next STCNV_H pulse.
   b) This cycle initiates at a Power On condition. It is not required to start the first cycle. It is autonomous.

Power Supply Sequencing

There is no power supply sequencing required for the RHD5958 and no harm will come to the unit with any combination of sequencing.

If a sequencing is desired, the suggested sequence would be: DV_{CC}, AV_{CC} followed by DVRP.

Notes:

If DVRP is applied first, the output drivers may be in unknown states until DV_{CC} is applied. This may affect downstream components.

The digital and analog inputs should not be powered to more than 0.5V above their supply voltages to ensure the protection diodes do not become forward biased and draw excessive current.

The part will not be damaged with Voltages within reason above the supply, but any possible long term reliability effects cannot be determined.

Best to make sure all devices connected to the RHD5958 are powered simultaneously or make sure no I/O power up before the RHD5958.

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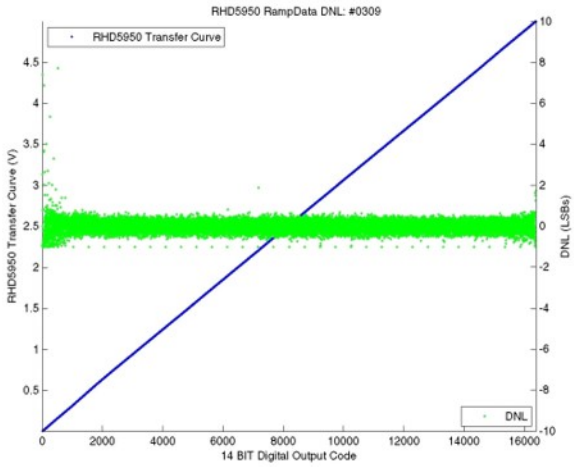
Differential and Integral Non-linearity (DNL, INL) Typical Plots

Typical DNL and INL plots for the CAES RHD5958 are shown below. The plots were taken on the CAES production tester. The references were set for 5.0v on the positive 'upper' reference (PREF) and 0.0 volts on the negative 'lower' reference (NREF). The input voltage was ramped from 0 volts to 5 volts and the data captured.

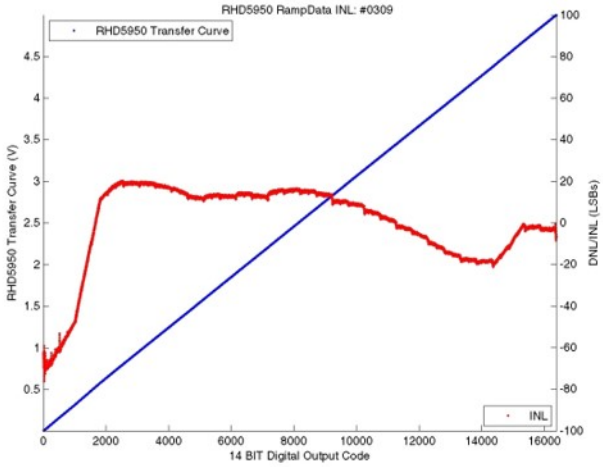
The majority of the DNL plot is within ±1 LSB throughout the input voltage range with the exception of some outliers (unit dependent). There are anomalies occurring at the end points. At the upper end, approaching the 5 volt supply limit, there are issues with parameters operating at the supply limits which creates inaccuracies that affect the DNL at the last few codes. At the lower end there is a wide swing in DNL which may be associated with the test system and noisy test environments. Further characterization is required.

The INL plot shows the additive effects of the DNL throughout the input voltage range. In the range of Vin =0.5 volts to 5 volts, the INL is shown to be ±20LSBs which for a reference range of 5 volts and 14 Bits is an inaccuracy of 6.1 mV. At input voltages less than 0.5 volts, the DNL anomaly dominates and the accuracy falls off.

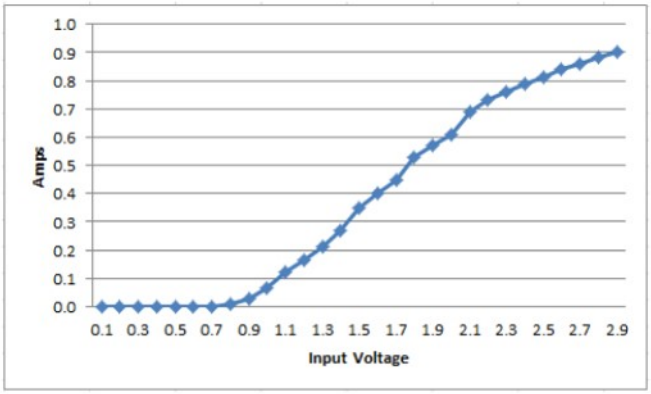
It has always been the intention for the RHD5958 to be operated away from the supply rail to avoid the inaccuracies of operating close to these areas.



Typical DNL Plot



Typical INL Plot



Typical Protection Diode I-V Curve

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FAQ:

Q. Does the ADC needs to flush out the first read value after waking up, before reading meaningful values.?
A. YES, after setting the EN input High, a full conversion should take place because there may be erroneous signal settings during the 'wake up' period that will need to be placed in the proper setting which would occur after a complete cycle has been executed. This way it is ensured that the state machine has all values initialized. So once an EOC high is detected, a meaningful conversion can be performed

Q. Does OE_H place EOC_H in Tri-State?
A. No, EOC_H is not affected by OE_H. The Output Enable signal (OE_H) is pertinent to the Output data lines B(0:13). The EOC_H signal is always enabled.

Q. Does OE_H place BUSY_L in Tri-State?
A. No, BUSY_L is not affected by OE_H either. The BUSY_L signal is also always enabled.

Q. Can the minimum wait time for starting a new conversion; rising edge of BUSY_L to rising edge of STCNV_H, be 0ns?
A. Since BUSY_L transitions high due to the rising edge of CLK and if there is 0ns time between BUSY_L and STCNV_H, then STCNV_H would not get clocked in until the next rising edge of CLK. This is the same as Continuous Conversion Mode where BUSY_L is tied to STCNV_H (0ns delay)

Q. What is the delay time for the rising edge of OE_H to data being driven delay?
A. The delay time from OE_H to valid data output is 25ns Maximum.

Q. Is the STCNV_H signal edge triggered or a level?
A. The STCNV_H signal is clocked in on the rising edge of CLK. So the width has to be coincident with the clock edge with a minimum setup time of 20ns.

Q. Are there internal references that powers the VPREF/VNREF pins on the device or are external references required?
A. The RHD5958 requires an external power source on the PREF and NREF pins. The NREF can be tied to Ground, but if the reference range is set to be between the power supply rails (say 0.5v and 4.5v), they both requires external sources. These sources should be clean and stable in order to get the best conversion. Use of stable voltage reference devices with filtering is preferable over resistor dividers from V_{CC}/Gnd.

DATASHEET

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SCD5958

8-Channel Multiplexed, 14-Bit, Analog-to-Digital Converter

RHD5958

Ordering Information

Model	DLA SMD #	Screening	Package
RHD5958-7	-	Commercial Flow, +25°C testing only	40-lead CQFP
RHD5958-S	-	Military Temperature, -55°C to +125°C Screened in accordance with the individual Test Methods of MIL-STD-883 for Space Applications	
RHD5958-201-1S	5962-1221101KXC	In accordance with DLA SMD	
RHD5958-901-1S	5962R1221101KXC	In accordance with DLA Certified RHA Program Plan to RHA Level "R", 100 krad(Si)	

Revision History

Date	Revision	Change Description
11/6/2019	B	Import into CAES format. Change TID level to 100krad(Si), Add Diode Protection Circuit, Update Figure numbering, Add Switching Characteristics Table, Add Application Notes.
03/15/2021	C	Revised per ECN 23555.

DATASHEET

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SCD5958

8-Channel Multiplexed, 14-Bit, Analog-to-Digital Converter

RHD5958

Datasheet Definitions

	DEFINITION
Advanced Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet **is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final**.
Preliminary Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

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