DATASHEET

RELEASED 1/14/16

16-Channel Multiplexed 14-Bit Analog-to-Digital Converter

RHD5950

Features

- Single power supply operation 5.0V or Dual power supply for 3.3V I/O
- Radiation performance
  - Total dose: > 100krad(Si); Dose rate = 50 - 300 rads(Si)/s
  - ELDRS Immune
  - SEL Immune >100 MeV-cm^2/mg
  - Neutron Displacement Damage >10^{14} neutrons/cm^2
- 16-Channel Input Multiplexer
- Successive Approximation A-to-D
- Level Shifting Digital Output Drivers allow interfaces to 5.0 or 3.3 volt logic
- Tri-State digital outputs
- Power Down (Sleep) mode
- Single or continuous conversion
- 20us conversion period (20 clocks @ 1MHz Clock rate)
- Multiplexer address is latched on first clock rising edge of a cycle
- Busy and End-of-Conversion status outputs
- Full military temperature range
- Designed for aerospace and high reliability space applications
- Packaging – Hermetic Ceramic
  - 48 leads, 0.700"Sq x 0.125"Ht quad flat pack
  - Weight - 6 grams max
- **CAES Radiation Hardness Assurance Plan is DLA Certified to MIL-PRF-38534, Appendix G.**

General Description

CAES RHD5950 is a radiation hardened, single supply, 16-Channel Multiplexed Analog-to-Digital converter in a 48-pin Ceramic Quad Flat Package. The RHD5950 design uses specific circuit topology and layout methods to mitigate total ionizing dose effects and single event latchup. It is guaranteed operational from -55°C to +125°C. Available screened in accordance with MIL-PRF-38534 Class K, the RHD5950 is ideal for demanding military and space applications.

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Organization and Application

The RHD5950 takes 16 analog sensor signals and using 4 address inputs and an enable input, selects one of the 16 analog inputs and performs a 14-bit successive approximation analog-to-digital conversion in a nominal period of 20 clock cycles (20uS nominal). The 14-bit digital output has a tri-state control allowing the connection of multiple RHD5950s. This provides the ability to interface many sensor voltage readings to the digital processor data bus. The full-scale range is determined by reference input voltages. The input impedance of the reference/span terminals is typically a constant 4K ohms.

Gain compression will occur near either power supply extremes but can be avoided if the references are more than 200mV away from the respective supply terminals. The input span can be less than 4 volts at the expense of ultimate resolution

The analog channel's input impedance is primary capacitance (20pF typical). The input voltage charges a track-and-hold hold capacitor through transmission gates. The input bandwidth is determined by the slew rate of the hold amplifier and is adequate to allow input sampling in three clock periods (3uS nominal). The ultimate bandwidth is determined by the aperture uncertainty associated with the closing of the sample gate (approximately 5nS). The converter bandwidth is then determined by the sampling Nyquist frequency rather than the input signal; change rate (dv/dt) and the LSB weight in volts as would be the case if there were no sample-and-hold.

Start-Convert (STCNV_H), Busy (BUSY_L) and End-Of-Convert (EOC_H) status and control lines are provided. The converter will operate in either continuous or single conversion modes. To operate in continuous mode, STCNV_H should be tied to BUSY_L. The digital output register changes at the end of a conversion and is latched when EOC_H is asserted High. The output data will remain latched until the next conversion is complete and will be updated when EOC_H is asserted High. The output circuitry operates from a voltage independent of the remainder of the chip such that I/O is compatible with digital systems from, less than 3.3 volts, to 5 volts.

The converter divides the reference voltage into 16 segments with a linear weighted resistor network. The voltage on any segment is passed to a linear 10-bit DAC for interpolation. The sampled input voltage is compared to the output of the two stage DAC for a 14-bit successive approximation conversion.

All inputs are protected to both power supply rails by semiconductor diodes. Inputs should be constrained to V_{CC}+0.4 and GND-0.4 to avoid forward biasing protection paths.

The devices will not latch with SEU events to above 100 MeV-cm²/mg. Displacement damage environments to neutron fluence equivalents in the mid 10^{14} neutrons per cm² range are readily tolerated. There is no sensitivity to low-dose rate (ELDRS) effects. SEU effects are application dependent.

Notes:

- The STCNV_H is a dynamic input (positive edge triggered) and should not be tied to a static voltage.
- The input signals should be low pass filtered to reduce high frequency noise
- If Sleep mode is enabled (EN_H=0), when waking up (EN_H=1), the unit has to complete an entire conversion cycle so the digital logic is in the proper state.
  Ex. If using a 1MHz clock; after EN_H=1 and 20us after STCNV_H is applied.

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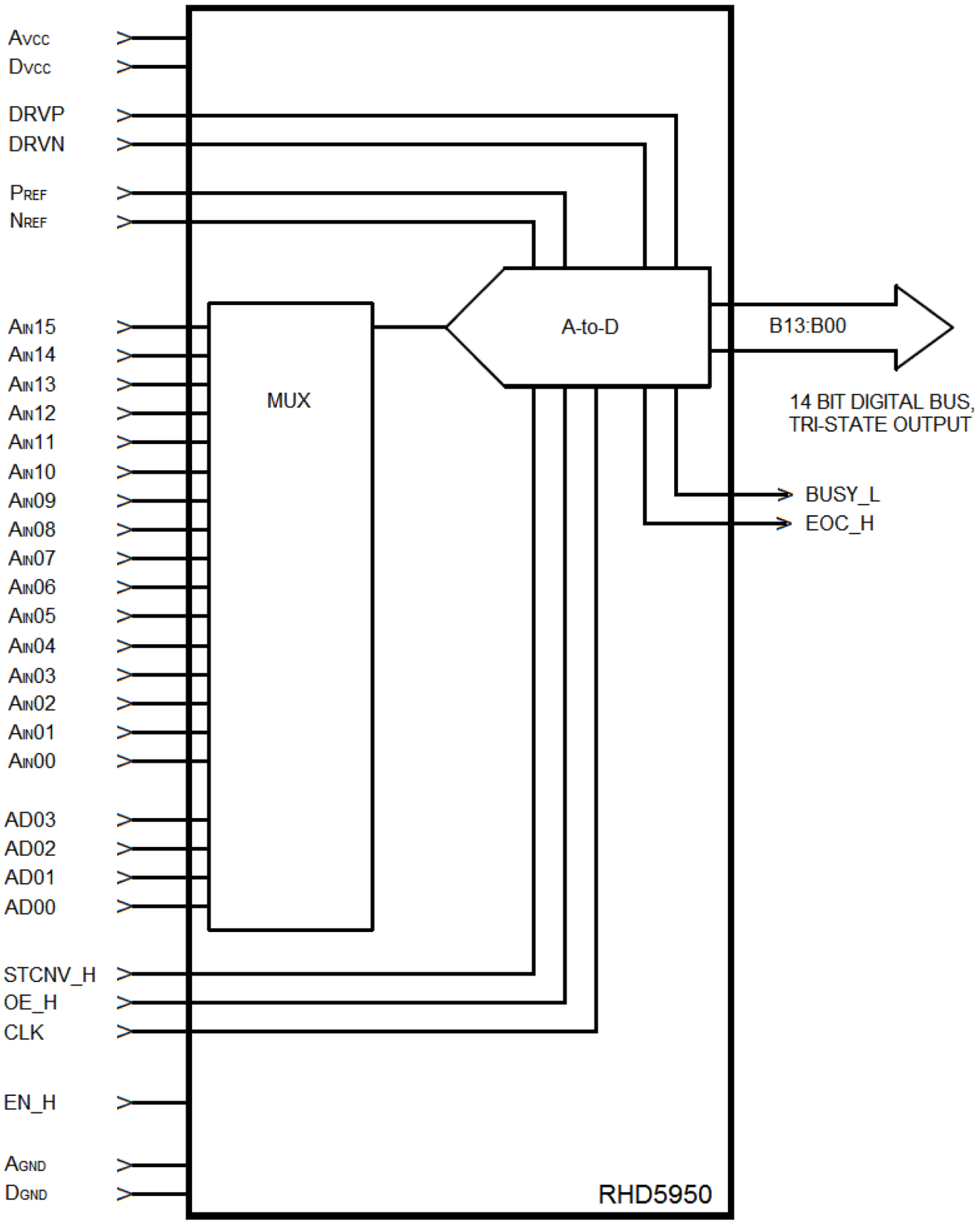

Figure 1: Block Diagram

16-Channel Multiplexed 14-Bit Analog-to-Digital Converter

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Absolute Maximum Ratings

Parameter	Range	Units
Case Operating Temperature Range	-55 to +125	℃
Storage Temperature Range	-65 to +150	℃
Junction Temperature	+150	℃
Supply Voltage V_{CC} - GND	+7.0	V
Input Voltage, PREF, NREF	V_{CC} +0.4 GND -0.4	V
Lead Temperature (soldering, 10 seconds)	300	℃
Thermal Resistance, Junction to Case, Θjc	2.0	℃/W

Notice:

1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress rating only; Functional operation beyond the "Operation Conditions" is not recommended and extended exposure beyond the "Operation Conditions" may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Typical	Units
$+A_{VCC}$	Analog Power Supply Voltage	5.0	V
$+D_{VCC}$	Digital Power Supply Voltage	5.0	V
DRVP	Digital Output High Reference Level	3.3 to 5.0	V
DRVN	Digital Output Low Reference Level	0	V
PREF	High Analog Reference Voltage	4.5	V
NREF	Low Analog Reference Voltage	0.5	V

Electrical Performance Characteristics

(T_C = -55°C to +125°C, +A_{VCC} = +5.0 V, +D_{VCC} = +5.0 V, +DRVP = +5.0 V, unless stated otherwise)

Parameter	Symbol	Conditions	MIN	MAX	Units
Analog Supply Current Quiescent 1/	AI_{CCQ}	V_{EN} = D_{VCC}, V_{OE} = D_{VCC}, CLK = D_{GND}	-	10	mA
Analog Supply Current Active 1/	AI_{CCA}	V_{EN} = D_{VCC}, V_{OE} = D_{VCC}	-	10	mA
Analog Supply Current Sleep 1/	AI_{CCS}	V_{EN} = D_{GND}, V_{OE} = D_{GND}	-	4	mA
Digital Supply Current Quiescent 1/	DI_{CCQ}	V_{EN} = D_{VCC}, V_{OE} = D_{VCC}, CLK = D_{GND}	-	1	mA
Digital Supply Current Active 1/	DI_{CCA}	V_{EN} = D_{VCC}, V_{OE} = D_{VCC}	-	2	mA
Digital Supply Current Sleep 1/	DI_{CCS}	V_{EN} = D_{GND}, V_{OE} = D_{GND}	-	1	mA
Digital Output Supply Current Quiescent 1/	$05I_{CCQ}$	V_{EN} = D_{VCC}, V_{OE} = D_{VCC}, CLK = D_{GND}, C_L = 50 pF	-	0.1	mA
Digital Output Supply Current Active 1/	$05I_{CCA}$	V_{EN} = D_{VCC}, V_{OE} = D_{VCC}, C_L = 50 pF	-	1	mA
Digital Output Supply Current Sleep 1/	$05I_{CCD}$	V_{EN} = D_{VCC}, V_{OE} = D_{GND}, C_L = 50 pF	-	1	mA
Full-scale Input Range 1/	V_{IN}		V_{NREF}	V_{PREF}	V
Input Capacitance 2/	C_{IN}	Tc = +25°C	-	50	pF
Analog Reference Impedance 1/	Z_{REF}	PREF to NREF	2	6	KΩ
High Analog Reference Voltage	V_{PREF}	DVRP = 5.0 V 1/	V_{NREF}	5.0	V
		DVRP = 3.3 V 2/			
Low Analog Reference Voltage	V_{NREF}	DVRP = 5.0 V 1/	0	V_{PREF}	
		DVRP = 3.3 V 2/			
Channel Isolation 2/	ISO	Tc = +25°C	80	-	dB

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Electrical Performance Characteristics

(Tc= -55°C to +125°C, $+A_{VCC}$ = +5.0 V, $+D_{VCC}$ = +5.0 V, +DRVP = +5.0 V, unless stated otherwise)

Parameter	Symbol	Conditions		MIN	MAX	Units
Integral Nonlinearity 1/	INL	PREF-NREF = 4.0 V		-48	48	LSBs
Differential Nonlinearity 1/	DNL	PREF-NREF = 4.0 V		-8.2	8.2	LSBs
Offset Error 1/	O_E	PREF-NREF = 4.0 V		-1	1	%FSR
Gain Error 1/	A_E	PREF-NREF = 4.0 V		-2	2	%FSR
Clock Frequency 1/	f_C	PREF-NREF = 5.0 V		-	1	MHz
Maximum Sampling Rate 2/	f_{SAMPLE} (MAX)	Fc = 1 MHz, 20 clocks per conversion		-	50	kSPS
High Input Leakage Current (AIN00-AIN15) 1/ 3/	$I_{INLK_{HI}}$	Input under test = A_{VCC}, V_{EN} = DV_{CC}	+25°C	-5	5	nA
			+125°C	-50	50	
Low Input Leakage Current (AIN00-AIN15) 1/ 3/	$I_{INLK_{LO}}$	Input under test = A_{GND}, V_{EN} = DV_{CC}	+25°C	-5	5	
			+125°C	-50	50	
Digital High Level Input Voltage EN_H, STCNV_H, OE_H, CLK, (AD00-AD03)	V_{IH}	DVRP = 5.0 V 1/		3.5	-	V
		DVRP = 3.3 V 2/		2.31	-	
Digital Low Level Input Voltage EN_H, STCNV_H, OE_H, CLK, (AD00-AD03)	V_{IL}	DVRP = 5.0 V 1/		-	1.5	
		DVRP = 3.3 V 2/		-	0.99	
Digital High Level Input Current EN_H, STCNV_H, OE_H, CLK, (AD00-AD03) 1/ 3/	I_{IH}	Digital input under test = 5.0 V All other digital inputs = D_{GND}	+25°C	-5	5	nA
			+125°C	-50	50	
Digital Low Level Input Current EN_H, STCNV_H, OE_H, CLK, (AD00-AD03) 1/ 3/	I_{IL}		+25°C	-5	5	
		All digital inputs = D_{GND}	+125°C	-50	50	
Digital High Level Output Voltage (B00-B13) 1/	V_{OH}	DVRP = 5.0 V, V_{EN} = D_{VCC}, I_{OH} = -4.0 mA		4.2	-	V
		DVRP = 3.3 V, V_{EN} = D_{VCC}, I_{OH} = -4.0 mA		2.7	-	
Digital Low Level Output Voltage (B00-B13) 1/	V_{OL}	DVRP = 5.0 V, V_{EN} = D_{VCC}, I_{OL} = +4.0 mA	-55°C,	-	0.6	
			+25°C			
			+125°C	-	0.8	V
		DVRP = 3.3 V, V_{EN} = D_{VCC}, I_{OL} = +4.0 mA	-55°C,	-	0.6	
			+25°C			
			+125°C	-	0.8	
Digital High Level Output Current (B00-B13) 1/	I_{OH} (SOURCE)	DVRP = 5.0 V, V_{EN} = V_{IH}		-	-4.0	
		DVRP = 3.3 V, V_{EN} = V_{IH}		-	-4.0	
Digital Low Level Output Current (B00-B13) 1/	I_{OL} (SINK)	DVRP = 5.0 V, V_{EN} = V_{IH}		-	4.0	mA
		DVRP = 3.3 V, V_{EN} = V_{IH}		-	4.0	
High Output Leakage Current (B00-B13) 1/ 3/	$I_{OUTLK_{HI}}$	V_{OE} = D_{GND}	+25°C	-5	5	
			+125°C	-50	50	
Low Output Leakage Current (B00-B13) 1/ 3/	$I_{OUTLK_{LO}}$	V_{OE} = D_{GND}	+25°C	-5	5	nA
			+125°C	-50	50	

Notes:

1) Specification derated to reflect Total Dose exposure to 100krad(Si) @ +25°C.
2) Not tested. Shall be guaranteed by design, characterization, or correlation to other test parameters.
3) These parameters for Tc = -55°C are guaranteed by design, characterization, or correlation to other test parameters.

Switching Characteristics

(Tc = -55°C to +125°C, +A_{VCC} = +5.0 V, +D_{VCC} = +5.0 V, +DRVP = +5.0 V, unless stated otherwise)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Units
STCNV_H to CLK			20	-	-	ns
ADDRESS to CLK Setup			20	-	-	ns
CLK to BUSY_L Low			-	50	-	ns
CLK to EOC_H High			-	50	-	ns
EOC_H to OUTPUT DATA			-	50	-	ns
CLK to EOC_H Low			-	50	-	ns
CLK to BUSY_L High			-	50	-	ns
CLK Pulse Width			50	-	-	ns
DATA Sampling Time			3	-	5	ns

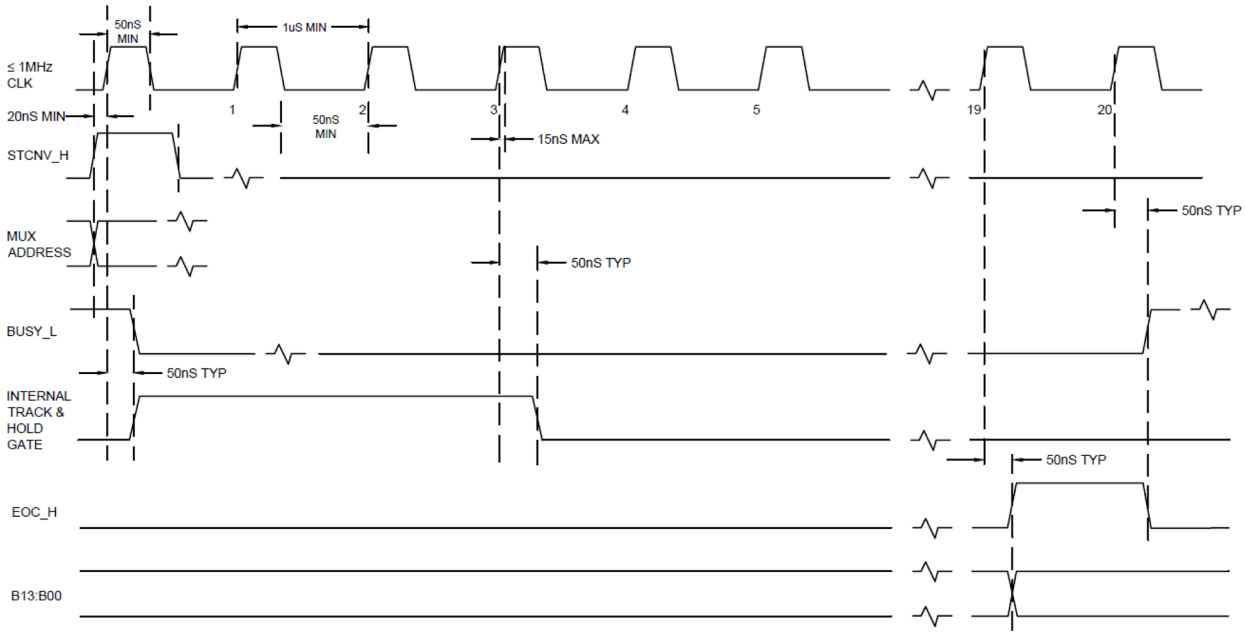

Figure 2: Basic Timing Diagram

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Package PIN-OUT and Signal Definition

Pin #	Signal	Definition	Pin #	Signal	Definition
1	AIN01	Analog Multiplexer Input 01	25	B11	Digital Output 11
2	AIN00	Analog Multiplexer Input 00	26	B12	Digital Output 12
3	NREF	Low Analog Reference Voltage	27	B13	Digital Output 13
4	A_{VCC}	Analog Supply Voltage	28	EOC_H	End of Convert Output (Active High)
5	D_{VCC}	Digital Supply Voltage	29	BUSY_L	Busy Output (Active Low)
6	AD03	Multiplexer Address 03	30	DRVN	Digital Output Low Reference Level
7	AD02	Multiplexer Address 02	31	DRVP	Digital Output High Reference Level
8	AD01	Multiplexer Address 01	32	D_{GND}	Digital Supply Return
9	AD00	Multiplexer Address 00	33	A_{GND}	Analog Supply Return
10	STCNV_H	Start Convert: A Low-to-High transition starts the conversion cycle	34	PREF	High Analog Reference Voltage
11	EN_H	A Low places part in SLEEP mode. A High Enable the A2D converter	35	AIN15	Analog Multiplexer Input 15
12	OE_H	A Low Tristates the outputs. A High Enables the outputs	36	AIN14	Analog Multiplexer Input 14
13	CLK	Clock Input	37	AIN13	Analog Multiplexer Input 13
14	B00	Digital Output 00	38	AIN12	Analog Multiplexer Input 12
15	B01	Digital Output 01	39	AIN11	Analog Multiplexer Input 11
16	B02	Digital Output 02	40	AIN10	Analog Multiplexer Input 10
17	B03	Digital Output 03	41	AIN09	Analog Multiplexer Input 09
18	B04	Digital Output 04	42	AIN08	Analog Multiplexer Input 08
19	B05	Digital Output 05	43	AIN07	Analog Multiplexer Input 07
20	B06	Digital Output 06	44	AIN06	Analog Multiplexer Input 06
21	B07	Digital Output 07	45	AIN05	Analog Multiplexer Input 05
22	B08	Digital Output 08	46	AIN04	Analog Multiplexer Input 04
23	B09	Digital Output 09	47	AIN03	Analog Multiplexer Input 03
24	B10	Digital Output 10	48	AIN02	Analog Multiplexer Input 02

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Truth Table (AIN00 – AIN15)

A3	A2	A1	A0	EN	"ON" Channel
X	X	X	X	L	NONE
L	L	L	L	H	AIN0
L	L	L	H	H	AIN1
L	L	H	L	H	AIN2
L	L	H	H	H	AIN3
L	H	L	L	H	AIN4
L	H	L	H	H	AIN5
L	H	H	L	H	AIN6
L	H	H	H	H	AIN7
H	L	L	L	H	AIN8
H	L	L	H	H	AIN9
H	L	H	L	H	AIN10
H	L	H	H	H	AIN11
H	H	L	L	H	AIN12
H	H	L	H	H	AIN13
H	H	H	L	H	AIN14
H	H	H	H	H	AIN15

Ordering Information

Model	DLA SMD #	Screening	Package
RHD5950-7	-	Commercial Flow, +25°C testing only	48-lead CQFP
RHD5950-S	-	Military Temperature, -55°C to +125°C Screened in accordance with the individual Test Methods of MIL-STD-883 for Space Applications	
RHD5950-201-1S	5962-1220301KXC	In accordance with DLA SMD	
RHD5950-901-1S	5962R1220301KXC	In accordance with DLA Certified RHA Program Plan to RHA Level "R", 100krads(Si)	

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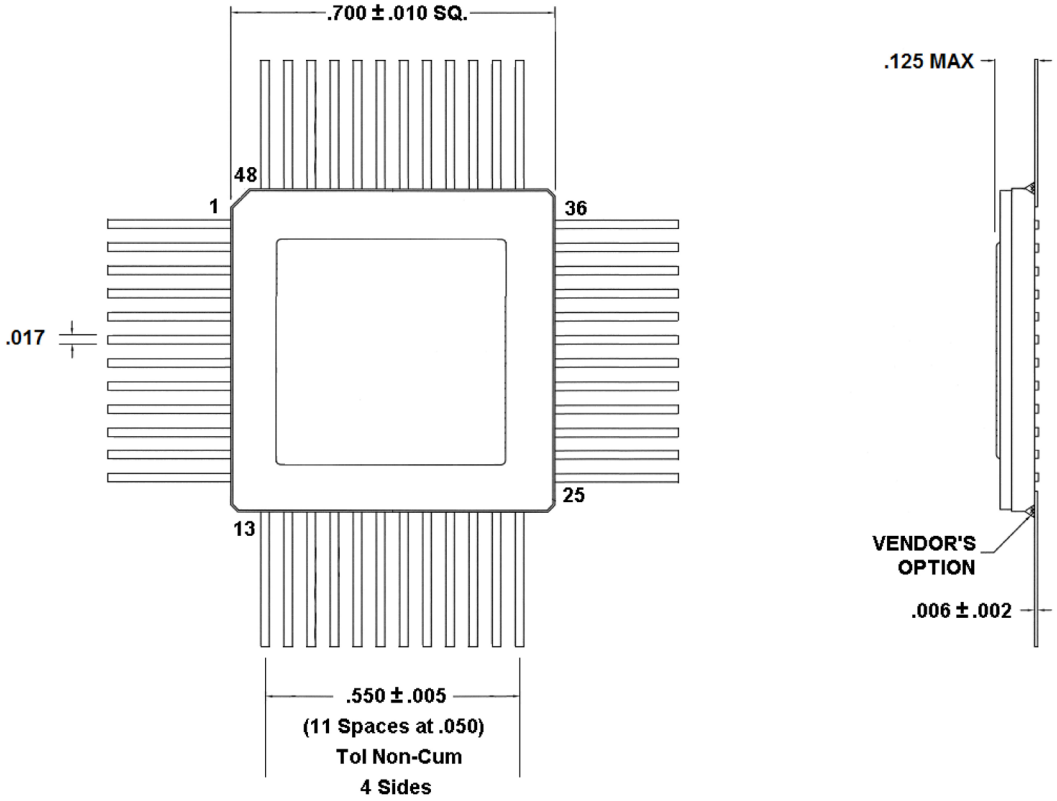

Figure 3: Package Outline

Note:

1) Outside ceramic tie bars not shown for clarity. Contact factory for details.

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Datasheet Definitions

	DEFINITION
Advanced Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet **is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final**.
Preliminary Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

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