

Quad Operational Amplifier

RHD5900

Features

- Single power supply operation at 3.3V or 5.0V
- Radiation performance
 - Total dose: >1 Mrad(Si); Dose rate = 50-300 rad(Si)/s
 - ELDRS Immune
 - SEL Immune >100 MeV-cm²/mg
 - Neutron Displacement Damage >10¹⁴ neutrons/cm²
- Rail-to-Rail input and output range
- Short Circuit Tolerant
- Full military temperature range
- Designed for aerospace and high reliability space applications
- Packaging – Hermetic ceramic SOIC
 - 16-pin, .417"L x .300"W x .120"Ht
 - Weight - 0.8 grams max
- **Radiation Hardness Assurance Plan: DLA Certified to MIL-PRF-38534, Appendix G.**



General Description

The RHD5900 is a radiation hardened, single supply, quad operational amplifier in a 16-pin SOIC package. The RHD5900 design uses specific circuit topology and layout methods to mitigate total ionizing dose effects and single event latchup. These characteristics make the RHD5900 especially suited for the harsh environment encountered in Deep Space missions. It is guaranteed operational from -55°C to +125°C. Available screened in accordance with MIL-PRF-38534 Class K, the RHD5900 is ideal for demanding military and space applications.

Organization and Application

The RHD5900 amplifiers are capable of rail-to-rail input and outputs. Performance characteristics listed are for general purpose CMOS operational amplifier applications at 3.3V ±10% and 5V ±10%. The amplifiers will drive substantial resistive or capacitive loads and are unity gain stable under normal conditions. Resistive loads in the low kohm range can be handled without gain derating and capacitive loads of several nF can be tolerated. CMOS device drive has a negative temperature coefficient and the devices are therefore inherently tolerant to momentary shorts, although on chip thermal shutdown is not provided. All inputs and outputs are diode protected.

The devices will not latch with SEU events to above 100 MeV-cm²/mg. Total dose degradation is minimal to above 1 Mrad(Si). Displacement damage environments to neutron fluence equivalents in the mid 10¹⁴ neutrons per cm² range are readily tolerated. There is no sensitivity to low-dose rate (ELDRS) effects. SEU effects are application dependent.

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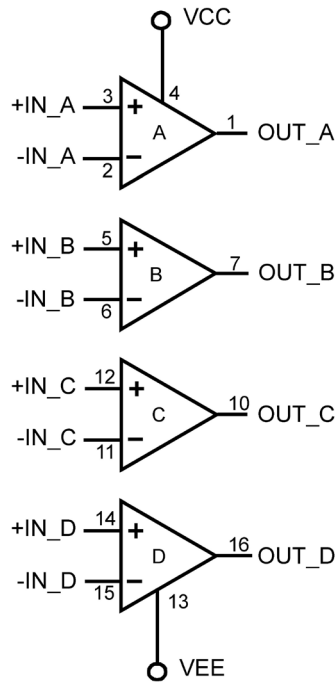
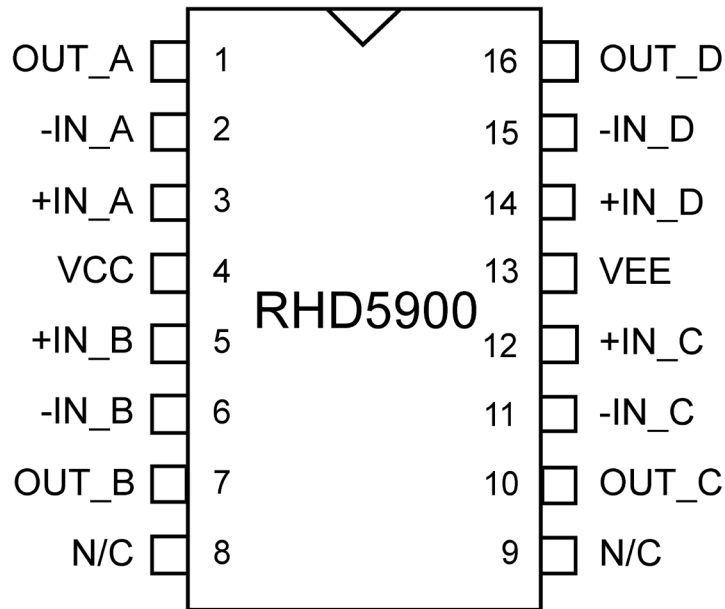


Figure 1: Block Diagram



16-Pin SOIC
Figure 2: Package Pin-out

Notes:

- 1) Package and lid are electrically isolated from signal pads.
- 2) It is recommended that N/C or no connect pins (pins 8 and 9) and lid be grounded. This eliminates or minimizes any ESD or static buildup.

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RHD5900 Pin-Out & Signal Definitions

Pin #	Signal	Function
1	OUT_A	Output of section A
2	-IN_A	Inverting input of section A
3	+IN_A	Non-inverting input of section A
4	VCC	Positive power supply
5	+IN_B	Non-inverting input of section B
6	-IN_B	Inverting input of section B
7	OUT_B	Output of section B
8	N/C	No Connect
9	N/C	No Connect
10	OUT_C	Output of section C
11	-IN_C	Inverting input of section C
12	+IN_C	Non-inverting input of section C
13	VEE	Power supply Return
14	+IN_D	Non-inverting input of section D
15	-IN_D	Inverting input of section D
16	OUT_D	Output of section D

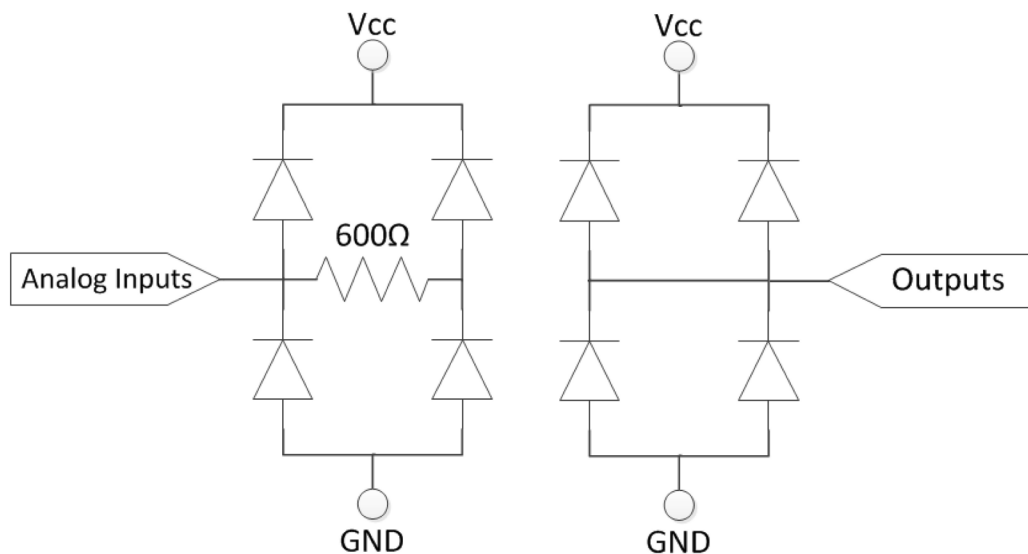


Figure 3: Diode Protection Circuits Diagram

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Absolute Maximum Ratings

Parameter	Range	Units
Case Operating Temperature Range	-55 to +125	°C
Storage Temperature Range	-65 to +150	°C
Junction Temperature	+150	°C
Supply Voltage $V_{CC} - V_{EE}$	+7.0	V
Input Voltage	$V_{CC} + 0.4$ $V_{EE} - 0.4$	V
Lead Temperature (soldering, 10 seconds)	300	°C
Thermal Resistance, Junction to Case, θ_{jc}	7	°C/W
Power @25°C	200	mW
ESD per MIL-STD-883, Method 3015, Class 2	2,000 to 3,999	V

Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress rating only; functional operation beyond the "Operation Conditions" is not recommended and extended exposure beyond the "Operation Conditions" may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Typical	Units
$+V_{CC}$	Power Supply Voltage	3.3 to 5.0	V
V_{CM}	Input Common Mode Range	V_{CC} to ($V_{EE} = \text{GND}$)	V

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Electrical Performance Characteristics IA

Parameter	Symbol	Conditions $V_{CC} = 3.3V \pm 10\%$, $V_{EE} = GND$	Temperature	MIN	MAX	Units
Quiescent Supply Current	I_{CCQ}	No Load	+25°C	-	3.5	mA
			+125°C	-	3.4	
			-55°C	-	3.3	
Input Offset Voltage	V_{OS}		+25°C	-2.2	2.2	mV
			+125°C, -55°C	-2.8	2.8	
Input Offset Current	I_{OS}		+25°C, -55°C	-75	75	pA
			+125°C	-100	100	
Input Bias Current	I_B		+25°C, -55°C	-75	75	pA
			+125°C	-500	500	
Common Mode Rejection Ratio	CMRR		+25°C	64		dB
			+125°C	69		
			-55°C	53		
Power Supply Rejection Ratio	PSRR		+25°C	55		dB
			+125°C, -55°C	50		
Output Voltage High	V_{OH}	$R_{OUT}=3.6K$ to GND	All	$V_{CC}-1$		V
Output Voltage Low	V_{OL}	$R_{OUT}=3.6K$ to V_{CC}	+25°C		0.080	V
			+125°C		0.095	
			-55°C		0.07	
Slew Rate	SR	$R_L = 8K$, Gain = 1	+25°C	2.1		V/uS
			+125°C	2.0		
			-55°C	1.9		
Open Loop Gain	A_{OL}	No Load	+25°C	97		dB
			+125°C	91		
			-55°C	94		
Unity Gain Bandwidth	UGBW	$R_L = 10K$	+25°C	3.7		MHz
			+125°C	2.4		
			-55°C	4.3		

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Electrical Performance Characteristics IB

Parameter	Symbol	Conditions $V_{CC} = 5.0V \pm 10\%$, $V_{EE} = GND$ Unless Otherwise Specified	Temperature	MIN	MAX	Units
Quiescent Supply Current	I_{CCQ}	No Load	+25°C	-	4.5	mA
			+125°C, -55°C	-	4.4	
Input Offset Voltage	V_{OS}		+25°C	-2.5	2.5	mV
			+125°C, -55°C	-2.8	2.8	
Input Offset Current	I_{OS}		+25°C, -55°C	-75	75	pA
			+125°C	-100	100	
Input Bias Current	I_B		+25°C, -55°C	-75	75	pA
			+125°C	-500	500	
Common Mode Rejection Ratio	CMRR		+25°C	73		dB
			+125°C, -55°C	71		
Power Supply Rejection Ratio	PSRR		+25°C	73		dB
			+125°C, -55°C	71		
Output Voltage High	V_{OH}	$R_{OUT}=3.6K$ to GND	All	$V_{CC}-1$		V
Output Voltage Low	V_{OL}	$R_{OUT}=3.6K$ to V_{CC}	+25°C		0.09	V
			+125°C		0.105	
			-55°C		0.080	
Short Circuit Output Current <u>1/</u>	$I_{O(SINK)}$	V_{OUT} to V_{CC} , ($V_{CC} = 5.0V$)	All	-30	-75	mA
	$I_{O(SOURCE)}$	V_{OUT} to GND, ($V_{CC} = 5.0V$)	All	45	55	mA
Slew Rate	SR	$R_L = 8K$, Gain = 1	+25°C	2.5		V/uS
			+125°C	2.2		
			-55°C	2.5		
Open Loop Gain	A_{OL}	No Load	+25°C	97		dB
			+125°C	92		
			-55°C	95		
Unity Gain Bandwidth	UGBW	$R_L = 10K$	+25°C	4.5		MHz
			+125°C	3.1		
			-55°C	5.4		
Channel Separation <u>1/</u>		$R_L = 2K$, $f = 1.0KHz$, ($V_{CC} = 5.0V$)	All	84		dB
Input-Referred Voltage Noise <u>1/</u>	e_n	$F = 5$ kHz, ($V_{CC} = 5.0V$)	All	15	15	nV/ \sqrt{Hz}
Phase Margin <u>1/</u>	Φ_m	No Load, ($V_{CC} = 5.0V$)	+25°C	30		Deg

Note:

1) Not Tested. Shall be guaranteed by design, characterization, or correlation to other test parameters.

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Radiation Electrical Performance Characteristics IIA

($T_C = +25^\circ\text{C}$, $+V_{CC} = +3.3\text{V} \pm 10\%$, $V_{EE} = \text{GND}$)

Parameter	Symbol	Test Conditions	MIN / MAX	100 krad(Si) <u>1/</u>	300 krad(Si) <u>2/</u>	650 krad(Si) <u>3/</u>	1 Mrad(Si) <u>4/</u>	Units
Supply Current	$+I_{CC}$	All Analog input = 0v, No Load	MIN	-	-	-	-	mA
			MAX	3.4	3.2	3.1	3	
Input Offset Voltage	V_{OS}		MIN	-2.8	-3.5	-3.8	-4.2	mV
			MAX	2.8	3.5	3.8	4.2	
Input Offset Current	I_{OS}		MIN	-100	-100	-200	-1500	pA
			MAX	100	100	200	1500	
Input Bias Current	I_B		MIN	-100	-100	-100	-700	pA
			MAX	100	100	100	700	
Common Mode Rejection Ratio	CMRR		MIN	59	54	51	50	dB
			MAX	-	-	-	-	
Power Supply Rejection Ratio	PSRR		MIN	51	47	46	46	dB
			MAX	-	-	-	-	
Output High Voltage	V_{OH}	$R_L = 3.6\text{K}$ to GND	MIN	$V_{CC}-0.1$	$V_{CC}-0.1$	$V_{CC}-0.1$	$V_{CC}-0.1$	V
			MAX	-	-	-	-	
Output Low Voltage	V_{OL}	$R_L = 3.6\text{K}$ to V_{CC}	MIN	-	-	-	-	V
			MAX	0.08	.079	0.078	0.078	
Slew Rate	SR	$R_L = 8\text{K}$ Gain = 1	MIN	1.9	1.45	0.91	0.75	V/us
			MAX	-	-	-	-	
Open Loop Gain	A_{OL}	No Load	MIN	90	86	84	83	dB
			MAX	-	-	-	-	
Unit Gain Bandwidth	UGBW	$R_L = 10\text{K}$	MIN	3.3	2.6	1.7	1.4	MHz
			MAX	-	-	-	-	

Notes:

- 1) RHA step level testing for this specification reflects Total Dose exposure at 100krad(Si) per method 1019, condition A of MIL-STD-883 @ +25°C.
- 2) RHA step level testing for this specification reflects Total Dose exposure at 300krad(Si) per method 1019, condition A of MIL-STD-883 @ +25°C.
- 3) RHA step level testing for this specification reflects Total Dose exposure at 650krad(Si) per method 1019, condition A of MIL-STD-883 @ +25°C.
- 4) RHA step level testing for this specification reflects Total Dose exposure at 1Mrad(Si) per method 1019, condition A of MIL-STD-883 @ +25°C.

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Radiation Electrical Performance Characteristics IIB

(T_c = +25°C, +V_{CC} = +5.0V ±10%, V_{EE} = GND)

Parameter	Symbol	Test Conditions	MIN / MAX	100 krad(Si) 1/	300 krad(Si) 2/	650 krad(Si) 3/	1Mrad(Si) 4/	Units
Supply Current	+I _{CC}	All Analog input = 0v, No Load	MIN	-	-	-	-	mA
			MAX	4.4	4.1	4	3.9	
Input Offset Voltage	V _{OS}		MIN	-3	-3.8	-4.5	-4.8	mV
			MAX	3	3.8	4.5	4.8	
Input Offset Current	I _{OS}		MIN	-100	-100	-200	-1500	pA
			MAX	100	100	200	1500	
Input Bias Current	I _B		MIN	-100	-100	-100	-700	pA
			MAX	100	100	100	700	
Common Mode Rejection Ratio	CMRR		MIN	70	68	66	66	dB
			MAX	-	-	-	-	
Power Supply Rejection Ratio	PSRR		MIN	72	71	70	69	dB
			MAX	-	-	-	-	
Output High Voltage	V _{OH}	R _L = 3.6K to GND	MIN	V _{CC} -0.1	V _{CC} -0.1	V _{CC} -0.1	V _{CC} -0.1	V
			MAX	-	-	-	-	
Output Low Voltage	V _{OL}	R _L = 3.6K to V _{CC}	MIN	-	-	-	-	V
			MAX	0.09	0.089	0.088	0.088	
Slew Rate	SR	R _L = 8K Gain = 1	MIN	2.4	2.2	2.0	1.9	V/us
			MAX	-	-	-	-	
Open Loop Gain	A _{OL}	No Load	MIN	95	92	90	90	dB
			MAX	-	-	-	-	
Unit Gain Bandwidth	UGBW	R _L = 10K	MIN	4.2	3.9	3.4	3.2	MHz
			MAX	-	-	-	-	

Notes:

- 1) RHA step level testing for this specification reflects Total Dose exposure at 100krad(Si) per method 1019, condition A of MIL-STD-883 @ +25°C.
- 2) RHA step level testing for this specification reflects Total Dose exposure at 300krad(Si) per method 1019, condition A of MIL-STD-883 @ +25°C.
- 3) RHA step level testing for this specification reflects Total Dose exposure at 650krad(Si) per method 1019, condition A of MIL-STD-883 @ +25°C.
- 4) RHA step level testing for this specification reflects Total Dose exposure at 1Mrad(Si) per method 1019, condition A of MIL-STD-883 @ +25°C.

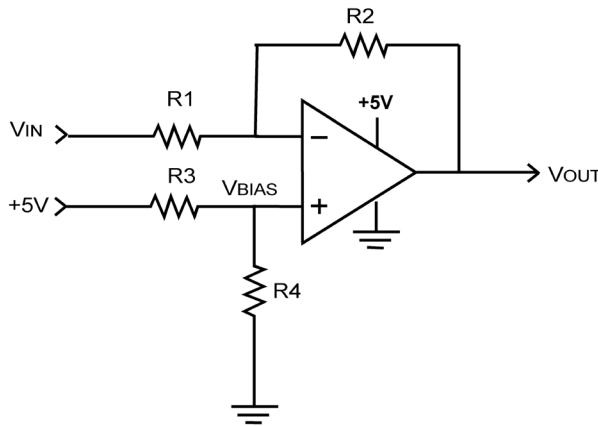
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RHD5900 Quad Operational Amplifier Application Notes

Application Note 1: Single Power Supply Amplifier

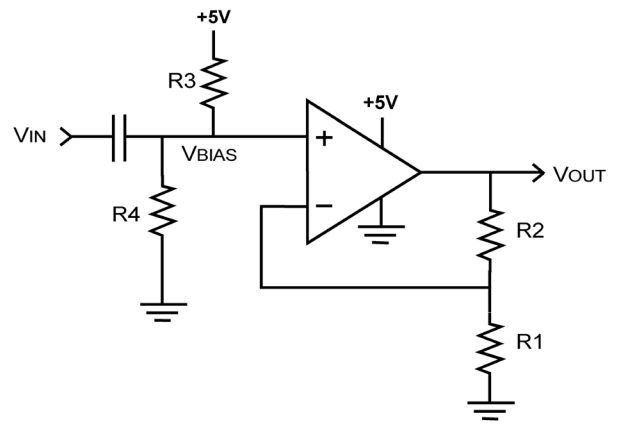
Inverting Amplifier

$$V_{OUT} = -V_{IN} \left(\frac{R_2}{R_1} \right)$$



Non Inverting Amplifier

$$V_{OUT} = V_{IN} \left(1 + \frac{R_2}{R_1} \right)$$



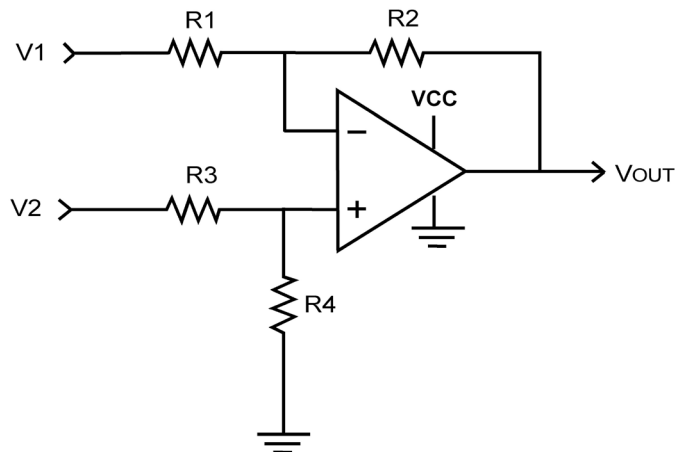
Note:

For V_{OUT} DC @ mid-range of common mode voltage range, $V_{BIAS} = 2.5 / (1 + R_2/R_1)$, $V_{BIAS} = +5 * R_4 / (R_3 + R_4)$

Application Note 2: Differential Input Amplifier

Differential Input Amplifier

$$V_{OUT} = \left(V_2 \left(\frac{R_4}{R_3 + R_4} \right) \left(1 + \frac{R_2}{R_1} \right) \right) - \left(V_1 \frac{R_2}{R_1} \right)$$



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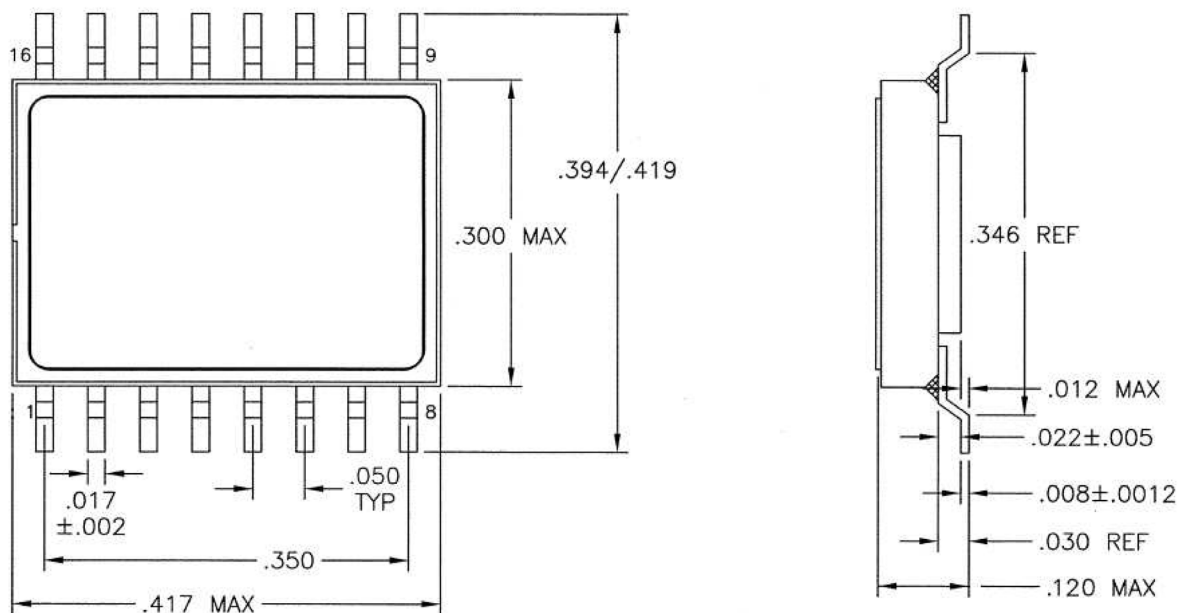


Figure 4: Package Outline

Note:

Package and lid are electrically isolated from signal pads.

Ordering Information

Model	DLA SMD #	Screening	Package
RHD5900-7	-	Commercial Flow, +25°C. testing only	16-pin SOIC Package
RHD5900-S	-	Military Temperature, -55°C to +125°C. Screened in accordance with the individual Test Methods of MIL-STD-883 for Space Applications	
RHD5900- 201-1S	5962-1024101KXC	In accordance with DLA SMD	
RHD5900- 201-2S	5962-1024101KXA		
RHD5900- 901-1S	5962H1024101KXC	In accordance with DLA Certified RHA Program Plan to RHA Level "H", 1 Mrad(Si)	
RHD5900- 901-2S	5962H1024101KXA		

Revision History

Date	Revision	Change Description
03/28/2016	H	Import into CAES format
05/14/2019	J	Add tables for 3.3v ±10% and 5.0v ±10% for Room Hot and Cold limits. Then add radiation limit tables for 3.3v ±10% and 5.0v ±10% for 100krad, 300krad, 650krad and 1Mrad. Add Diode Protection diagram. Update to the latest format. Add Titus.
06/13/2019	K	Revise the limits in the 3.3v Radiation table for the V _{OL} parameter
07/1/2019	L	Remove the Dual Power Supply comment in the Features. Change Pin-out 13 function to 'Power supply return'. Remove Note 1/ in tables 1A and 1B. Change note 2/ to 1/ in table 1B. Place parentheses around V _{CC} =5.0V in table 1B for note 1/ parameter conditions. Add V _{EE} = GND to tables IA, IB, IIA, IIB. Remove Application Note 1. Change Application Note 2 & 3 to Application Note 1 & 2.

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Datasheet Definitions

	DEFINITION
Advanced Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet is subject to change . Specifications can be TBD and the part package and pinout are not final .
Preliminary Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

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