DATASHEET

RELEASED 5/5/14

64-Channel Analog Multiplexer Module Radiation Tolerant & ESD Protected

ACT8501

Features

- 64-Channels provided by four 16-channel multiplexers
- Radiation performance
  - Total dose: 150 krads(Si), Dose rate = 50 - 300 rads(Si)/s
  - SEU: Immune up to 90 MeV-cm^2/mg
  - SEL: Immune by process design
- Full military temperature range
- Low power consumption < 60mW
- Two address buses (A0-3 & B0-3) and four enable lines afford flexible organization
- All channel inputs are protected by ±20V nominal Transorbs
- Fast access time < 500ns typical
- Break-Before-Make switching
- High analog input impedance (power on or off)
- Designed for aerospace and high reliability space applications
- Packaging – Hermetic ceramic
  - 96 leads, 1.32"Sq x 0.20"Ht quad flat pack
  - Typical Weight 15 grams
- **CAES Radiation Hardness Assurance Plan is DLA Certified to MIL-PRF-38534, Appendix G.**

General Description

CAES ACT8501 is a radiation tolerant, 64 channel multiplexer MCM (multi-chip module) with electrostatic discharge (ESD) protection on all channel inputs.

The ACT8501 has been specifically designed to meet exposure to radiation environments. It is available in a 96 lead High Temperature Co-Fired Ceramic (HTCC) Quad Flatpack (CQFP). It is guaranteed operational from -55°C to +125°C. Available screened in accordance with MIL-PRF-38534, the ACT8501 is ideal for demanding military and space applications.

Organization and Application

The ACT8501 consists of four 16 channel multiplexers arranged as shown in the Block Diagram. The ACT8501 design is inherently radiation tolerant.

A Section

Thirty-two (32) channels addressable by bus A_0~A_3, in two 16 channel blocks, each block enabled separately.

B Section

Thirty-two (32) channels addressable by bus B_0~B_3, in two 16 channel blocks, each block enabled separately.

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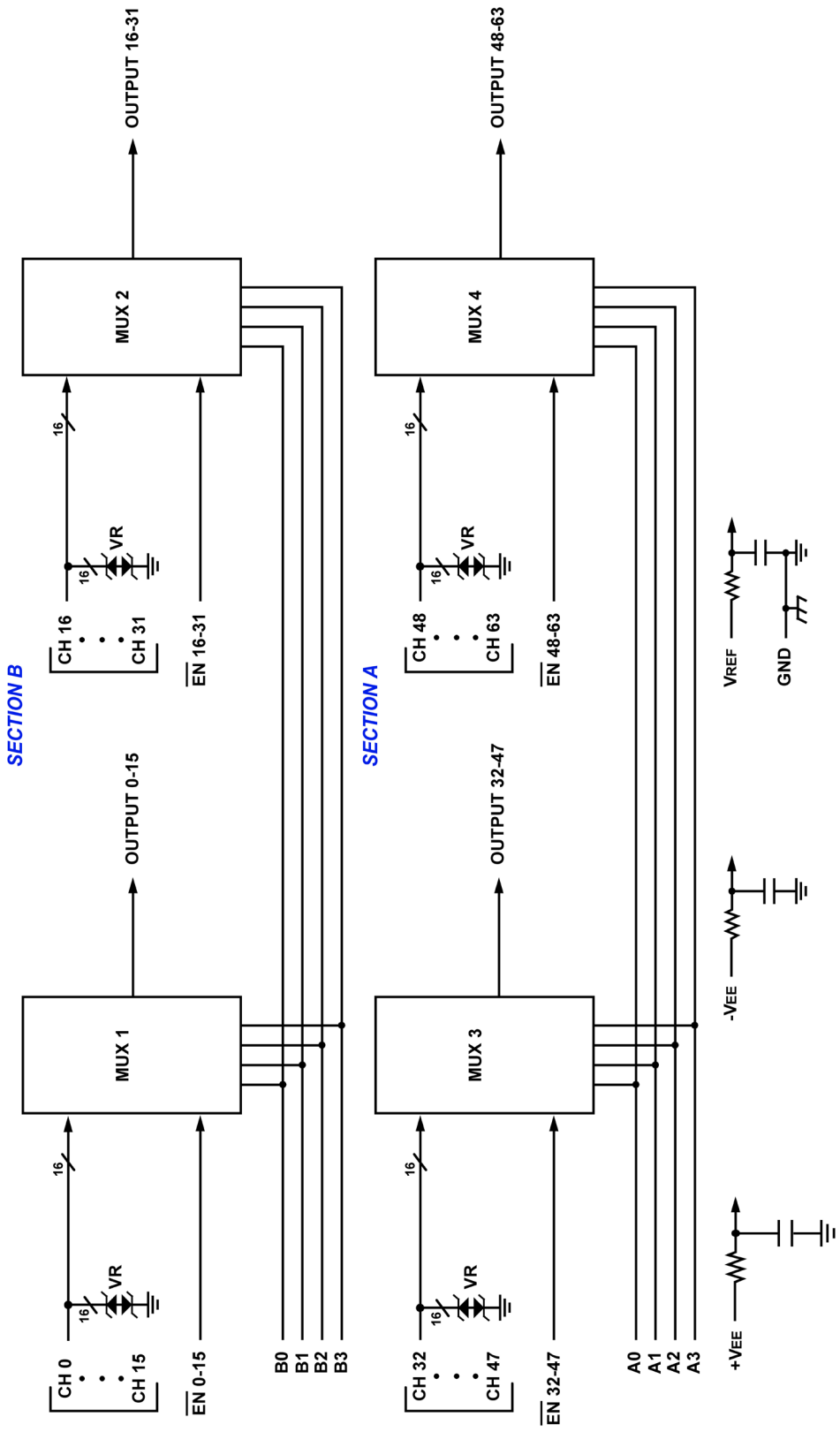

ACT8501 64 - Channel Analog Mux Block Diagram

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Absolute Maximum Ratings 1/

Parameter	Range	Units
Case Operating Temperature Range	-55 to +125	ºC
Storage Temperature Range	-65 to +150	ºC
Supply Voltage $+V_{EE}$ (Pin 44) $-V_{EE}$ (Pin 46) V_{REF} (Pin 48)	 +16.5 -16.5 +16.5	 V V V
Digital Input Overvoltage V_{EN} (Pins 5, 6, 91, 92), V_A (Pins 1, 3, 93, 95), V_B (Pins 2, 4, 94, 96)	< V_R +4 > GND -4	V V
Analog Input Over Voltage V_S	±18V	V

Note:

1) All measurements are made with respect to ground.

NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress rating only; functional operation beyond the "Operation Conditions" is not recommended and extended exposure beyond the "Operation Conditions" may affect device reliability.

Recommended Operating Conditions 1/

Symbol	Parameter	Typical	Units
$+V_{EE}$	+15V Power Supply Voltage	+15.0	V
$-V_{EE}$	-15V Power Supply Voltage	-15.0	V
V_{REF}	Reference Voltage	+5.00	V
V_{AL}	Logic Low Level	+0.8	V
V_{AH}	Logic High Level	+4.0	V

Note:

1) Power Supply turn-on sequence shall be as follows: $+V_{EE}$, $+V_{EE}$, followed by V_{REF}.

DC Electrical Performance Characteristics 1/

(T_C = -55°C to +125°C, $+V_{EE}$ = +15V, $-V_{EE}$ = -15V, V_{REF} = +5.0V - Unless otherwise specified)

Parameter	Symbol	Conditions	MIN	MAX	Units
Supply Current	$+I_{EE}$	$V_{EN}(0\text{-}63) = V_A(0\text{-}3)_A = V_A(0\text{-}3)_B = 0$	0.2	2	mA
	$-I_{EE}$		-2	-0.2	mA
	$+I_{SBY}$	$V_{EN}(0\text{-}63) = 4V, V_A(0\text{-}3)_A = V_A(0\text{-}3)_B = 0$ 6/	0.2	2	mA
	$-I_{SBY}$		-2	-0.2	mA
Address Input Current	$I_{AL}(0\text{-}3)_A$	V_A = 0V 1/, 7/	-2	2	µA
	$I_{AH}(0\text{-}3)_A$	V_A = 5V 1/, 7/	-2	2	µA
	$I_{AL}(0\text{-}3)_B$	V_B = 0V 1/, 7/	-2	2	µA
	$I_{AH}(0\text{-}3)_B$	$_{VB}$ = 5V 1/, 7/	-2	2	µA
Enable Input Current	$I_{ENL}(0\text{-}15)$	$V_{EN}(0\text{-}15)$ = 0V 7/	-1	1	µA
	$I_{ENH}(0\text{-}15)$	$V_{EN}(0\text{-}15)$ = 5V 7/	-1	1	µA
	$I_{ENL}(16\text{-}31)$	$V_{EN}(16\text{-}31)$ = 0V 7/	-1	1	µA
	$I_{ENH}(16\text{-}31)$	$V_{EN}(16\text{-}31)$ = 5V 7/	-1	1	µA
	$I_{ENL}(32\text{-}47)$	$V_{EN}(32\text{-}47)$ = 0V 7/	-1	1	µA
	$I_{ENH}(32\text{-}47)$	$V_{EN}(32\text{-}47)$ = 5V 7/	-1	1	µA
	$I_{ENL}(48\text{-}63$	$V_{EN}(48\text{-}63)$ = 0V 7/	-1	1	µA
	$I_{ENH}(48\text{-}63)$	$V_{EN}(48\text{-}63)$ = 5V 7/	-1	1	µA

DC Electrical Performance Characteristics 1/ (continued)

(T_C = -55°C to +125°C, $+V_{EE}$ = +15V, $-V_{EE}$ = -15V, V_{REF} = +5.0V - Unless otherwise specified)

Parameter	Symbol	Conditions		MIN	MAX	Units
Positive Input Leakage Current CH0-CH63	$+I_{SOFFOUTPUT}$(0-63)	V_{IN} = +10V, V_{EN} = 4V, output and all unused MUX inputs under test = -10V 2/, 3/, 7/		-100	+700	nA
				-100	+700	nA
Negative Input Leakage Current CH0-CH63	$-I_{SOFFOUTPUT}$(0-63)	V_{IN} = -10V, V_{EN} = 4V, output and all unused MUX inputs under test = +10V 2/, 3/, 7/		-100	+700	nA
				-100	+700	nA
Output Leakage Current OUTPUTS (pins 25, 26, 68 & 70)	$+I_{DOFFOUTPUT}$(0-63)	V_{OUT} = +10V, V_{EN} = 4V, output and all unused MUX inputs under test = -10V 3/, 4/, 7/		-100	+100	nA
Output Leakage Current OUTPUTS (pins 25, 26, 68 & 70)	$-I_{DOFFOUTPUT}$(0-63)	V_{OUT} = -10V, V_{EN} = 4V, output and all unused MUX inputs under test = +10V 3/, 4/, 7/		-100	+100	nA
Input Clamped Voltage CH0 - CH63	$+V_{CLMP}$(0-63)	V_{EN} = 4V, all unused MUX inputs under test are open. 3/	+25°C +125°C -55°C	18.0 18.0 17.5	23.0 23.5 22.5	V V V
Input Clamped Voltage CH0 - CH63	$-V_{CLMP}$(0-63)		+25°C +125°C -55°C	-23.0 -23.5 -22.5	-18.0 -18.0 -17.5	V V V
Switch ON Resistance OUTPUTS (pins 25,26, 68 & 70) 6/	$R_{DS(ON)(0-63)A}$	V_{IN} = +15V, V_{EN} = 0.8V, I_{OUT} = -1mA 2/, 3/, 5/		500	3000	Ω
	$R_{DS(ON)(0-63)B}$	V_{IN} = +5V, V_{EN} = 0.8V, I_{OUT} = -1mA 2/, 3/, 5/		500	3000	Ω
	$R_{DS(ON)(0-63)C}$	V_{IN} = -5V, V_{EN} = 0.8V, I_{OUT} = +1mA 2/, 3/, 5/		500	3000	Ω

Notes:

1) Measure inputs sequentially. Ground all unused inputs of the device under test. V_A is the applied input voltage to the address lines A(0-3). V_B is the applied input voltage to the address lines B(0-3).
2) V_{IN} is the applied input voltage to the input channels CH0-CH63.
3) V_{EN} is the applied input voltage to the enable lines EN (0-15), EN (16-31), EN (32-47) and EN (48-63).
4) V_{OUT} is the applied input voltage to the output lines OUTPUT(0-15), OUTPUT(16-31), OUTPUT(32-47), OUTPUT(48-63).
5) Negative current is the current flowing out of each of the MUX pins. Positive current is the current flowing into each MUX pin.
6) If not tested, shall be guaranteed to the specified limits.
7) These parameters for Tc = -55°C are guaranteed by design, characterization, or correlation to other test parameters but not production tested.

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Switching Characteristics

(Tc = -55°C to +125°C, $+V_{EE}$ = +15V, $-V_{EE}$ = -15V, V_{REF} = +5.0V - Unless otherwise specified)

Parameter	Symbol	Conditions	MIN	MAX	Units
Switching Test MUX	t_AHL	R_L = 10KΩ, C_L = 50pF	10	1500	ns
	t_ALH	R_L = 10KΩ, C_L = 50pF Tc = +25°C, +125°C Tc = -55°C	 10 10	 2000 5000	 ns ns
	$t_{ON}EN$	R_L = 1KΩ, C_L = 50pF	10	1000	ns
	$t_{OFF}EN$	R_L = 1KΩ, C_L = 50pF	10	1000	ns

Truth Table (CH0 – CH15)

B3	B2	B1	B0	EN(0-15)	"ON" Channel 1/
X	X	X	X	H	NONE
L	L	L	L	L	CH0
L	L	L	H	L	CH1
L	L	H	L	L	CH2
L	L	H	H	L	CH3
L	H	L	L	L	CH4
L	H	L	H	L	CH5
L	H	H	L	L	CH6
L	H	H	H	L	CH7
H	L	L	L	L	CH8
H	L	L	H	L	CH9
H	L	H	L	L	CH10
H	L	H	H	L	CH11
H	H	L	L	L	CH12
H	H	L	H	L	CH13
H	H	H	L	L	CH14
H	H	H	H	L	CH15

1/ Between CH0-15 and OUTPUT (0-15)

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Truth Table (CH16 – CH31)

B3	B2	B1	B0	EN(16-31)	"ON" Channel 1/
X	X	X	X	H	NONE
L	L	L	L	L	CH16
L	L	L	H	L	CH17
L	L	H	L	L	CH18
L	L	H	H	L	CH19
L	H	L	L	L	CH20
L	H	L	H	L	CH21
L	H	H	L	L	CH22
L	H	H	H	L	CH23
H	L	L	L	L	CH24
H	L	L	H	L	CH25
H	L	H	L	L	CH26
H	L	H	H	L	CH27
H	H	L	L	L	CH28
H	H	L	H	L	CH29
H	H	H	L	L	CH30
H	H	H	H	L	CH31

1/ Between CH16-31 and OUTPUT (16-31)

Truth Table (CH32 – CH47)

A3	A2	A1	A0	EN(32-47)	"ON" Channel 1/
X	X	X	X	H	NONE
L	L	L	L	L	CH32
L	L	L	H	L	CH33
L	L	H	L	L	CH34
L	L	H	H	L	CH35
L	H	L	L	L	CH36
L	H	L	H	L	CH37
L	H	H	L	L	CH38
L	H	H	H	L	CH39
H	L	L	L	L	CH40
H	L	L	H	L	CH41
H	L	H	L	L	CH42
H	L	H	H	L	CH43
H	H	L	L	L	CH44
H	H	L	H	L	CH45
H	H	H	L	L	CH46
H	H	H	H	L	CH47

1/ Between CH32-47 and OUTPUT (32-47)

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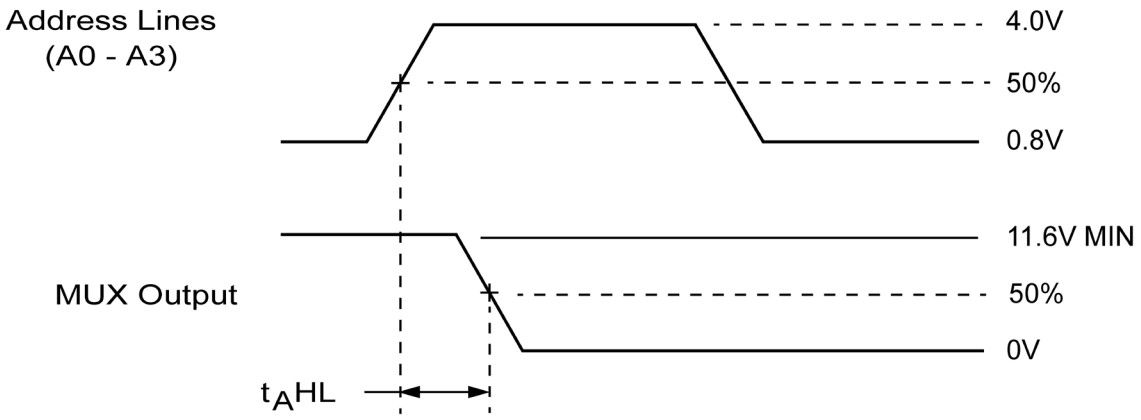
Truth Table (CH48 – CH63)

A3	A2	A1	A0	EN(48-63)	"ON" Channel 1/
X	X	X	X	H	NONE
L	L	L	L	L	CH48
L	L	L	H	L	CH49
L	L	H	L	L	CH50
L	L	H	H	L	CH51
L	H	L	L	L	CH52
L	H	L	H	L	CH53
L	H	H	L	L	CH54
L	H	H	H	L	CH55
H	L	L	L	L	CH56
H	L	L	H	L	CH57
H	L	H	L	L	CH58
H	L	H	H	L	CH59
H	H	L	L	L	CH60
H	H	L	H	L	CH61
H	H	H	L	L	CH62
H	H	H	H	L	CH63

1/ Between CH48-63 and OUTPUT (48-63)

ACT8501 Switching Diagrams



Definition of t_AHL

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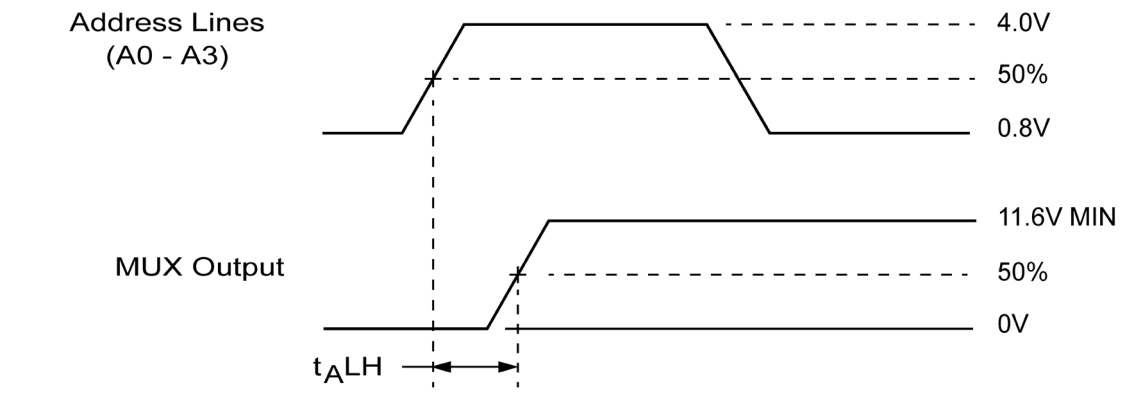
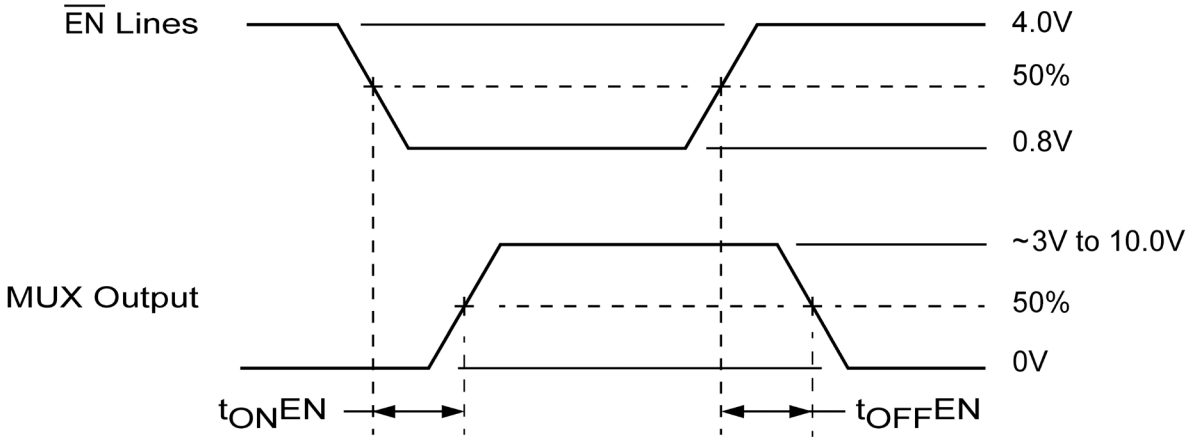


Definition of t_ALH



Definition of $t_{ON}EN$ and $t_{OFF}EN$
ACT8501 Switching Diagrams

Note: f = 10KHz, Duty cycle = 50%.

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Pin Numbers & Functions

ACT8501 – 96 Leads Ceramic QUAD Flat Pack					
Pin #	**Function**	**Pin #**	**Function**	**Pin #**	**Function**
1	A2	33	CH11	65	CH49
2	B2	34	CH27	66	CH48
3	A3	35	CH12	67	NC
4	B3	36	CH28	68	Output V(48-63)
5	$\overline{EN}$ 0-15	37	CH13	69	NC
6	$\overline{EN}$ 16-31	38	CH29	70	Output V(32-47)
7	CH0	39	CH14	71	GND
8	CH16	40	CH30	72	GND
9	CH1	41	CH15	73	CH47
10	CH17	42	CH31	74	CH46
11	CH2	43	NC	75	CH45
12	CH18	44	$+V_{EE}$	76	CH44
13	CH3	45	NC	77	CH43
14	CH19	46	$-V_{EE}$	78	CH42
15	CH4	47	NC	79	CH41
16	CH20	48	V_{REF}	80	CH40
17	CH5	49	NC	81	CH39
18	CH21	50	CASE GND	82	CH38
19	CH6	51	CH63	83	CH37
20	CH22	52	CH62	84	CH36
21	CH7	53	CH61	85	CH35
22	CH23	54	CH60	86	CH34
23	GND	55	CH59	87	CH33
24	GND	56	CH58	88	CH32
25	Output V(0-15)	57	CH57	89	GND
26	Output V(16-31)	58	CH56	90	GND
27	CH8	59	CH55	91	$\overline{EN}$ 48-63
28	CH24	60	CH54	92	$\overline{EN}$ 32-47
29	CH9	61	CH53	93	A0
30	CH25	62	CH52	94	B0
31	CH10	63	CH51	95	A1
32	CH26	64	CH50	96	B1

Note: It is recommended that all "NC or "no connect pin" be grounded. This eliminates or minimizes any ESD or static buildup.

64-Channel Analog Multiplexer Module Radiation Tolerant & ESD Protected

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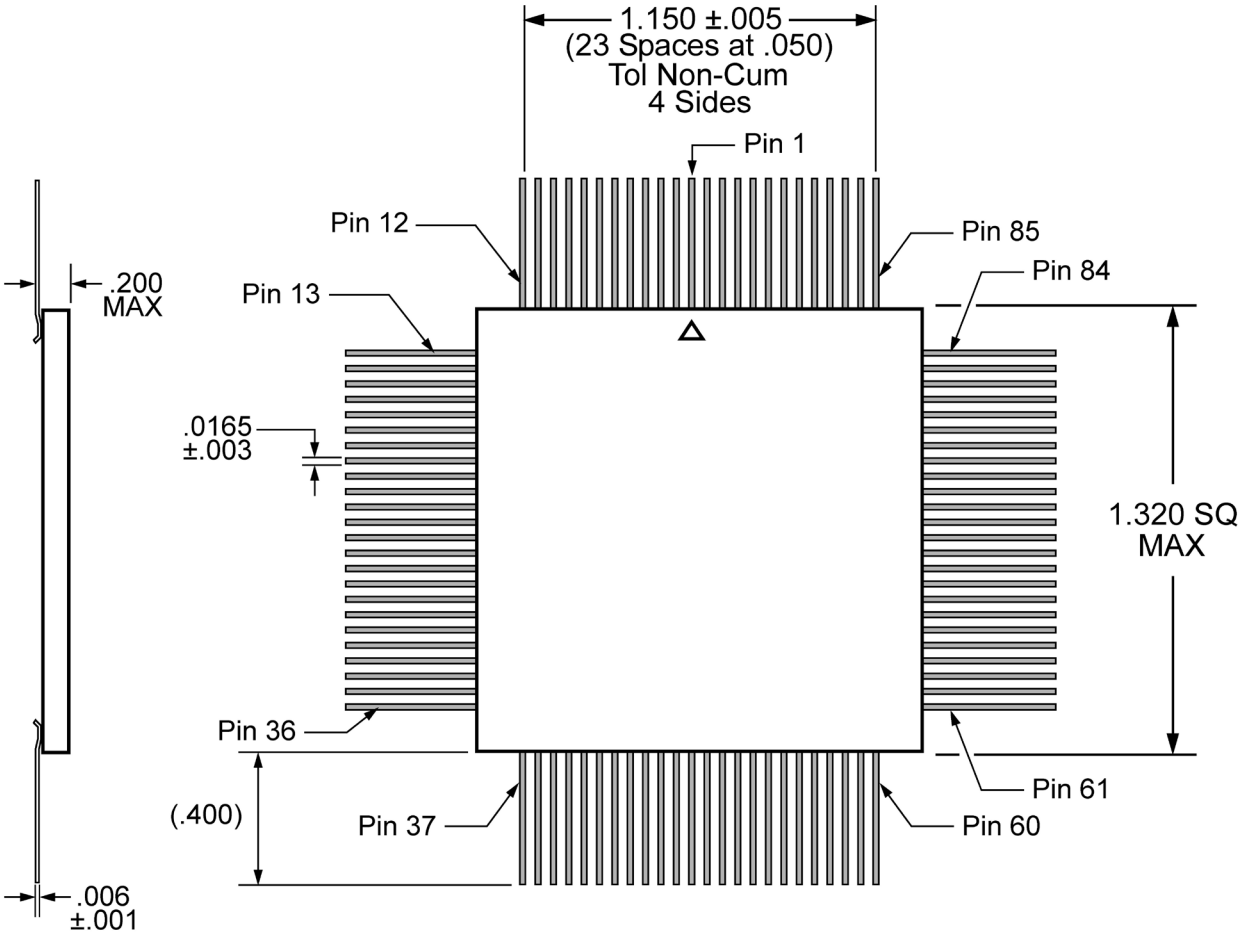
Ordering Information

Model Number	DLA SMD #	Screening	Package
ACT8501-7	-	Commercial Flow, +25°C testing only	QUAD Flat Pack
ACT8501-S	5962-0050202KXC	In accordance with DLA SMD	
ACT8501-901-1S	5962F0050202KXC	In accordance with DLA Certified RHA Program Plan to RHA Level "F", 300krads(Si)	



Flat Package Outline

Note: Outside ceramic tie bars not shown for clarity. Contact factory for details.

64-Channel Analog Multiplexer Module Radiation Tolerant & ESD Protected

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Datasheet Definitions

	DEFINITION
Advanced Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet **is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final**.
Preliminary Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

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