DATASHEET

RELEASED 6/23/17

Generation 6 SBC Design Specification

DS4350272-X00

Flight Model: AX9-4350272-30X

1.0 Scope

This specification describes the performance, design, fabrication, assembly, test, and verification of the Generation 6 Single Board Computer, hereinafter referred to as the GEN 6 SBC. The GEN 6 SBC is a general-purpose cPCI SBC card.

1.1 Conventions and Operational Definitions are as follows:

The words "shall", "will", "should", and "may" are used in this document as defined in this paragraph.

- "Shall" is used whenever a specification or requirement is binding on all versions of the SBC.
- "Should" and "may" are used when necessary to express non-mandatory provisions that apply to one or more versions of the SBC.
- "Will" is used to express a declaration of purpose and is used when the simple future tense is required for clarity.

1.1.1 Signal Naming Convention

Signal names throughout this document follow the convention described in this section.

A signal name by itself represents an active high signal, i.e. "SIGNALA". A signal name with a "#" suffix represents an active low signal, i.e. "SIGNALA#".

The backplane connection consists of the mechanical and electrical design using the compact PCI (cPCI) standard (J1 and J2 populated).

1.1.2 Measurement Units

The metric unit system will be the standard used throughout this specification document. All seller supplied documents and measurements are expected to be in English or Metric units.

1.1.3 GEN 6 Single Board Computer EM, FM Designations

Several models of the GEN 6 SBC's can be manufactured based on the usage purpose, delivery schedule, mass, and cost. The following types of assemblies are identified:

a) Flight Modules (FM): Designated by a -3xx in the part number, the FMs are used in spacecraft final production. These units meet full specifications.

b) Engineering Model (EM): Designated by a -1xx in the part number, the EMs are flight-like units used in the flight design checkout, software development and qualification, upper assembly unit checkout and initial flight unit integration (pre-environmental). EMs meet full design specifications less the Flight Parts and board level environmental tests/screening.

1.1.4 GEN 6 Single Board Computer Versions

Several versions of the GEN 6 SBC's can be manufactured based on the end user system requirements. An ordering example for a Flight Model UT700, 132MHz main clock SBC would be, AX9-4350272-304. An outline for the different versions of the GEN 6 SBC assemblies is as follows:

Table 1: Single Board Computer Configuration and DMIPS Estimate

Conditions: cPCI active/Memory Access [Typical = no access | Max = 50%], All other IP functions disabled via clock gating register

Flight Model AX9-4350272	LEON	Sys Clk (MHz)	AMBA Clk (MHz)	Memory wait states	DMIPS	SPW Clk (MHz)	Typical Power (W)	Max Power (W)
-xx0*	UT699E	33	33	0	44.2	33	3.0	5.1
-xx1	UT699E	66	66	3	70.4	132	3.5	6.6
-xx2*	UT700	33	33	0	44.2	33	3.0	5.1
-xx3*	UT700	66	66	3	70.4	132	3.5	6.6
-xx4	UT700	132	66	3	94.9	132	4.2	7.3

1.2 GEN 6 Single Board Computer DMIPS/Power

The target DMIPS/Power and associated dash number is shown in **Table 1**. All values are estimated based on the data sheet values for the major power IC's that contribute to the SBC's power profile. **Figure 1** shows all available SBC configuration options for each dash-number listed.

2.0 Applicable Documents

2.1 Military Standards and Specifications

EEE-INST-002	Instructions for EEE Parts Selection, Screening, Qualification, and Derating
MIL-HDBK-217	Reliability Prediction of Electronic Equipment
MIL-STD-461E	Requirements for the Control of Electromagnetic Interference Characteristics of Subsystems and Equipment
MIL-STD-1629	Procedures for Performing a Failure Mode, Effects, and Criticality Analysis
NASA-STD 8739.3	Soldered Electrical Connections

2.2 GEN 6 Specifications

DS4350272-xxx GEN 6 SBC Design Specification

2.3 Other Specifications and Standards

cPCI 2.0 Rev 3.0	PICMG - Compact Peripheral Component Interconnect, Specification 2.0 Rev 3.0 (Oct. 1, 1999)
PCI -2.2	PCI-SIG - PCI Local Bus Specification Rev 2.2 (Dec. 18, 1998)
311P822	Hypertronics cPCI Connectors, NASA Goddard Series Designation. Quality Conformance Inspection: NASA GSFC S-311-P-822 Table II
IPC-2221	Generic Standard on Printed Board Design
IPC-2222	Sectional Design Standard for Rigid Organic Printed Boards
IPC-6012	Qualification and Performance Specification for Rigid Printed Boards
46500010-001	Frame, Support, PCB

2.4 Reference Documents

The following documents are for reference only and compliance with these documents or their sections are as specified in this document.

M8513/10F02NP	Glenair 37-pin Connector (J3), micro-D socket-type
K2A110FMDTBH	Hypertronix cPCI J1
K2B110FMDTBH	Hypertronix cPCI J2
M83513/04-A11N	Glenair 9-pin Connector, Micro-D type (P1 & P2)

3.0 Requirements GEN 6 LEON Version

The GEN 6 SBC described within this specification will pass all of the examinations, analyses, and tests specified in this document.

All Seller supplied documents/drawings use the English unit system for measurements of dimensions and the metric unit system for all other measurements.

The Printed Circuit Board (PCB) are designed to IPC Class 3A specifications. Flight units are conformal coated and staked.

3.1 GEN 6 SBC Overview and Definition

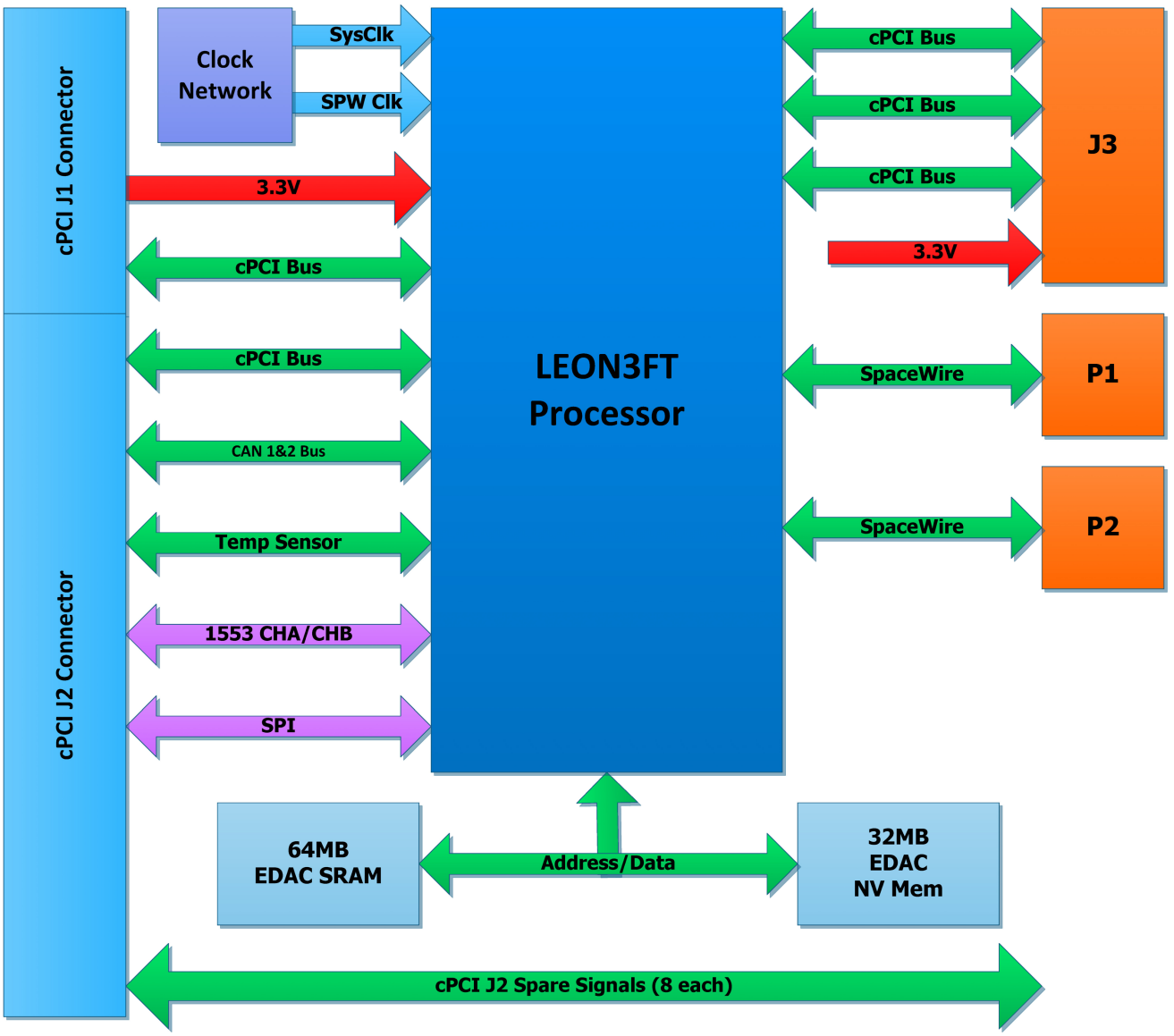
The GEN 6 SBC is a Fault Tolerant master single board computer, based on the standard 3U (3.94 inches x 6.3 inches) form factor and an CAES LEON 3FT processor. The GEN 6 SBC contains the following

- 64MB of SRAM (EDAC Protected)
- 32MB of Non-volatile memory (EDAC Protected)
- Two cPCI (J1/J2) bus I/F connectors (Hypertronix Flight Type)
  - Eight cPCI spare signals
  - Two 3.3V LVTTL CAN Bus Channels
  - One 3.3V LVTTL UT700 SPI port (**UT700 only**)
  - Two 3.3V LVTTL UT700 1553B (CHA & CHB) ports (**UT700 only**)
- One front panel test connector (J3)
  - 3.3 VDC & Ground
  - One single-ended I/F to the UART
  - One Ethernet MII bus to MAC
  - One Debug Support Unit (DSU) I/F
- Two front panel SpaceWire connectors (P1 & P2)
- GPIOs 6-9 interfaces

3.1.1 Functional Block Diagram and Design Concepts

A block diagram of the GEN 6 SBC is shown in **Figure 1**.

- The LEON processor main input clock rate, refer to **Table 1**.
- The SpaceWire bus Transmit Clock rate, refer to **Table 1**.
- The processor module provides the SPI port signals to J2 (**UT700 only**)
- The processor module provides the 1553B port signals to J2 (**UT700 only**)
- The processor module implements software configurable watchdog timer utilizing processor Timer 4.
- The processor design is capable of disabling Error Detection and Correction (EDAC) through the J3 connector.
- The GEN 6 SBC operates as a 33 MHz, 32 bit cPCI System Slot 1, locally incorporates the cPCI bus arbitration, and supplies the 33MHz cPCI clocks to the J1 and J2 cPCI backplane connectors.



Processor: UT699E or UT700
1553 and SPI: **UT700 only**

Figure 1: GEN 6 SBC Block Diagram

3.2 SBC System Power

The GEN 6 SBC design power contained in the following section includes the two SpaceWire functions operating at the indicated clock rate, see **Table 1**.

3.2.1 Power Consumption

- The total power consumption for the board does not include the power consumed by the customer's debug interface when connected to J3 connector
- The GEN 6 processor module power goal and DMIPS estimates are contained in **Table 1**.

3.3 SBC System Clocking

A functional block diagram of the GEN 6 SBC clock network is shown in **Figure 2**, illustrating the clock network manager's primary functions and electrical interfaces.

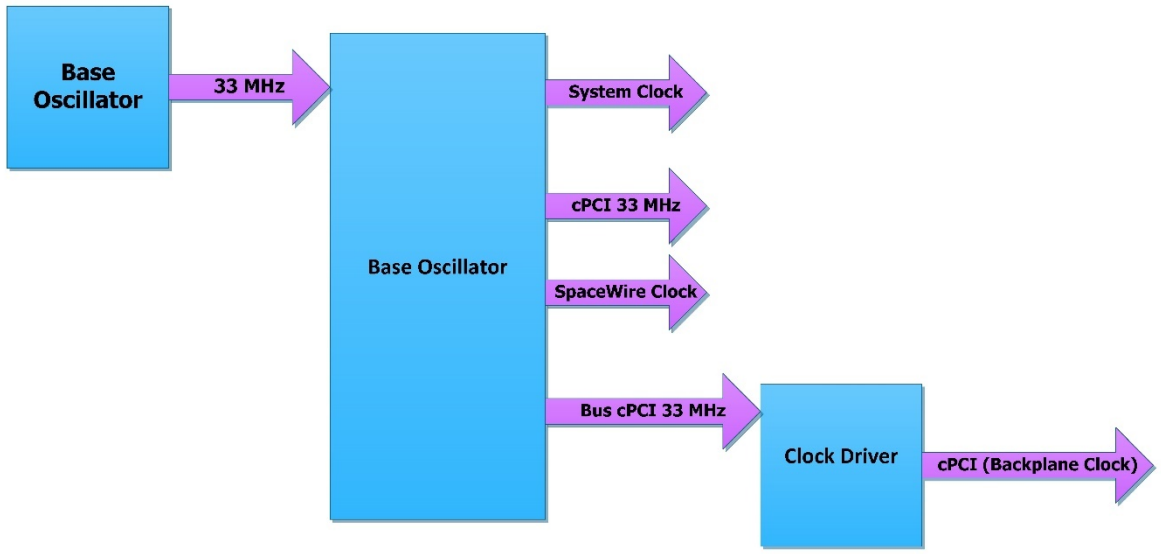


Figure 2: Clock Network Block Diagram

Note:

1) See Table 1 for System and SpaceWire Clock frequencies.

3.3.1 Base Oscillator Characteristics

The 33MHz oscillator used for the base clock has a total minimum frequency/temperature stability of +/- 50 ppm over - 55°C to +125°C. The final clock output tolerance including cycle- to- cycle jitter for stage 1 clock generator is 52 ps (stage 1 device jitter added to +/- 50 ppm).

3.3.2 Clock Network Architecture

The basic architecture for system clock generation is separated into two stages. Stage 1 receives the input clock (one input load) from the base 33MHz oscillator. The subsequent outputs from Stage 1 and 2 produce the derived output clock frequencies needed for the cPCI backplane and other local devices. Total clock- to- clock signal skew for cPCI J1/J2 (CLK0, CLK1, CLK2, CLK3, CLK4, CLK5, CLK6, including the local LEON PCI input clock), due to jitter and component delays are 800 ps or less.

3.3.3 LEON 3FT Main Input Clock

Refer to Table 1 for LEON system clock frequency, memory access wait-states and DMIPS estimates.

3.3.4 LEON 3FT cPCI Input Clock

33MHz via clock network manager see **Figure 2.**

3.3.5 LEON 3FT SpaceWire Receive Clock

Refer to **Table 1** for different LEON SBC clock settings.

3.4 LEON 3FT GPIO Assignments

The GPIO Assignments are outlined in **Table 2**. **GPIOs highlighted in red** indicates the GPIO pins are inputs to the LEON and should not be set to output mode via the LEON GPIO command register.

Table 2: GPIO Assignments

GPIO	Function	SBC Actions
0	Set the width of the data bus	Set by board @reset & POR
1	Set the width of the data bus	Set by board @reset & POR
2	EDAC Enable	(Active High) J3 I/F can disable the EDAC (reset required if changed). Pulled-up at reset/POR to enable EDAC by default
3	WDTO reset Indicator	Indicates a WDT reset occurred (WDT must be enabled and a time out condition must occur)
4	WDTO reset Indicator Clear	(Active Low --momentary) clears the WDTO indicator register (Pulled-up with reset/POR)
5	WDTO hardware disable	(Active High) On power-up/reset this GPIO is pulled-up and will mask the LEON WDT signal, set this GPIO low to allow the WDT signal to generate a board reset
6	J3 Test I/F "GPIO6"	GPIO6 (Output) can be used by software (I/F POD, header & LED illuminated by setting GPIO to low) for ground development
7	J3 Test I/F "GPIO7"	GPIO7 (Output) can be used by software (I/F POD, header & LED illuminated by setting GPIO to low) for ground development
8	J3 Test I/F "GPIO8"	GPIO8 (Output) can be used by software (I/F POD, header & LED illuminated by setting GPIO to low) for ground development
9	J3 Test I/F "GPIO9"	GPIO9 (Output) can be used by software (I/F POD, header & LED illuminated by setting GPIO to low) for ground development
10	Software Controlled Reset	(Active Low) If set low, will issue a hardware reset to SBC
11	INT A	cPCI Bus INT A
12	INT B	cPCI Bus INT B
13	INT C	cPCI Bus INT C
14	INT D	cPCI Bus INT D
15	cPCI Reset	Set active (Low to cPCI J1-C5) via pull-up on GPIO (inverted to cPCI J1-C5) after reset/POR. Set GPIO15 low to release cPCI reset

4.0 GEN 6 Specifications

4.1 cPCI 33 MHZ Backplane Source Clocks

- 33MHz is distributed to the cPCI backplane through a clock driver device.
- Maximum skew tolerance of 800ps maximum is maintained between all routed cPCI clock traces including each cPCI J2 & J1 receiving the 33MHz cPCI master clock and the local UT699E/UT700 33MHz cPCI input

4.2 Processor Local Memory

The GEN 6 processor will have directly- coupled SRAM and NVRAM. The initial memory LEON (UT699E/700) configuration register setting is contained in **Table 3**.

Table 3: Memory Configuration

Register Name	APB Address	Value (Hex)
MCFG1	0x8000_0000	0x0003_CA33
MCFG2	0x8000_0004	0x0000_166F
MCFG3	0x8000_0008	0x0000_0300

4.2.1 Memory Organization and Architecture

The architecture for the design assumes the NVRAM will contain the portions of the O/S Kernel that are transferred into the local SRAM after a power- up or reset condition occurs. All subsequent processor operations and the main O/S execution will be from and to the SRAM memory.

- The processor module contains 64 MB of EDAC protected volatile memory.
- The processor module contains 32 MB of EDAC protected non-volatile memory.

4.3 cPCI Bus Interface

Since the SBC will operate as a System Slot processor, both J1 and J2 connectors will be utilized for cPCI bus operations. Geographical Addressing (GA) is not implemented.

4.3.1 cPCI Design Considerations

- The backplane 5.0 VDC input is not required by the GEN 6 SBC. A 33uF Tantalum Capacitor is provided on the GEN 6 SBC 5 Volt cPCI input pins as directed in the cPCI 2.0 specification, a single 10K ohm resistor shall be connected between the cPCI 5VDC and GND rails. If applied to the GEN 6 SBC from the backplane, the 5 Volt supply regulation is 5.0 VDC +/- 5%.
- The backplane 3.3 VDC Input voltage level utilized in the design is 3.3V +/- 5%.
- The backplane I/O signal voltage level utilized in the design is 3.3 VDC +/- 5%.
- The backplane +/- 12V is not required for the GEN 6 SBC operation and is not connected to the SBC backplane.
- The GEN 6 SBC has a board characteristic impedance of 65 ohms +/- 10% for all PCB traces that connect to the J1 and J2 cPCI I/F.
- The GEN 6 SBC Board signal stub length is less than or equal to 2.5 inches for all signals connected between the UT700/UT699E's cPCI I/F and the J1/J2 cPCI backplane connectors.
- Stub termination includes a 10 ohm +/- 10%, series termination resistor located on the board at the cPCI connector interface. The signals that are terminated are: AD0-AD31, CBE0#- CBE3#, PAR, FRAME#, IRDY#, TRDY#, STOP#, LOCK#, IDSEL, DEVSEL#, PERR#, SERR#, INTA#, INTB# and RST#.

- The series termination resistor are placed within 0.6 inches of the signal's connector pin; this length shall be included in the overall length of trace.
- Each GNT# signal supplied by the GEN 6 SBC is series terminated at the driver (UT700/UT699E) with a resistor matched to the driving buffer output characteristics.

4.3.2 Additional GEN 6 SBC cPCI Specifications

Additional GEN 6 SBC requirements are incorporated for J1 and J2; these signals are referred to as the "Spare cPCI" signals. These modifications to the design architecture conflict with the signaling designated for other purposes by the PICMG 2.0 CompactPCI Specification (employed on 64- bit cPCI backplane signal connections). As a result, the GEN 6 SBC cPCI is not compatible with 64 bit cPCI implementations.

- The backplane J1 and J2 Connectors are flight-type Hypertronics connectors.
- The processor module accepts a power on reset (active-low) signal from the cPCI J2 connector on pin J2 pin C17 (PRST#).
- The GEN 6 SBC accepts a reset (1uS minimum) signal (3.3 VDC - inactive, Ground - active) on J2 pin C17 (PRST#), will be active low, and will behave as a total system reset when active, causing the UT699E/UT700 to boot from the on-board NVRAM.
- The GEN 6 SBC provides a reset (active low) signal to the cPCI peripheral cards on J1 pin C5 (RST#).
- The GEN 6 SBC provides a temperature monitor signal set to J2 pin D21 (+) and J2 pin E21 (-), part number 311P18-01S7R6 (YSI Temperature Sensor). The temperature sensor is located under the UT699E/UT700 processor on the opposite side of the PCB.

4.3.3 CompactPCI J1 Connector Definition

The J1 cPCI connector is outlined in **Figure 3**.

Pin #	Signal Name Row A	Signal Name Row B	Signal Name Row C	Signal Name Row D	Signal Name Row E	Signal Name Row F
25	*5V	REQ64#	ENUM#	3.3VDC	*5V	GND
24	AD[1]	*5V	3.3VDC	AD[0]	ACK64#	GND
23	3.3VDC	AD[4]	AD[3]	*5V	AD[2]	GND
22	AD[7]	GND	3.3VDC	AD[6]	AD[5]	GND
21	3.3VDC	AD[9]	AD[8]	M66EN	C/BE[0]#	GND
20	AD[12]	GND	3.3VDC	AD[11]	AD[10]	GND
19	3.3VDC	AD[15]	AD[14]	GND	AD[13]	GND
18	SER#	GND	3.3VDC	PAR	C/BE[1]#	GND
17	3.3VDC	NC	SBO#	GND	PERR#	GND
16	DEV SEL#	GND	3.3VDC	STOP#	LOCK#	GND
15	3.3VDC	FRAME#	IRDY#	GND	TRDY#	GND
14	NC	NC	NC	NC	NC	NC
13	NC	NC	NC	NC	NC	NC
12	NC	NC	NC	NC	NC	NC
11	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND
10	AD[21]	GND	3.3VDC	AD[20]	AD[19]	GND
9	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	GND
8	AD[26]	GND	3.3VDC	AD[25]	AD[24]	GND
7	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
6	REQ#	GND	3.3VDC	CLK	AD[31]	GND
5	NC	NC	RST#	GND	GNT#	GND
4	NC	gnd	3.3VDC	NC	NC	GND
3	INTA#	INTB#	INTC#	*5V	INTD#	GND
2	NC	*5V	NC	NC	NC	GND
1	*5V	NC	NC	NC	*5V	GND

Figure 3: cPCI J1 Pin Assignment

*5V not used by SBC, a 33uF capacitor is installed on SBC for cPCI bus in parallel with a 10K ohm resistor pulldown to GND supplied on the SBC

All SBC Dash Number Versions (x00-x04)

4.3.4 CompactPCI J2 Connector Definition

The J2 cPCI connector is outlined in Figure 4.

Pin#	Signal Name					
	Row A	Row B	Row C	Row D	Row E	Row F
22	NC	NC	NC	NC	NC	GND
21	CLKB	GND	NC	Temp(+)	Temp(-)	GND
20	CLK5	GND	NC	NC	NC	GND
19	GND	GND	NC	NC	NC	GND
18	NC (SPARE5)	NC	NC	NC	NC	GND
17	NC (SPARE4)	NC	PRST#	REQ6#	GNT6#	GND
16	NC (SPARE3)	NC	NC	GND	NC	GND
15	NC (SPARE2)	NC	NC	REQ5#	GNT5#	GND
14	GND 10KΩ 1553RXA	NC	CAN1RX	GND	GND 10KΩ 1553RXENB	GND
13	GND 10KΩ 1553RXA#	GND	3.3VDC	NC	GND 10KΩ 1553RXB	GND
12	GND 10KΩ 1553RXENA	NC	CAN1TX	GND	GND 10KΩ 1553RXB#	GND
11	GND 10KΩ 1553TXA	GND	3.3VDC	NC	NC	GND
10	GND 10KΩ 1553TXA#	NC (SPARE8)	CAN2RX	GND	GND 10KΩ SPIMOSI	GND
9	GND 10KΩ 1553TXINHA	NC	3.3VDC	NC	GND 10KΩ SPIEN	GND
8	GND 10KΩ 1553TXINHB	NC (SPARE7)	CAN2TX	GND	3.3V 10KΩ SPIMISO	GND
7	GND 10KΩ 1553TXB	GND	3.3VDC	NC	3.3V 10KΩ SPICLK	GND
6	GND 10KΩ 1553TXB#	NC (SPARE6)	NC	GND	NC	GND
5	NC (SPARE1)	GND	3.3VDC	NC	GND 10KΩ 1553CLK	GND
4	3.3VDC	NC	NC	NC	NC	GND
3	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
2	CLK2	CLK3	GND	GNT2#	REQ3#	GND
1	CLK1	GND	REQ1#	GNT1#	REQ2#	GND

Highlighting depicts non-standard cPCI signals

UT699E SBC Versions (-x00, -x01)

UT700 SBC Versions (-x02, -x03, -x04)

Figure 4: cPCI J2 Pin Assignment

4.4 cPCI REQ# and GNT# Assignments

Since the GEN 6 SBC operates in the System Slot of the cPCI backplane, it must host the arbitration for the full complement of REQ#/GNT# signals.

4.4.1 cPCI REQ# and GNT# Mapping

Each Peripheral Board interfaces to one pair of REQx#/GNTx# signals using pins called REQ# (J1:A6) and GNT# (J1:E5). **Figure 5**, "System to Logical Slot Signal Assignments (Typical)," lists the backplane assignment of request/grant signals from the GEN 6 SBC to each board's REQ# and GNT# pins.

The GEN 6 SBC supports seven pairs of REQx#/GNTx# signals.

Signal	Connector: Pin	Signal	Connector: Pin
System Slot (Δ), Logical Slot 1		Peripheral Slot (O), Logical Slot 2	
AD31	P1:E6	IDSEL[1]	P1:B9
REQ0#	P1:A6	REQ#	P1:A6
GNT0#	P1:E5	GNT#	P1:E5
System Slot (Δ), Logical Slot 1		Peripheral Slot (O), Logical Slot 3	
AD30	P1:A7	IDSEL[1]	P1:B9
REQ1#	P2:C1	REQ#	P1:A6
GNT1#	P2:D1	GNT#	P1:E5
System Slot (Δ), Logical Slot 1		Peripheral Slot (O), Logical Slot 4	
AD29	P1:B7	IDSEL[1]	P1:B9
REQ2#	P2:E1	REQ#	P1:A6
GNT2#	P2:D2	GNT#	P1:E5
System Slot (Δ), Logical Slot 1		Peripheral Slot (O), Logical Slot 5	
AD28	P1:C7	IDSEL[1]	P1:B9
REQ3#	P2:E2	REQ#	P1:A6
GNT3#	P2:C3	GNT#	P1:E5
System Slot (Δ), Logical Slot 1		Peripheral Slot (O), Logical Slot 6	
AD27	P1:E7	IDSEL[1]	P1:B9
REQ4#	P2:D3	REQ#	P1:A6
GNT4#	P2:E3	GNT#	P1:E5
System Slot (Δ), Logical Slot 1		Peripheral Slot (O), Logical Slot 7	
AD26	P1:A8	IDSEL[1]	P1:B9
REQ5#	P2:D15	REQ#	P1:A6
GNT5#	P2:E15	GNT#	P1:E5
System Slot (Δ), Logical Slot 1		Peripheral Slot (O), Logical Slot 8	
AD25	P1:D8	IDSEL[1]	P1:B9
REQ6#	P2:D17	REQ#	P1:A6
GNT6#	P2:E17	GNT#	P1:E5

Figure 5: System to Logical Slot Signal Assignments (Typical)

[1] The IDSEL signal at each slot is connected with minimal trace length at the intended slot.

4.5 CompactPCI Interrupt Implementation

Backplane assignments rotate through logical board slots to provide a unique cPCI interrupt to each board for the first four cPCI connectors (assuming that each board drives only the local INTA# signal). Rotating interrupt assignments allows multiple cPCI peripherals that drive only INTA# in order to utilize a different interrupt on the GEN 6 SBC without the need to share an interrupt with another cPCI interface.

4.5.1 GEN 6 SBC cPCI Interrupt Mapping

The GEN 6 SBC architecture does not implement a device to allow multiple configurations/changes to the INTA#, INTB#, INTC#, INTD# mapping from the backplane to the UT700/UT699E LEON processor.

- The GEN 6 SBC shall implement mapping from the backplane to the UT700/UT699E GPIO[11:14] bus for cPCI signals INTA#- INTD#.

4.6 Front Panel J3 Test Connector Pin Assignments

A 37- pin micro- D type connector provides signal interface connections for the GEN 6 SBC enabling ground development and debug. The J3 pin assignments are outlined in **Figure 6**, "J3 Pin Assignments," and the pin requirements are included in the following paragraphs.

Pin#	Function	Pin#	Function
1	DSU Enable	20	GND
2	DSU Break	21	Ethernet Collision Detect
3	DSU RX	22	Ethernet Transmit CLK
4	GND	23	Ethernet Management Data I/O
5	Ethernet RX Data Valid	24	Ethernet Transmit Error
6	Ethernet Carrier Sense	25	Ethernet Management Data CLK
7	Ethernet Receiver Error	26	Ethernet Transmit Enable
8	J3 Port Power	27	Ethernet Transmit D0
9	3.3 VSC SBC Power	28	Ethernet Transmit D1
10	EDAC Disable	29	Ethernet Transmit D2
11	SBC GPIO[8]	30	Ethernet Transmit D3
12	GND	31	DSU Acknowledge
13	SBC Test Reset	32	SBC DSU Transmit
14	Ethernet Receive D0	33	Supervisor Memory Enable
15	Ethernet Receive D1	34	SBC UART Transmit
16	Ethernet Receive D2	35	SBC GPIO[9]
17	Ethernet Receive D3	36	SBC GPIO[6]
18	Ethernet Receive CLK	37	SBC GPIO[7]
19	SBC UART Receive		

Figure 6: J3 Pin Assignments

4.6.1 J3 Signal Buffering

- The J3 connector is buffered using a cold-spare type of device to isolate the UT700/UT699E from the physical pins on the connector, and to remove signaling from J3 when the debug interface is disconnected from J3.
- When cold-spared, the J3 I/F buffer circuit provides proper inactive levels to the UT700/UT699E side of the interface.
- When in use, the ground system connected to J3 provides a connection from the 3.3 VDC J3 pin [8] to J3 pin [9].
- When not in use, the open connection from J3 pin [8] to J3 pin [9] removes power from the interface buffer circuit. This loss of power from J3 cold-spares all of the signals between the UT700/UT699E and J3.

4.6.2 SBC Debug Support Unit (DSU) I/F

The J3 connector maps to the UT700/UT699E Debug Support Unit (DSU) and associated Enable and Break signals through the buffering circuit.

4.6.3 J3 MRAM Protected Boot Space Write Access

J3 pin [33] provides an external enable allowing the ground system to write boot images to the protected area of the MRAM. Once the ground interface is disconnected from J3, the protected boot space of the MRAM (bottom 16MB starting at address 0) becomes a read-only area.

4.6.4 3.3 VDC and Ground Supply I/F

The J3 connector receives 3.3VDC and Ground supply lines from the GEN 6 SBC, with a current capacity of 0.5 Amps maximum.

4.6.5 Ethernet Interface

The J3 connector maps to the UT700/UT699E Ethernet MAC (MII type) and associated signals through the buffering circuit.

4.6.6 Serial UART Interface

The J3 connector maps to the UT700/UT699E Serial UART and associated signals through the buffering circuit.

4.6.7 SpaceWire Interface

A standard 9-pin micro-D connector provides signal interface connections for the two UT700/UT699E's SpaceWire front panel interface connectors. The P1/P2 signal assignment is shown in **Figure 7**, "P1/P2 Pin Assignments."

Pin#	Function
1	RX Data (+)
2	RX Strobe (+)
3	GND
4	TX Strobe (-)
5	TX Data (-)
6	RX Data (-)
7	RX Strobe (-)
8	TX Strobe (+)
9	TX Data (+)

Figure 7: P1/P2 Pin Assignments

4.6.8 Spare I/O Pin Interface

Eight Spare I/O signals maps to cPCI connector J2 pins [A5, A15, A16, A17, A18, B6, B8, B10], assigned as NC for future use.

4.6.9 cPCI J2 CAN Bus Interface

The J2 cPCI connector maps the two CAN Bus ports and associated signals, to the J2 cPCI connector outlined in **Figure 4**, "cPCI J2 CAN Bus Pin Assignment."

4.6.10 cPCI J2 1553B Bus Interface (UT700 Only)

The J2 cPCI connector maps the two 1553B Bus ports and associated signals, to the J2 cPCI connector outlined in **Figure 4**, "cPCI J2 1553 Bus Pin Assignment."

4.6.11 cPCI J2 SPI Bus Interface (UT700 Only)

The J2 cPCI connector maps the SPI Bus port and associated signals, to the J2 cPCI connector outlined in **Figure 4**, "cPCI J2 SPI Bus Pin Assignment."

4.7 Radiation Considerations

The GEN 6 SBC module is designed to be utilized in a variety of applications including, but not limited to LEO, GEO, and interplanetary missions.

4.7.1 Total Ionizing Dose (TID)

The GEN 6 SBC module is designed with components selected to operate in a Total Ionizing Dose (TID) environment of 100 kRad (worst case LEO).

4.7.2 Single Event Transient & Single Event Upset (SET/SEU)

The GEN 6 SBC module is designed with components selected to operate with SET/SEU, Linear Energy Transfer (LET) of greater than 40 M_eVcm^2 /mg.

4.7.3 Single Event Latch Up (SEL)

The GEN 6 SBC module is designed with components selected to operate with SEL, Linear Energy Transfer (LET) of greater than 75 M_eVcm^2 /mg.

4.7.4 Floating Metal

The GEN 6 SBC module design has no floating metal. The GEN 6 uses 1 oz. copper pour areas on the top and bottom side of the PCB for thermal conduction. All copper islands used for thermal purposes are connected to chassis ground. A dual (redundant) zero- ohm resistor can be used to either isolate the chassis ground from signal ground at the board (IE: not installed) or connect the chassis ground to signal ground at the board (IE: installed); either of these options is available at build time.

4.7.5 EMI/EMC Compliance

The GEN 6 board is designed to minimize radiated EMI. EMI/EMC testing should be conducted at the next- level assembly.

5.0 Mechanical Design

5.1 GEN 6 Requirements

The GEN 6 SBC described by this specification passes all of the examinations, analyses, and tests specified in this document. All Seller supplied documents/drawings use the English unit system for measurements of dimensions and the metric unit system for all other measurements. The Printed Circuit Board (PCB) is designed to IPC Class 3A specifications. Flight units are conformal coated and staked.

5.2 GEN 6 SBC Overview and Definition

The GEN 6 SBC is a Fault Tolerant master single board computer, based on the standard 3U (3.94 inches x 6.3 inches) form factor and an CAES UT700 LEON 3FT processor. The GEN 6 SBC is a slice comprised of a PCB, frame stiffener, and wedgelock channel clamping system.

5.2.1 GEN 6 SBC Physical Form

- The GEN 6 SBC is based on the 3U cPCI form factor.
- The GEN 6 SBC module is designed with high profile parts on the connector (Top) side.
- The GEN 6 SBC module is designed with low profile parts on the wedge lock (Bottom) side.
- The GEN 6 SBC module is a wedge lock securing method using Calmark Series 265 type parts.
- The GEN 6 SBC outline diagram and frame guide dimensions are shown in **Figure 8**.

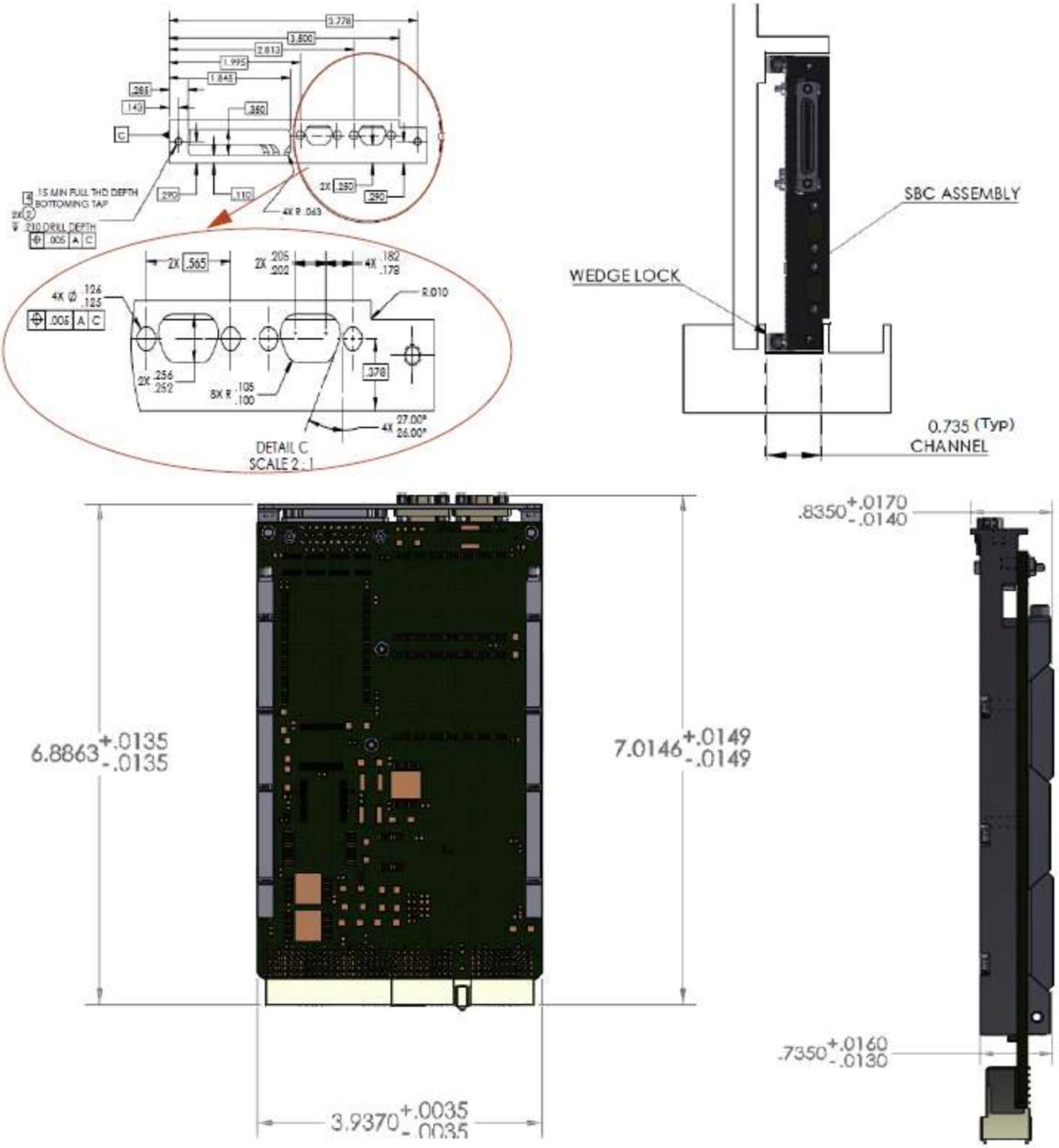


Figure 8: Outline Dimensions and Frame Guide

5.2.2 GEN 6 SBC Environments

- The GEN 6 SBC is designed and constructed to operate within a module rail temperature range -31°C to 62°C.
- The GEN 6 processor module is designed and constructed to operate in a 1x10-5 torr or less environment.

5.2.3 GEN 6 SBC Acceleration

The GEN 6 processor module is designed to withstand a steady state acceleration of 16g's.The steady state analysis incorporates factors of safety of 1.36 (yield) and 1.56 (ultimate). The analysis also incorporates a model uncertainty factor of 1.25.

5.2.4 GEN 6 SBC Vibration

The GEN 6 processor module is designed to be able to operate within specification during and after being subjected to the following Random/Sine vibration environment:

Test	Description
Random Vibration	60 seconds/axis
Proto-flight – spectrum	0.026 g^2/Hz at 20Hz, +6dB/octave 20-50Hz, 0.16 g^2/Hz 50-800Hz, -6 dB/octave 800-2000Hz, 0.026 g^2/Hz at 2000Hz
Proto-flight – overall	14.1 Grms
Acceptance – spectrum	0.013 g^2/Hz at 20Hz, +6dB/octave 20-50Hz, 0.08 g^2/Hz 50-800Hz, -6 dB/octave 800-2000Hz, 0.013 g^2/Hz at 2000Hz
Acceptance – overall	10.0 Grms
Sine Sweep/Burst	11 mm zero-to-peak from 5 Hz to 20 Hz; 20 g from 20 Hz to 100 Hz
Axes	All three

The random vibration design analysis incorporates a safety factor of 2.0 (ultimate) and 1.58 (yield). The analysis may be conducted to either the acceptance test levels with the appropriate safety factors, or at the listed design yield and design ultimate levels that already incorporate these safety factors. In addition to the safety factors, a model uncertainty factor of 1.25 shall be applied to all structural analyses.

- The GEN 6 processor module is designed to be able to withstand the following Shock environment:

Frequency (Hz)	Acceptance (g)	Protoflight	Qualification
10	20	+3dB 1 shock per axis or 1 firing	+6dB 3 shocks per axis or 3 firings
1000	1500		
10000	1500		

- The shock analysis shall be conducted at the qualification levels and shall incorporate a model uncertainty factor of 1.25.
- Additional shock screening/testing for the flight version of the oscillator (reference designator U23) is required to be screened and tested to at least MIL- STD-202, method 213, condition F (1500 g's peak).

5.2.5 Module Mass

- The total mass of the GEN 6 SBC Processor module model is approximately 1.4 lbs.; this total mass is based on EM unit build data.

5.2.6 The GEN 6 SBC Environmental Test Flow (Typical Qualification)

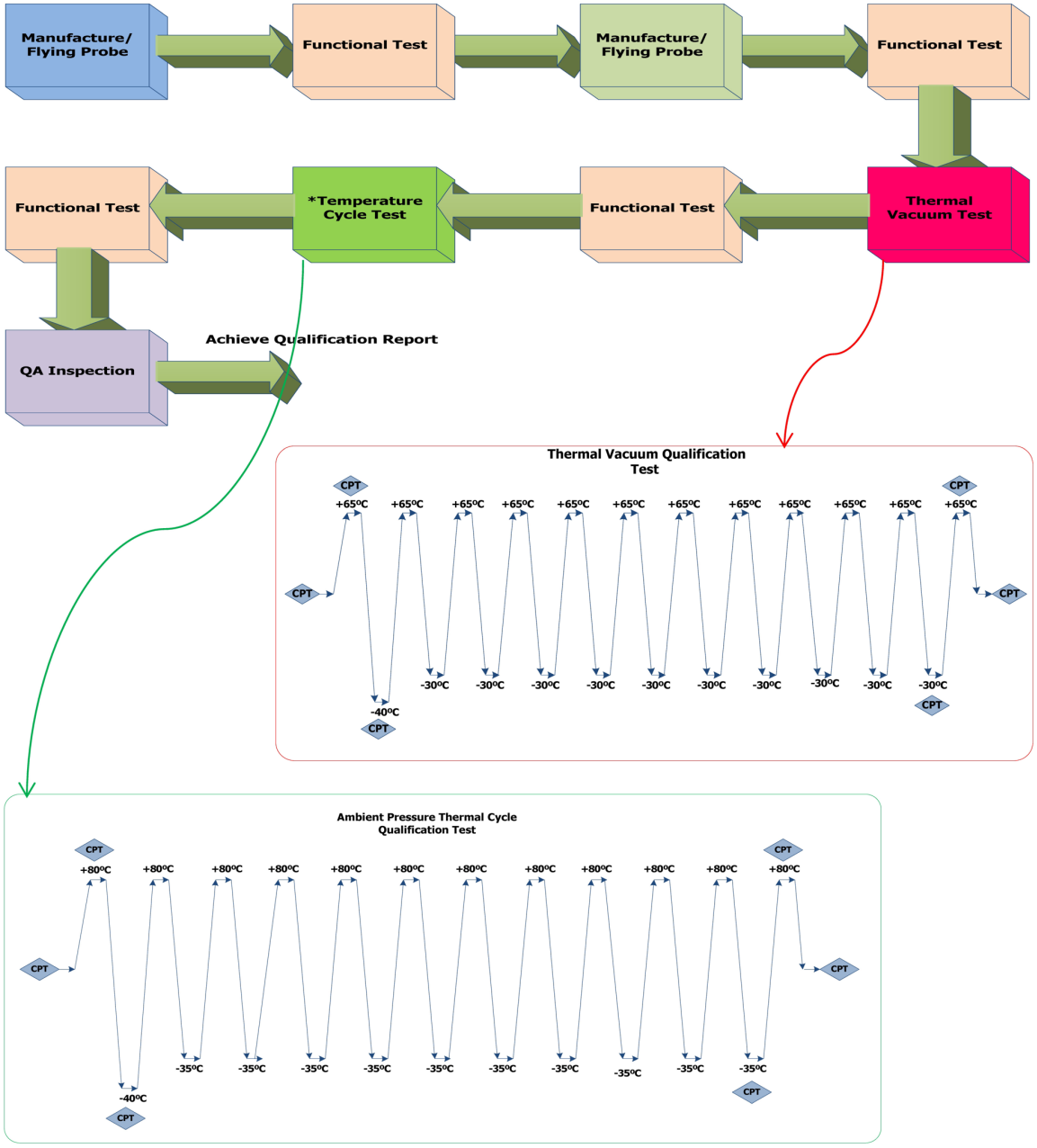


Figure 9: Qualification Test Flow

- Temperature Cycle Limits shown are set to higher/lower extremes allowing TV to be omitted from qualification flows
- Transition < 5°C / min
- Cold start survival at -40 °C
- Comprehensive Performance Test

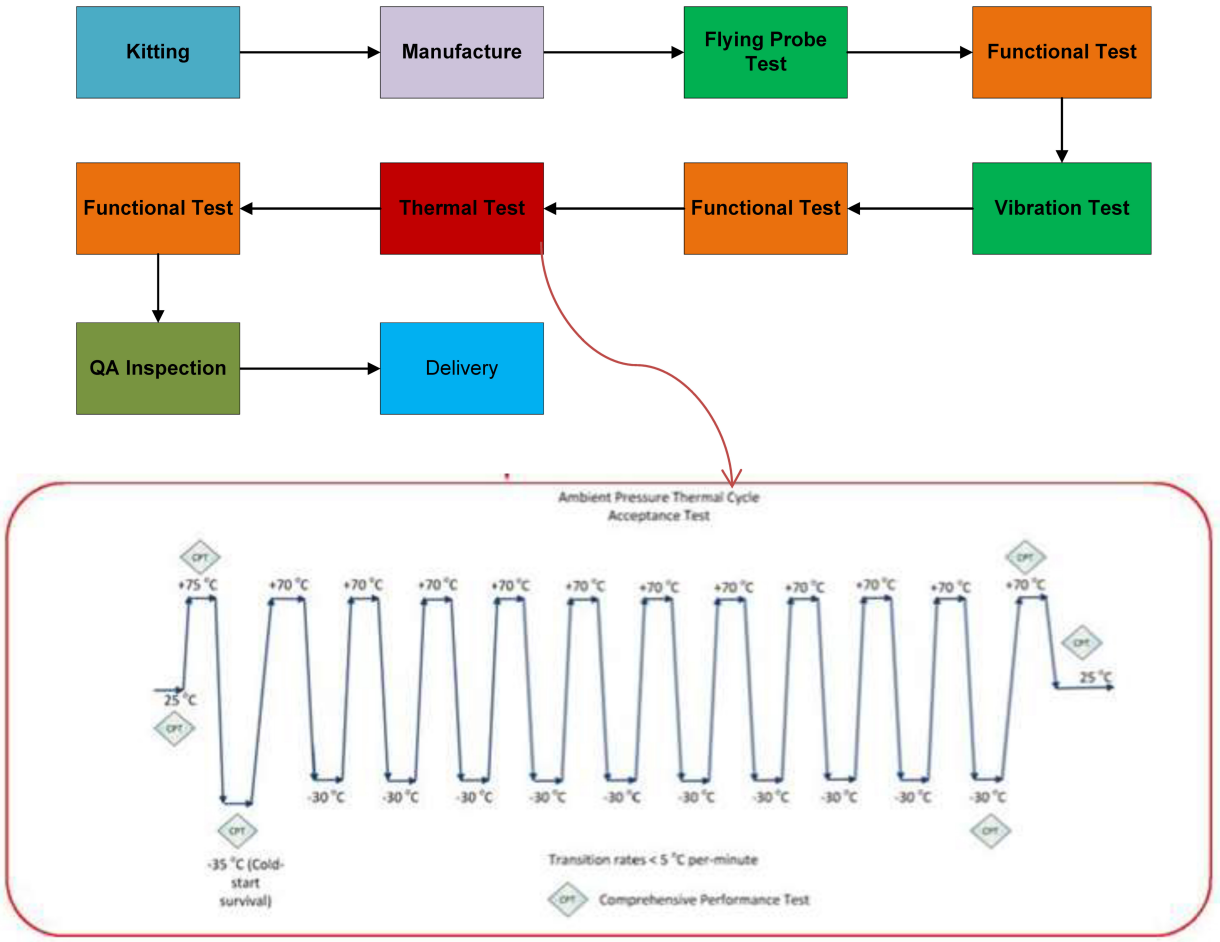


Figure 10: Acceptance Test Flow

Revision History

Date	Revision	Author	Change Description
01/27/2016	0.0.0	---	Initial Revision up to Rev H
06/23/2017	0.0.1	M.T.S	Change Format, Merge different models

Generation 6 SBC Design Specification

DS4350272-X00

Datasheet Definitions

	DEFINITION
Advanced Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet **is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final**.
Preliminary Datasheet	CAES reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.

The following United States (U.S.) Department of Commerce statement shall be applicable if these commodities, technology, or software are exported from the U.S.: These commodities, technology, or software were exported from the United States in accordance with the Export Administration Regulations. Diversion contrary to U.S. law is prohibited.