FRONTGRADE

APPLICATION NOTE

UT7R995/C RadClock™

Banks 3Q, 4Q Output Clock Phase

9/21/2023

Table 1: Cross Reference of Applicable Products

Product Name	Manufacturer Part Number	SMD Number	Device Type	Internal Pic Number
RadClock™ Multi-phase PLL Clock Buffer	UT7R995 UT7R995C	5962-05214	01-04	WD27 WD35

Note:

- * PIC = Product Identification Code

1.0 Overview

This Application Note (AN) documents a known RadClock™ condition when using the internal output dividers for Bank 3 (/K) and Bank 4 (/M), depending on the connection to the phase-locked loop (PLL) feedback (FB) input pin. It has been empirically determined and verified by simulations that using the Bank 3 (/K) and Bank 4 (/M) output dividers with divide ratios other than /1 (i.e. /2 or /4) can result in uncertainty of phasing at PLL power-up/start-up with-respect-to the input reference clock, XTAL1 for these two RadClock™ clock output banks.

2.0 Technical Background

The UT7R995/C RadClock™ 2.5V/3.3V 200 MHz High-Speed Multi-Phase PLL Clock Buffer is a low-voltage, low-power, eight-output, 6-200 MHz clock driver with output clock frequency and phase programmability. The core power supply is 3.3V. The outputs can be operated on either 2.5V or 3.3V power supplies, where output banks 1-4 can be operated using either 2.5V or 3.3V independently of one another. There are several dividers utilized in the RadClock™ IC to provide the user with a high level of flexibility in selecting multiple output clock frequencies.

The Bank 3, 4 output dividers (/K, /M, respectively), phasing issue originates with a potential indeterminate startup state (i.e. logic 0 or logic 1) of these dividers. The internal RadClock™ PLL output is buffered and directly drives the Bank 1, 2 outputs (1Q0,1, 2Q0,1). There are no output dividers at either the Bank 1, 2 outputs, and the Bank 1, 2 outputs always start in phase with the reference clock presented at the XTAL1 input, as set by the PLL control loop.

The measured data shown in section 4.0, below, demonstrates the behaviors of the Bank 3, 4 output clocks for some example configurations, where FB=2Q1, 3Q1, or 4Q1. This is not a complete set of all RadClock™ divider configurations, but rather a selection of representative examples showing both determinate and indeterminate Bank 3, 4 output clock phase, depending on the FB pin connection and settings.

3.0 UT7R995 & UT7R995C RadClock™ Block Diagram

The UT7R995 & UT7R995C RadClock™ Block Diagram is provided here as a reference for the different RadClock™ internal divider configurations. Note output dividers /K, /M for output Banks 3, 4, respectively. Please see Figure A. The RadClock™ Frequency & Skew Calculator tool is available to assist in the configuration of the RadClock™ clock frequency and phase settings. Please contact Frontgrade Applications Engineering Support for calculator tool download information.

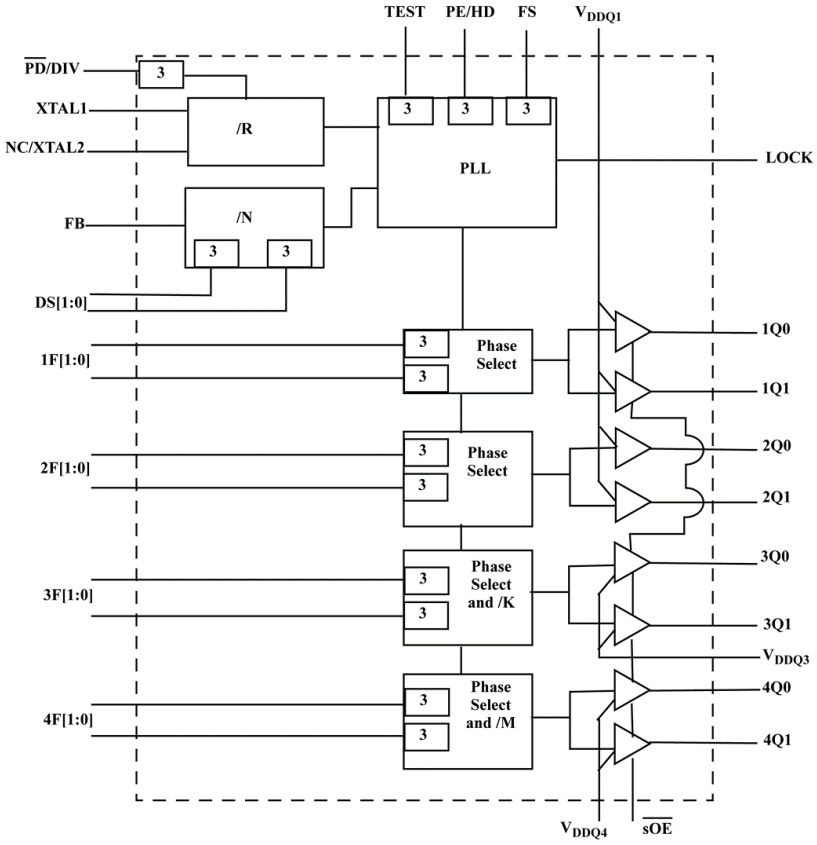

Figure A: UT7R995/C RadClock™ Block Diagram

Note:

- Please refer to the UT7R995/C RadClock™ Datasheet (DS) via the Frontgrade product link provided here:
- https://frontgrade.com/sites/default/files/documents/Datasheet-UT7R995.pdf
- RadClock™ 2.5V/3.3V 200MHz High-Speed Multi-phase PLL Clock
- UT7R995 & UT7R995C
- p.3, Figure 2
- Frontgrade UT7R995/C RadClock™ downloads and Applications Engineering Support links, respectively, are provided here:
- https://frontgrade.com/product/ut7r995#downloads
- https://frontgrade.com/product/ut7r995#support

4.0 Measured Data - RadClock™ Settings + Output Clock Waveforms

This section contains nominal UT7R995 RadClock™ lab measurement results using a limited range of input and output clock frequencies. The RadClock™ Frequency & Skew Calculator tool was employed to assist in configuring the RadClock™. The test equipment setup included: a precision DC power supply, frequency generator, digital oscilloscope (o'scope), and the UT7R995 RadClock™ Evaluation Board. See *Appendix A - Test Equipment Setup* for additional details.

The rising edge of either the input reference clock (XTAL1), or undivided PLL output 1Q0 are used to trigger the o'scope for all measurements. This means that all output waveform timing waveforms are with-respect-to one of these two reference clocks. Note that Bank 1, 2 output clock signals 1Q0,1, 2Q0,1 are always in phase with-respect-to the PLL input reference clock, and that there are no output dividers on these two banks. The reference clock is provided by the external frequency generator clock input, which is connected to the RadClock™ XTAL1 input pin and to the AUX (EXT) o'scope input. This is indicated on the lower right area in each of the o'scope plots. The o'scope input channels 1-4 are connected to RadClock™ Bank 1-4 clock outputs, 1Q0-4Q0, respectively. The RadClock™ feedback (FB) input pin is connected to Bank 2-4 clock outputs 2Q1, 3Q1, or 4Q1 as indicated in the parameter tables for each measurement in this section (4.0), and in summary Table 2 in section 4.1.

RadClock™ Settings								Clock Frequency (MHz)					Results	
TEST #	DS[1:0] (/N)	FS	PE/HD	PD*/ DIV (/R)	3F[1:0] (/K)	4F[1:0] (/M)	FB	XTAL1 (Ref. Clk.)	1Q [1:0]	2Q [1:0]	3Q [1:0]	4Q [1:0]	3Q[1:0] (FLIP?)	4Q[1:0] (FLIP?)
1A	LL (/N=2)	H	M	H (/R=1)	LL (/K=2)	LL (/M=2)	2Q1	60	120	120	60	60	Y	Y

Notes:

1. Trigger = AUX (XTAL1)

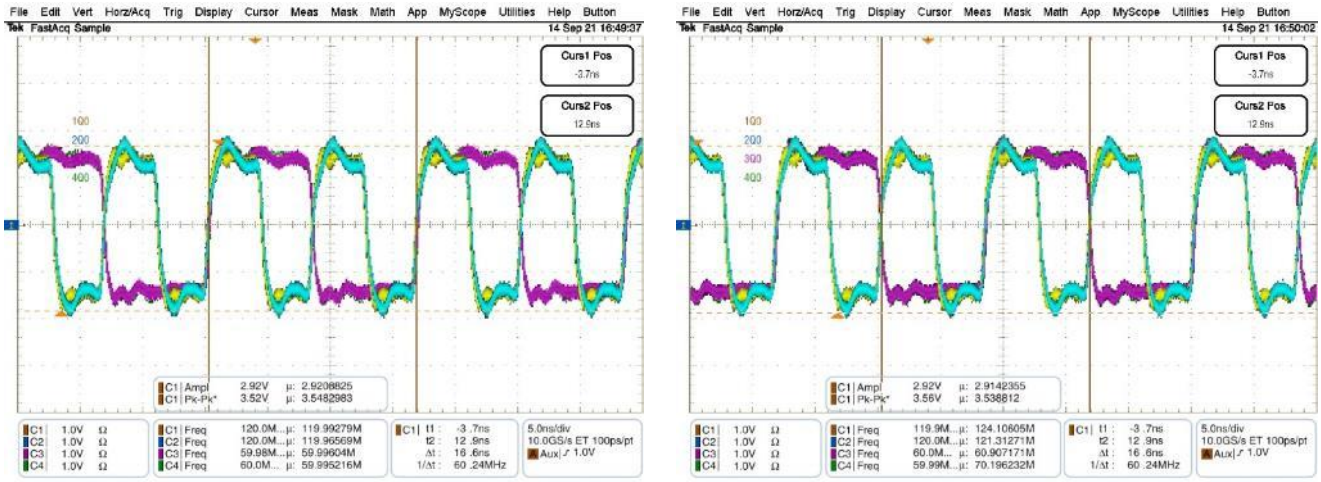

Figure 1a: O'scope waveforms: RadClock™ Output Signals: 1Q0, 2Q0, 3Q0, 4Q0

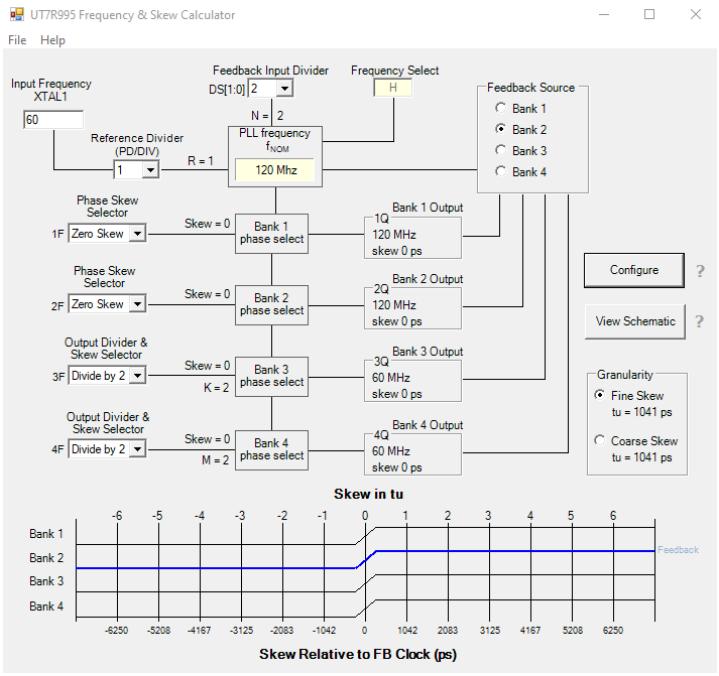

Figure 1b: RadClock™ Frequency & Skew Calculator – Settings

RadClock™ Settings								Clock Frequency (MHz)					Results	
TEST #	DS[1:0] (/N)	FS	PE/HD	PD*/ DIV (/R)	3F[1:0] (/K)	4F[1:0] (/M)	FB	XTAL1 (Ref. Clk.)	1Q [1:0]	2Q [1:0]	3Q [1:0]	4Q [1:0]	3Q[1:0] (FLIP?)	4Q[1:0] (FLIP?)
2A	LL (/N=2)	M	M	H (/R=1)	LL (/K=2)	LL (/M=2)	2Q1	40	80	80	40	40	Y	Y

Notes:

1. Trigger = AUX (XTAL1)

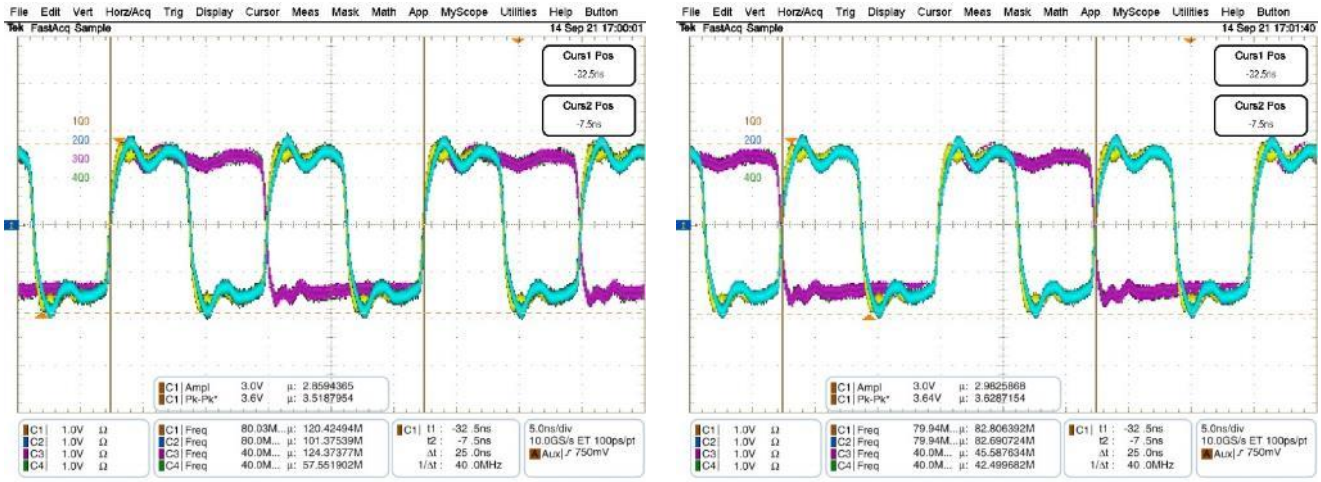

Figure 2a: O'scope waveforms: RadClock™ Output Signals: 1Q0, 2Q0, 3Q0, 4Q0

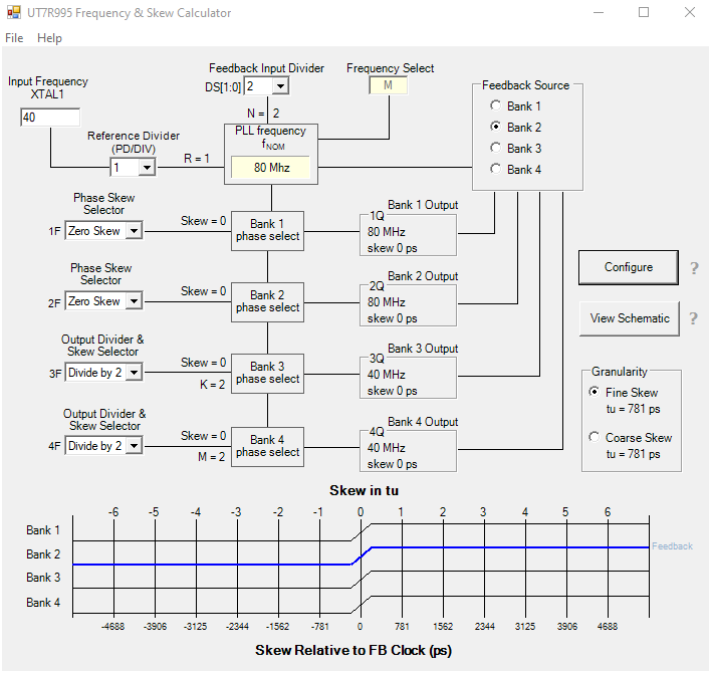

Figure 2b: RadClock™ Frequency & Skew Calculator - Settings

RadClock™ Settings								Clock Frequency (MHz)					Results	
TEST #	DS[1:0] (/N)	FS	PE/HD	PD*/ DIV (/R)	3F[1:0] (/K)	4F[1:0] (/M)	FB	XTAL1 (Ref. Clk.)	1Q [1:0]	2Q [1:0]	3Q [1:0]	4Q [1:0]	3Q[1:0] (FLIP?)	4Q[1:0] (FLIP?)
3A	LL (/N=2)	M	M	H (/R=1)	MM (/K=1)	LL (/M=2)	3Q1	40	80	80	80	40	N	Y

Notes:

1. Trigger = AUX (XTAL1)

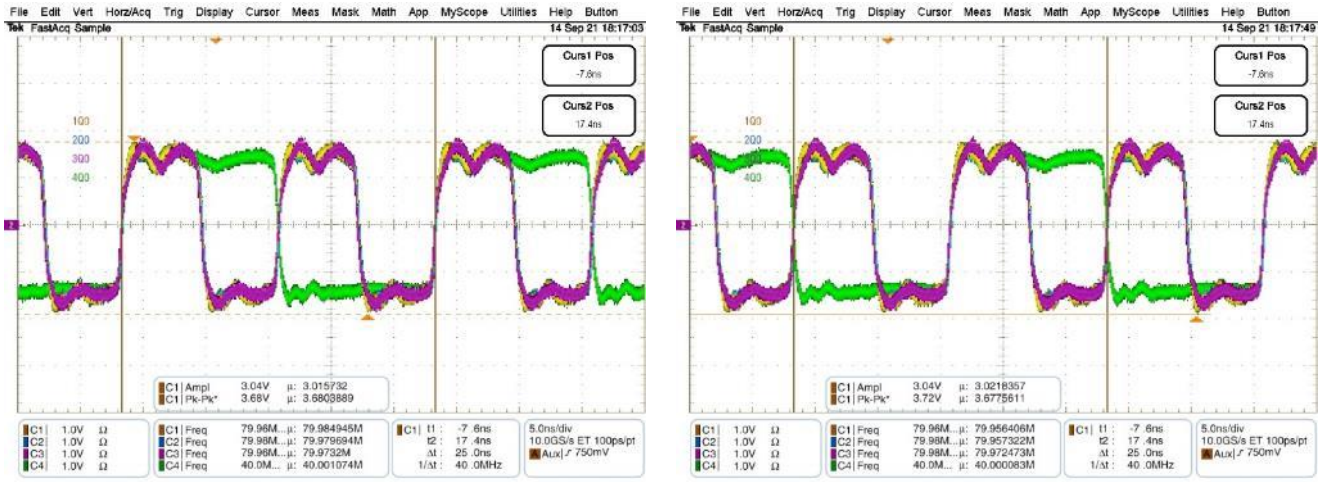

Figure 3a: O'scope waveforms: RadClock™ Output Signals: 1Q0, 2Q0, 3Q0, 4Q0

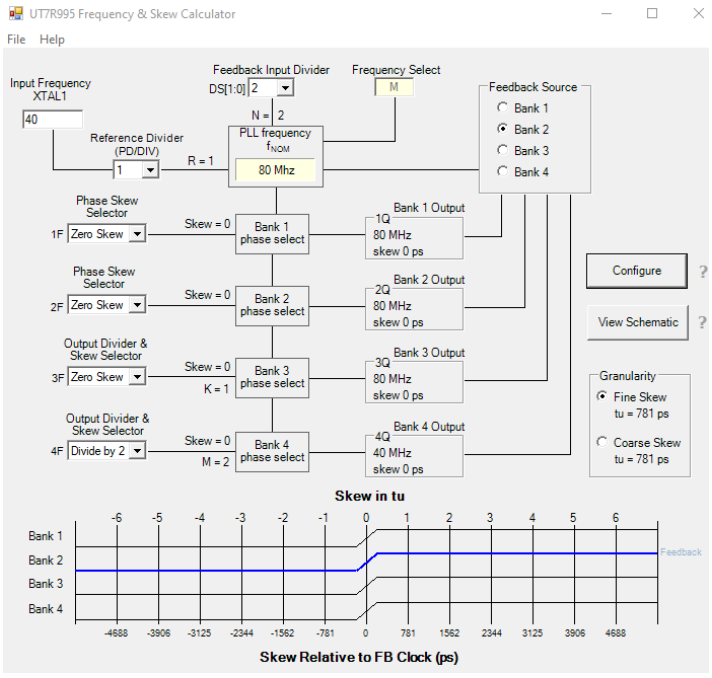

Figure 3b: RadClock™ Frequency & Skew Calculator - Settings

RadClock™ Settings								Clock Frequency (MHz)					Results	
TEST #	DS[1:0] (/N)	FS	PE/HD	PD*/ DIV (/R)	3F[1:0] (/K)	4F[1:0] (/M)	FB	XTAL1 (Ref. Clk.)	1Q [1:0]	2Q [1:0]	3Q [1:0]	4Q [1:0]	3Q[1:0] (FLIP?)	4Q[1:0] (FLIP?)
4A	LL (/N=2)	H	M	H (/R=1)	MM (/K=1)	LL (/M=2)	3Q1	80	160	160	160	80	N	Y

Notes:

1. Trigger = AUX (XTAL1)

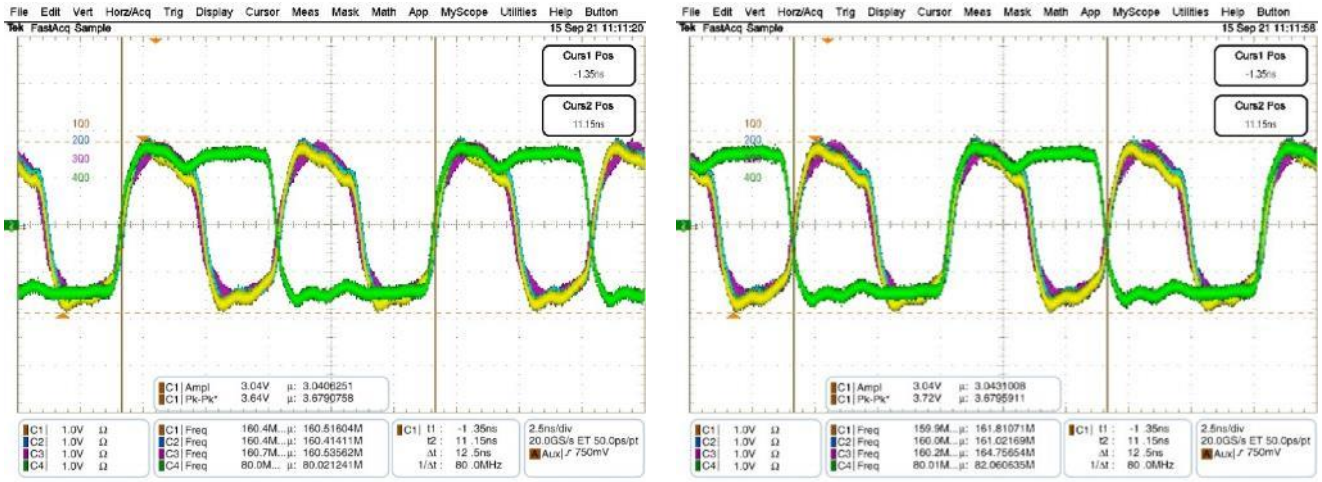

Figure 4a: O'scope waveforms: RadClock™ Output Signals: 1Q0, 2Q0, 3Q0, 4Q0

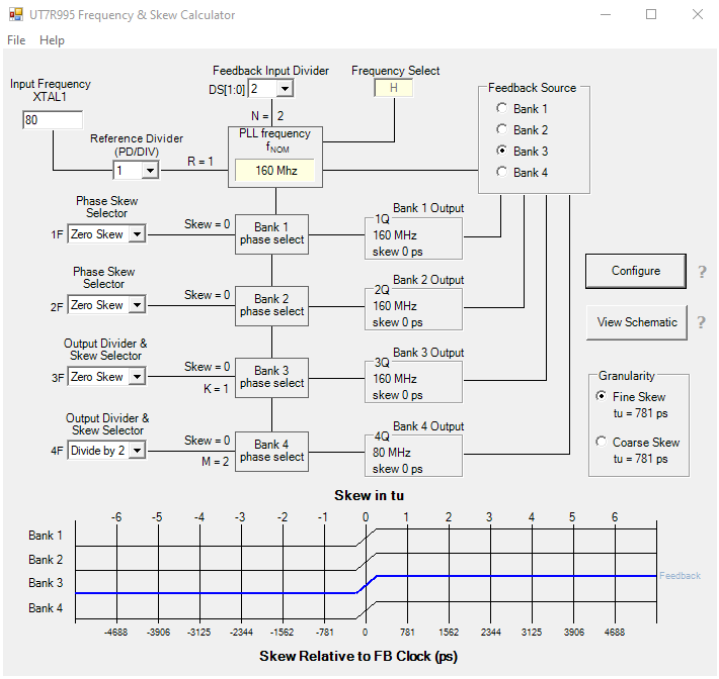

Figure 4b: RadClock™ Frequency & Skew Calculator - Settings

RadClock™ Settings								Clock Frequency (MHz)					Results	
TEST #	DS[1:0] (/N)	FS	PE/HD	PD*/ DIV (/R)	3F[1:0] (/K)	4F[1:0] (/M)	FB	XTAL1 (Ref. Clk.)	1Q [1:0]	2Q [1:0]	3Q [1:0]	4Q [1:0]	3Q[1:0] (FLIP?)	4Q[1:0] (FLIP?)
5A	LL (/N=2)	H	M	H (/R=1)	LL (/K=2)	LL (/M=2)	3Q1	40	160	160	80	80	N	N

Notes:

1. Trigger = AUX (XTAL1)

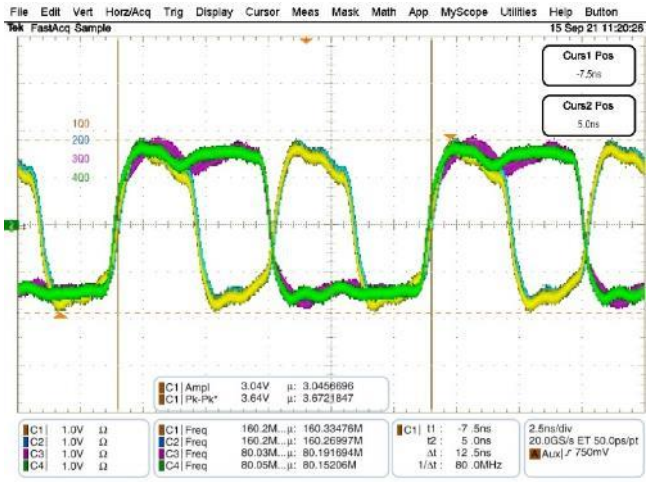

Figure 5a: O'scope waveforms: RadClock™ Output Signals: 1Q0, 2Q0, 3Q0, 4Q0

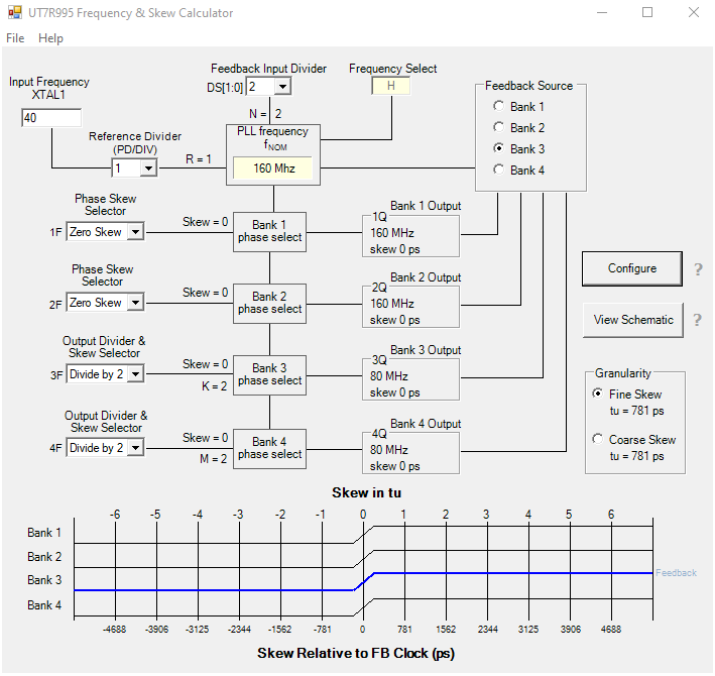

Figure 5b: RadClock™ Frequency & Skew Calculator - Settings

RadClock™ Settings								Clock Frequency (MHz)					Results	
TEST #	DS[1:0] (/N)	FS	PE/HD	PD*/ DIV (/R)	3F[1:0] (/K)	4F[1:0] (/M)	FB	XTAL1 (Ref. Clk.)	1Q [1:0]	2Q [1:0]	3Q [1:0]	4Q [1:0]	3Q[1:0] (FLIP?)	4Q[1:0] (FLIP?)
6A	LL (/N=2)	M	M	H (/R=1)	MM (/K=1)	MM (/M=1)	3Q1	40	80	80	80	80	N	N

Notes:

1. Trigger = AUX (XTAL1)

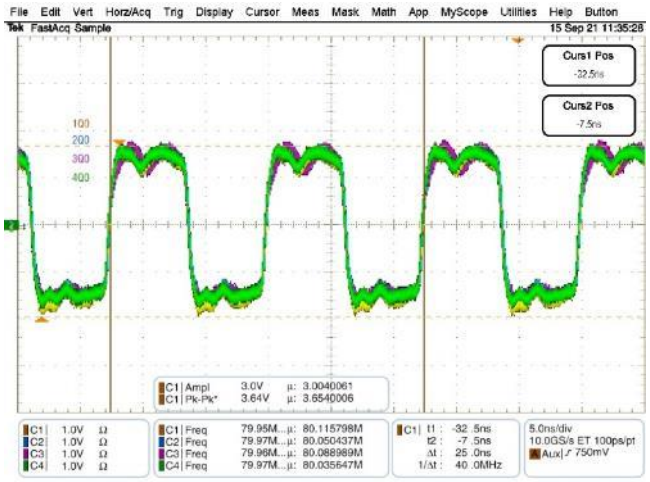

Figure 6a: O'scope waveforms: RadClock™ Output Signals: 1Q0, 2Q0, 3Q0, 4Q0

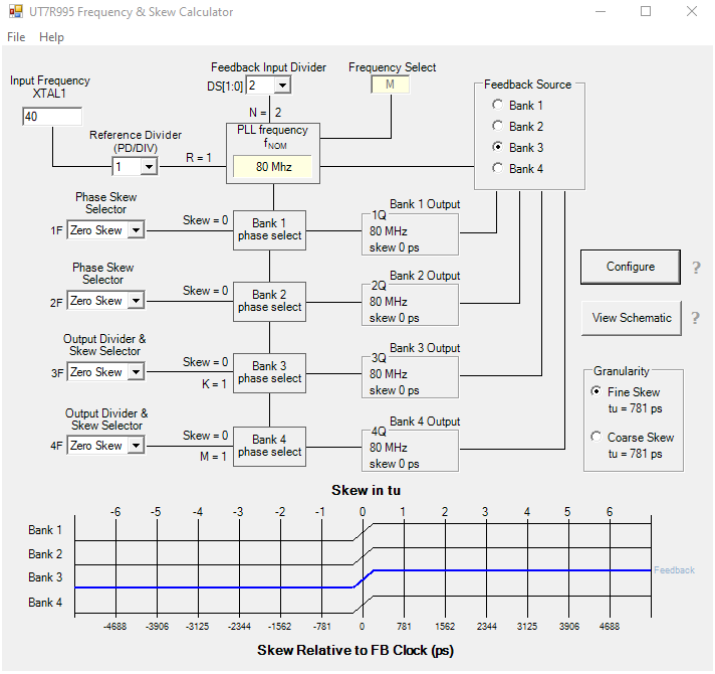

Figure 6b: RadClock™ Frequency & Skew Calculator - Settings

RadClock™ Settings								Clock Frequency (MHz)					Results	
TEST #	DS[1:0] (/N)	FS	PE/HD	PD*/ DIV (/R)	3F[1:0] (/K)	4F[1:0] (/M)	FB	XTAL1 (Ref. Clk.)	1Q [1:0]	2Q [1:0]	3Q [1:0]	4Q [1:0]	3Q[1:0] (FLIP?)	4Q[1:0] (FLIP?)
7A	LL (/N=2)	H	M	H (/R=1)	LL (/K=2)	MM (/M=1)	3Q1	40	160	160	80	160	N	N

Notes:

1. Trigger = AUX (XTAL1)

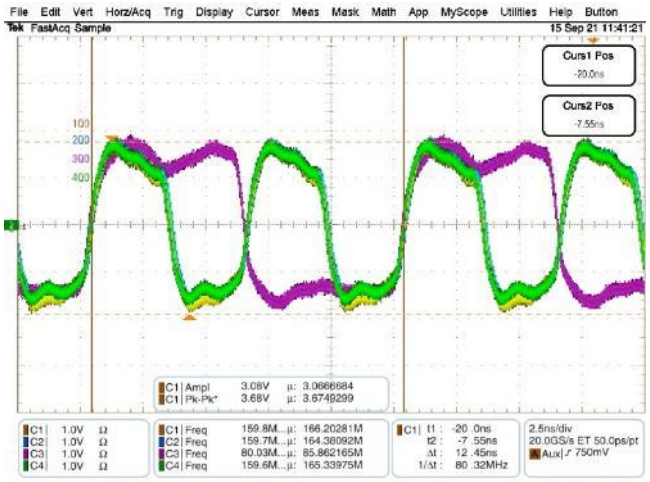

Figure 7a: O'scope waveforms: RadClock™ Output Signals: 1Q0, 2Q0, 3Q0, 4Q0

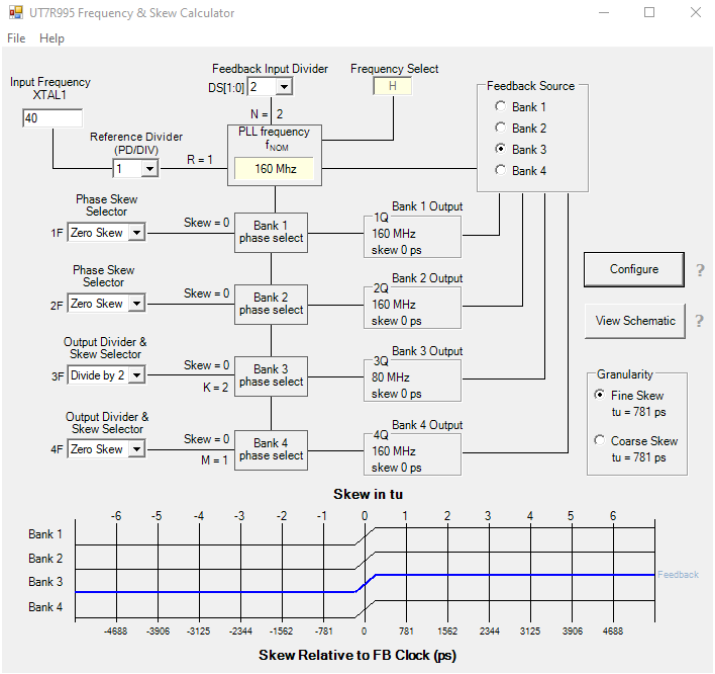

Figure 7b: RadClock™ Frequency & Skew Calculator - Settings

RadClock™ Settings								Clock Frequency (MHz)					Results	
TEST #	DS[1:0] (/N)	FS	PE/HD	PD*/ DIV (/R)	3F[1:0] (/K)	4F[1:0] (/M)	FB	XTAL1 (Ref. Clk.)	1Q [1:0]	2Q [1:0]	3Q [1:0]	4Q [1:0]	3Q[1:0] (FLIP?)	4Q[1:0] (FLIP?)
8A	LL (/N=2)	H	M	H (/R=1)	HH (/K=4)	LL (/M=2)	3Q1	20	160	160	40	80	N	N

Notes:

1. Trigger = AUX (XTAL1)

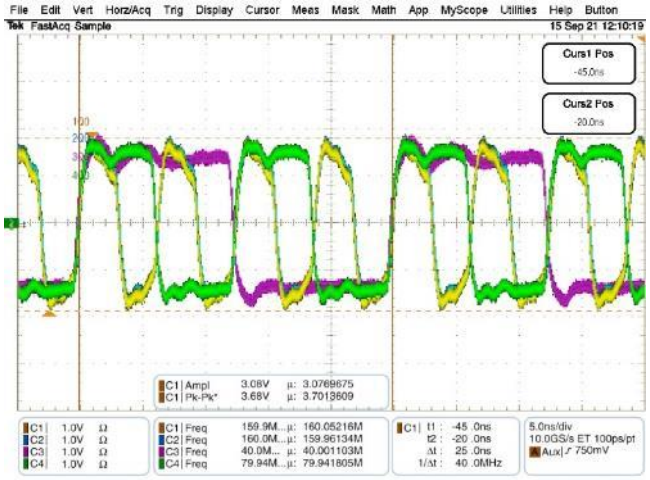

Figure 8a: O'scope waveforms: RadClock™ Output Signals: 1Q0, 2Q0, 3Q0, 4Q0

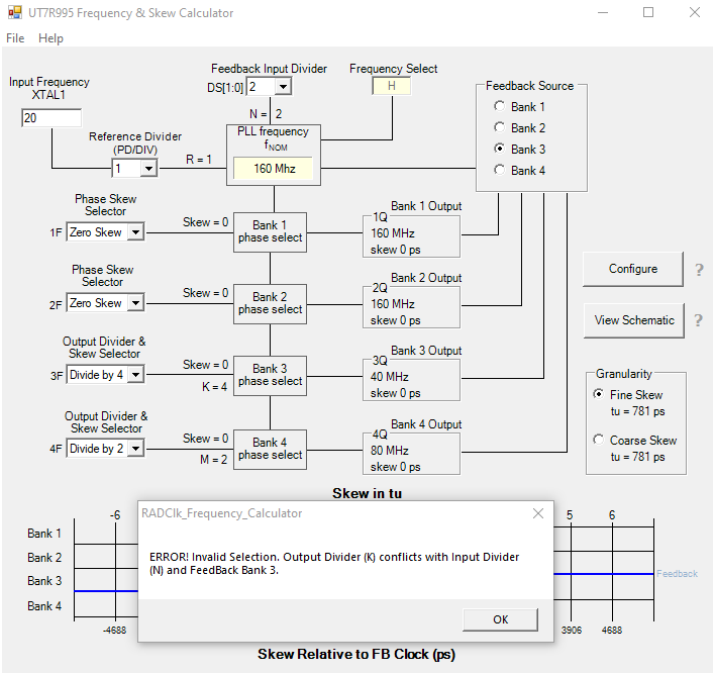

Figure 8b: RadClock™ Frequency & Skew Calculator - Settings

Note: This /K 3Q[1:0] divider configuration is not allowed, per the RadClock calculator tool.

RadClock™ Settings								Clock Frequency (MHz)					Results	
TEST #	DS[1:0] (/N)	FS	PE/HD	PD*/ DIV (/R)	3F[1:0] (/K)	4F[1:0] (/M)	FB	XTAL1 (Ref. Clk.)	1Q [1:0]	2Q [1:0]	3Q [1:0]	4Q [1:0]	3Q[1:0] (FLIP?)	4Q[1:0] (FLIP?)
9A	MM (/N=1)	M	M	M (/R=2)	HH (/K=4)	LL (/M=2)	3Q1	30	60	60	15	30	Y	N

Notes:

1. Trigger = AUX (XTAL1) divided by 2 (15 MHz)

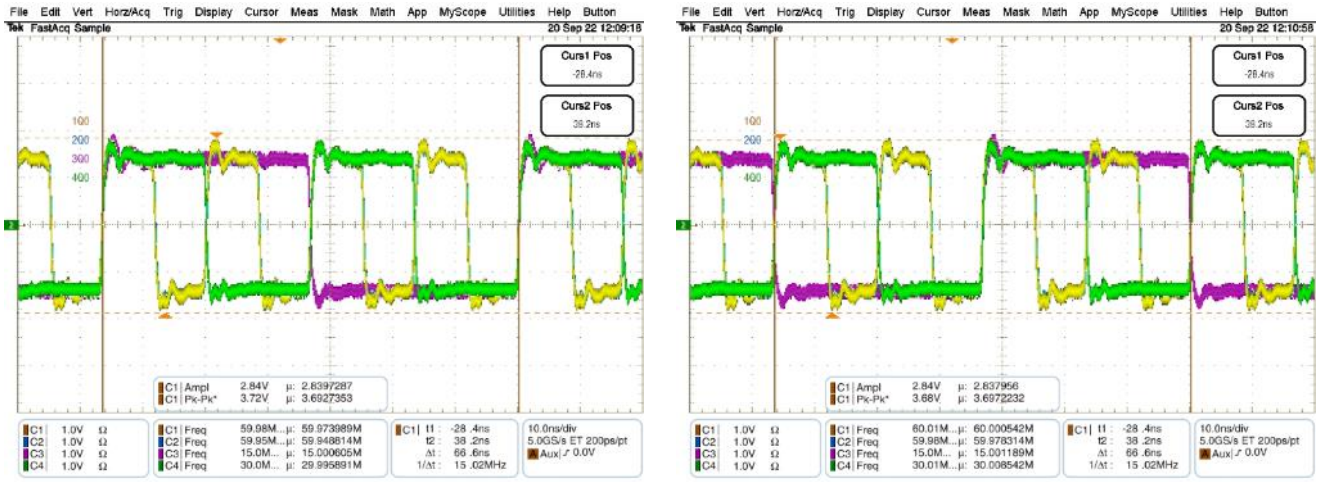

Figure 9a: O'scope waveforms: RadClock™ Output Signals: 1Q0, 2Q0, 3Q0, 4Q0

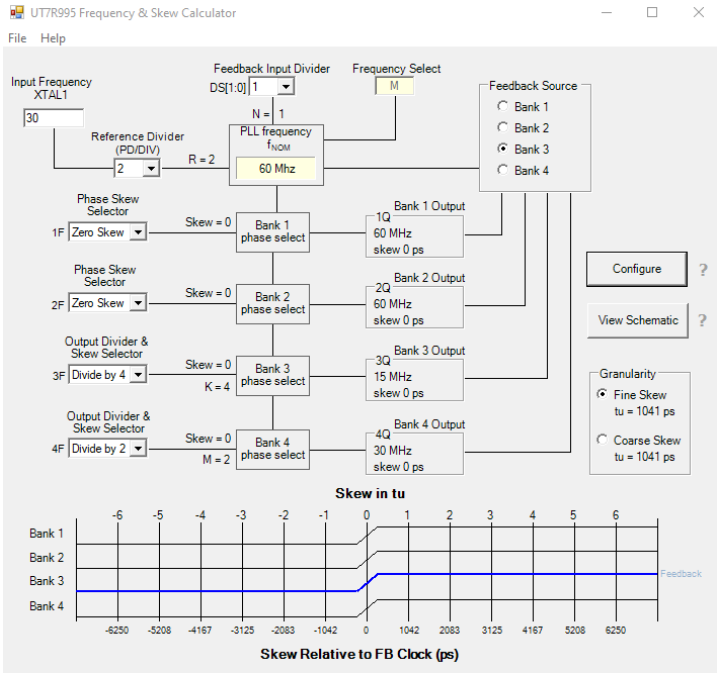

Figure 9b: RadClock™ Frequency & Skew Calculator - Settings

RadClock™ Settings								Clock Frequency (MHz)					Results	
TEST #	DS[1:0] (/N)	FS	PE/HD	PD*/ DIV (/R)	3F[1:0] (/K)	4F[1:0] (/M)	FB	XTAL1 (Ref. Clk.)	1Q [1:0]	2Q [1:0]	3Q [1:0]	4Q [1:0]	3Q[1:0] (FLIP?)	4Q[1:0] (FLIP?)
10A	MM (/N=1)	M	M	H (/R=1)	LL (/K=2)	MM (/M=1)	3Q1	40	80	80	40	80	N	N

Notes:
1. Trigger = AUX (XTAL1)

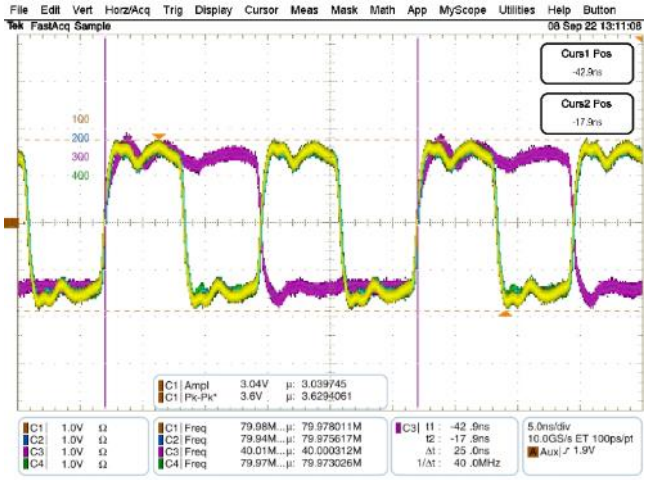

Figure 10a: O'scope waveforms: RadClock™ Output Signals: 1Q0, 2Q0, 3Q0, 4Q0

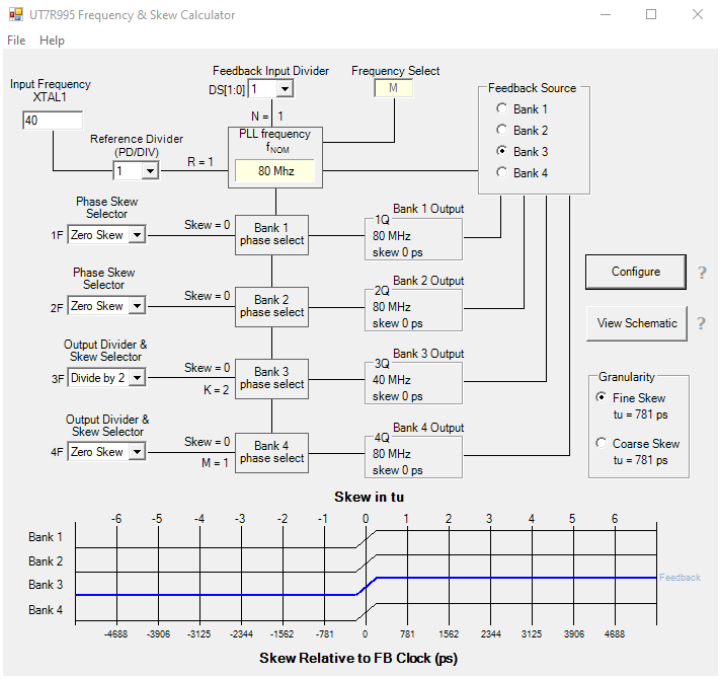

Figure 10b: RadClock™ Frequency & Skew Calculator - Settings

RadClock™ Settings								Clock Frequency (MHz)					Results	
TEST #	DS[1:0] (/N)	FS	PE/HD	PD*/ DIV (/R)	3F[1:0] (/K)	4F[1:0] (/M)	FB	XTAL1 (Ref. Clk.)	1Q [1:0]	2Q [1:0]	3Q [1:0]	4Q [1:0]	3Q[1:0] (FLIP?)	4Q[1:0] (FLIP?)
11A	MM (/N=1)	L	M	M (/R=2)	LL (/K=2)	MM (/M=1)	3Q1	40	40	40	20	40	Y	N

Notes:

1. Trigger = AUX (XTAL1) divided by 2 (20 MHz)

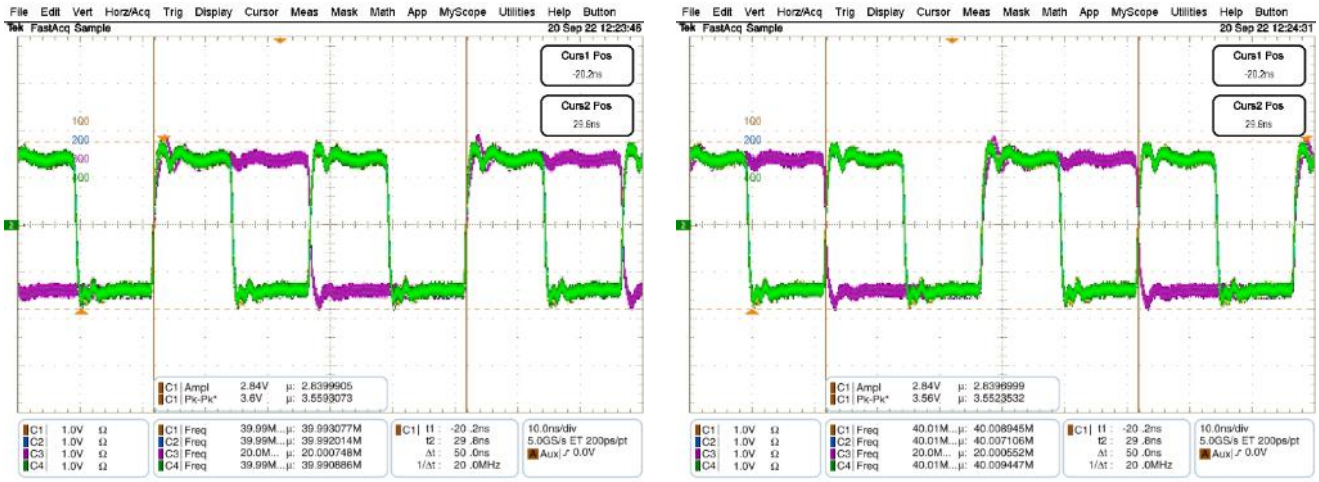

Figure 11a: O'scope waveforms: RadClock™ Output Signals: 1Q0, 2Q0, 3Q0, 4Q0

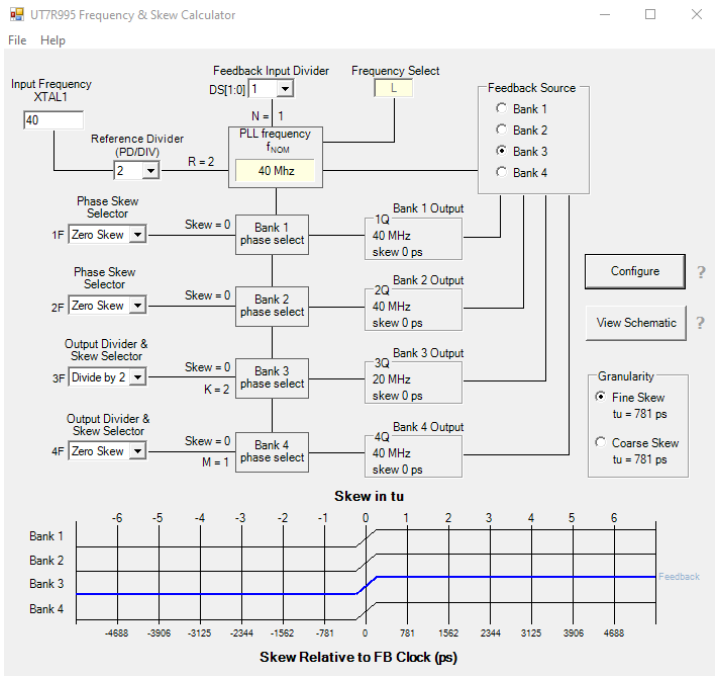

Figure 11b: RadClock™ Frequency & Skew Calculator - Settings

RadClock™ Settings								Clock Frequency (MHz)					Results	
TEST #	DS[1:0] (/N)	FS	PE/HD	PD*/ DIV (/R)	3F[1:0] (/K)	4F[1:0] (/M)	FB	XTAL1 (Ref. Clk.)	1Q [1:0]	2Q [1:0]	3Q [1:0]	4Q [1:0]	3Q[1:0] (FLIP?)	4Q[1:0] (FLIP?)
12A	MM (/N=1)	H	M	H (/R=1)	HH (/K=4)	LL (/M=2)	3Q1	40	160	160	40	80	N	N

Notes:
1. Trigger = AUX (XTAL1)

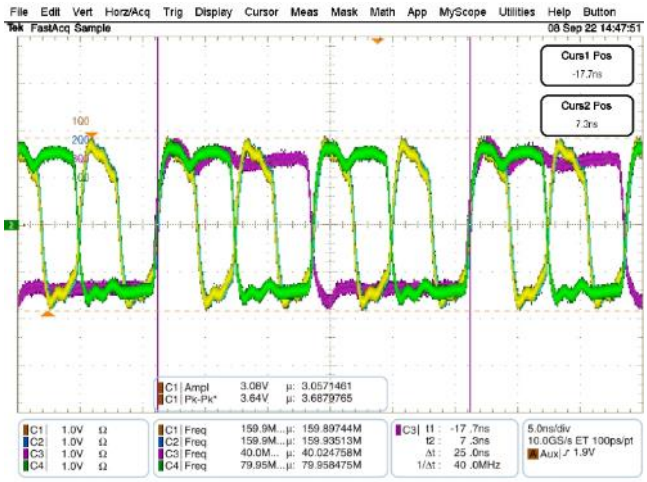

Figure 12a: O'scope waveforms: RadClock™ Output Signals: 1Q0, 2Q0, 3Q0, 4Q0

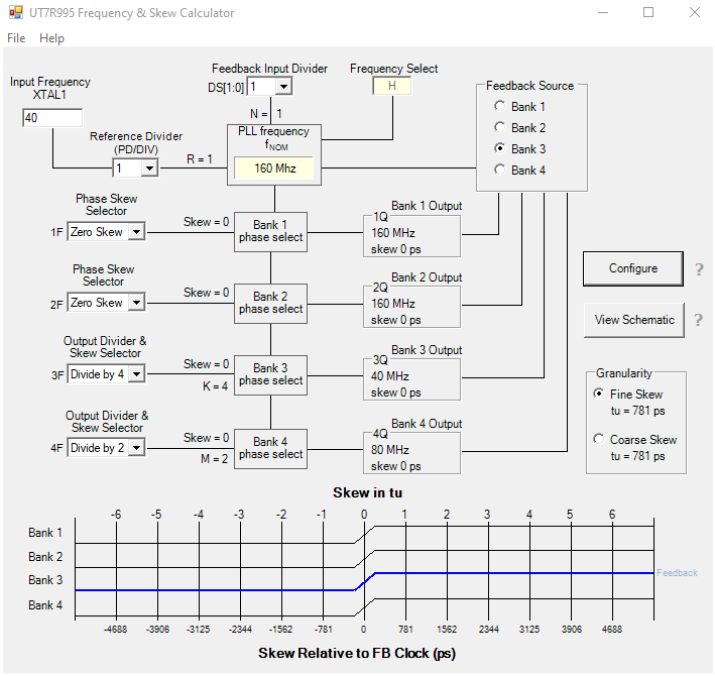

Figure 12b: RadClock™ Frequency & Skew Calculator - Settings

RadClock™ Settings								Clock Frequency (MHz)					Results	
TEST #	DS[1:0] (/N)	FS	PE/HD	PD*/ DIV (/R)	3F[1:0] (/K)	4F[1:0] (/M)	FB	XTAL1 (Ref. Clk.)	1Q [1:0]	2Q [1:0]	3Q [1:0]	4Q [1:0]	3Q[1:0] (FLIP?)	4Q[1:0] (FLIP?)
13A	MM (/N=1)	M	M	M (/R=2)	HH (/K=4)	LL (/M=2)	3Q1	40	80	80	20	40	Y	N

Notes:

1. Trigger = AUX (XTAL1) divided by 2 (20 MHz)

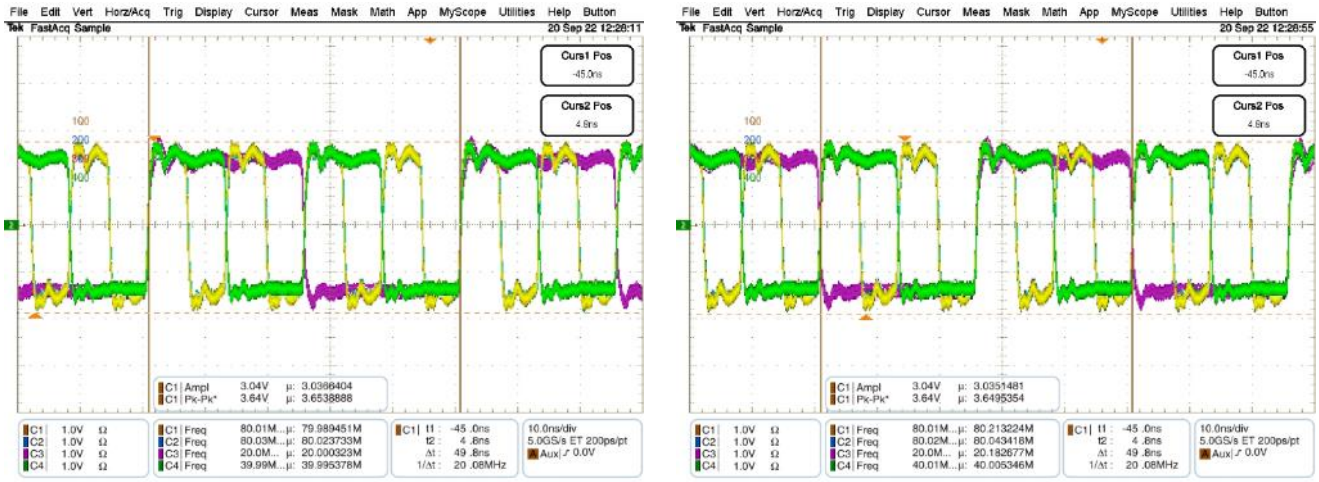

Figure 13a: O'scope waveforms: RadClock™ Output Signals: 1Q0, 2Q0, 3Q0, 4Q0

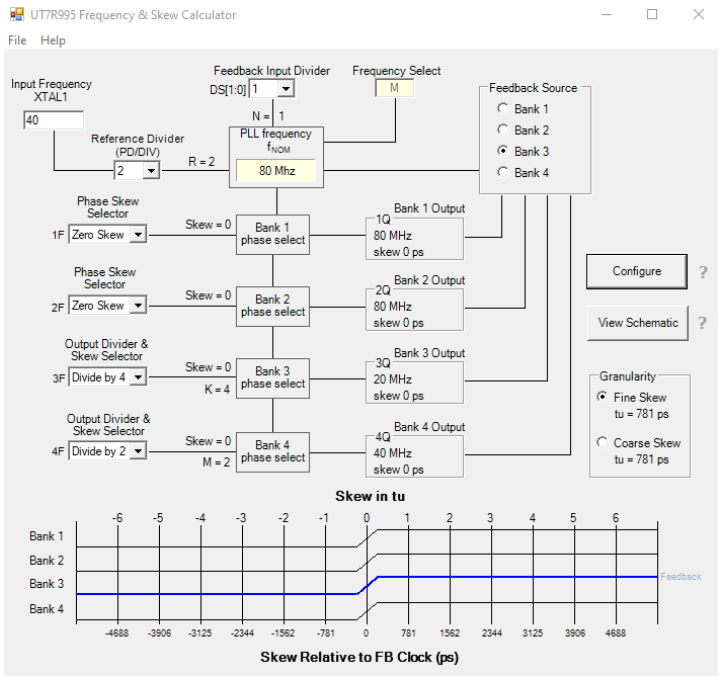

Figure 13b: RadClock™ Frequency & Skew Calculator - Settings

RadClock™ Settings								Clock Frequency (MHz)					Results	
TEST #	DS[1:0] (/N)	FS	PE/HD	PD*/ DIV (/R)	3F[1:0] (/K)	4F[1:0] (/M)	FB	XTAL1 (Ref. Clk.)	1Q [1:0]	2Q [1:0]	3Q [1:0]	4Q [1:0]	3Q[1:0] (FLIP?)	4Q[1:0] (FLIP?)
14A	LL (/N=2)	H	M	M (/R=2)	HH (/K=4)	LL (/M=2)	3Q1	40	160	160	40	80	N	N

Notes:

1. Trigger = AUX (XTAL1)

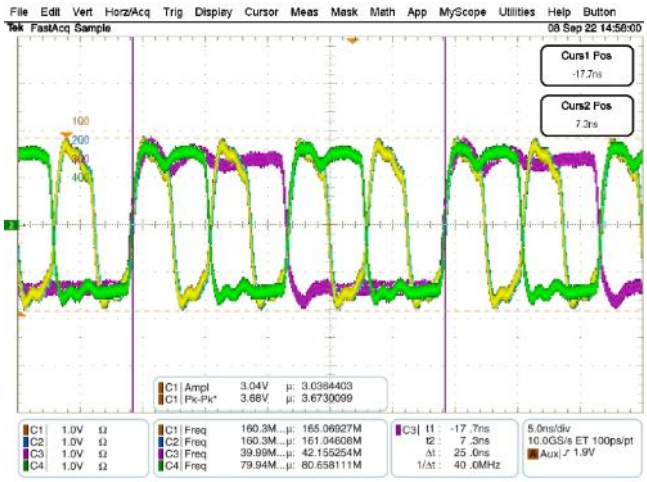

Figure 14a: O'scope waveforms: RadClock™ Output Signals: 1Q0, 2Q0, 3Q0, 4Q0

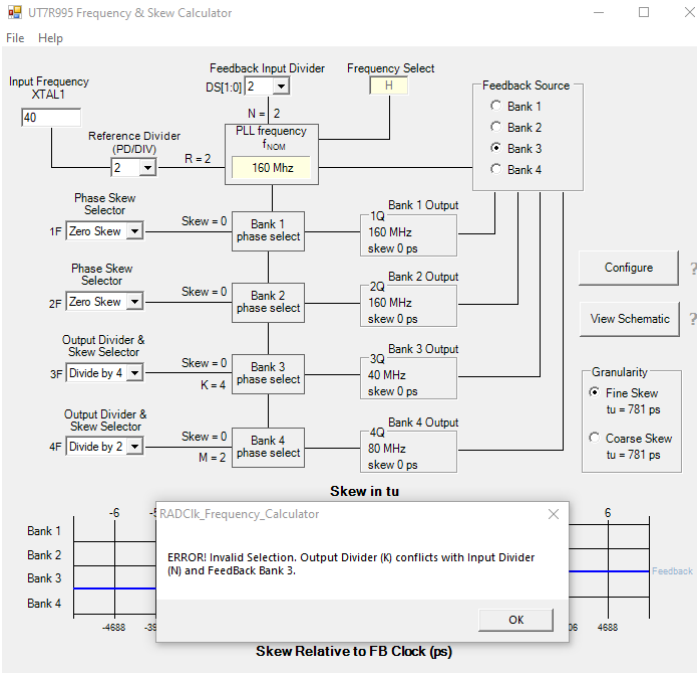

Figure 14b: RadClock™ Frequency & Skew Calculator - Settings

Note: This /K 3Q[1:0] divider configuration is not allowed, per the RadClock™ calculator tool

RadClock™ Settings								Clock Frequency (MHz)					Results	
TEST #	DS[1:0] (/N)	FS	PE/HD	PD*/ DIV (/R)	3F[1:0] (/K)	4F[1:0] (/M)	FB	XTAL1 (Ref. Clk.)	1Q [1:0]	2Q [1:0]	3Q [1:0]	4Q [1:0]	3Q[1:0] (FLIP?)	4Q[1:0] (FLIP?)
15C	LL (/N=2)	M	M	H (/R=1)	MM (/K=1)	LL (/M=2)	3Q1	40	80	80	80	40	N	Y

Notes:

1. Trigger = AUX (XTAL1)

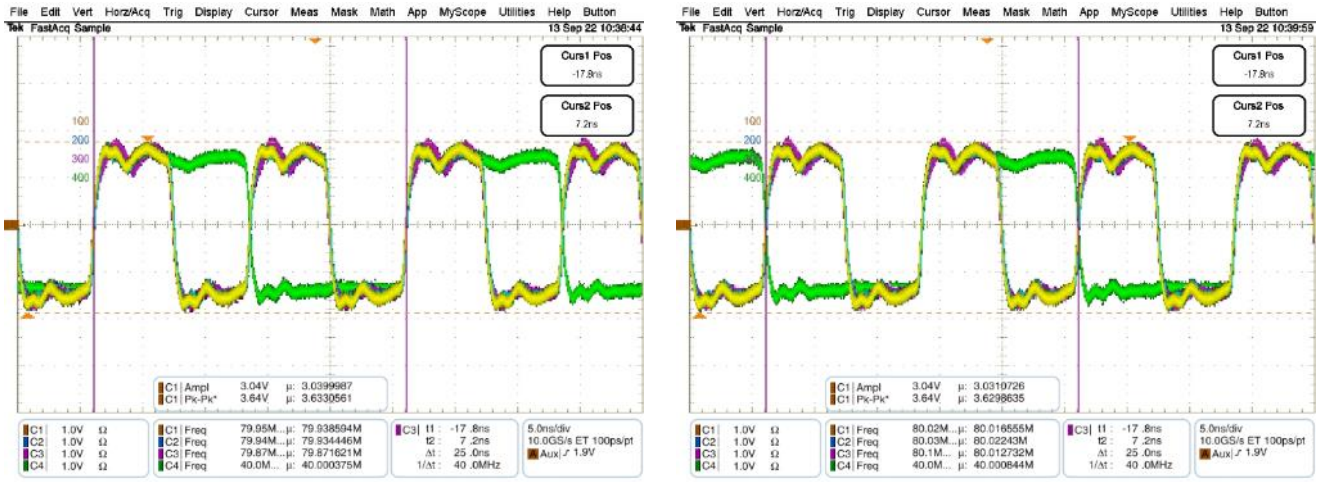

Figure 15a: O'scope waveforms: RadClock™ Output Signals: 1Q0, 2Q0, 3Q0, 4Q0

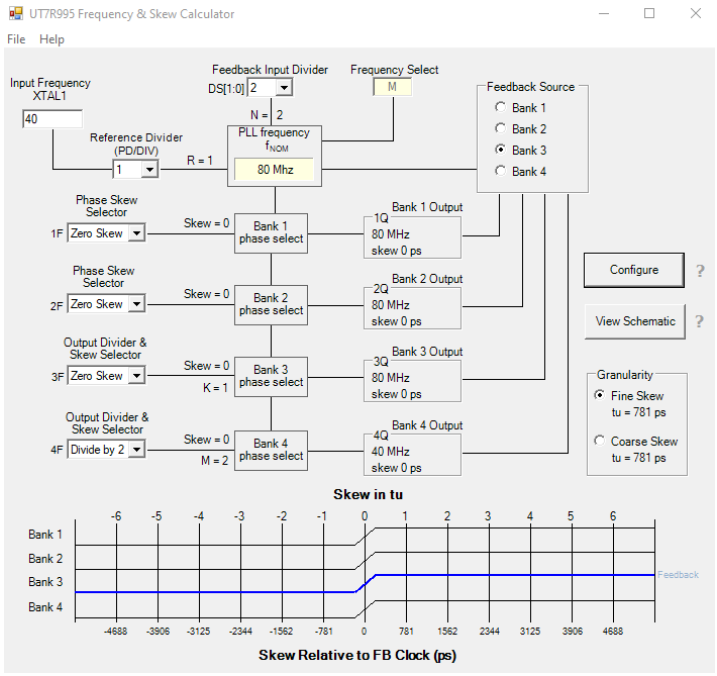

Figure 15b: RadClock™ Frequency & Skew Calculator - Settings

RadClock™ Settings								Clock Frequency (MHz)					Results	
TEST #	DS[1:0] (/N)	FS	PE/HD	PD*/ DIV (/R)	3F[1:0] (/K)	4F[1:0] (/M)	FB	XTAL1 (Ref. Clk.)	1Q [1:0]	2Q [1:0]	3Q [1:0]	4Q [1:0]	3Q[1:0] (FLIP?)	4Q[1:0] (FLIP?)
16C	LL (/N=1)	M	M	H (/R=1)	MM (/K=1)	LL (/M=2)	3Q1	40	40	40	40	20	N	Y

Notes:

1. Trigger = AUX (XTAL1) divided by 2 (20 MHz)

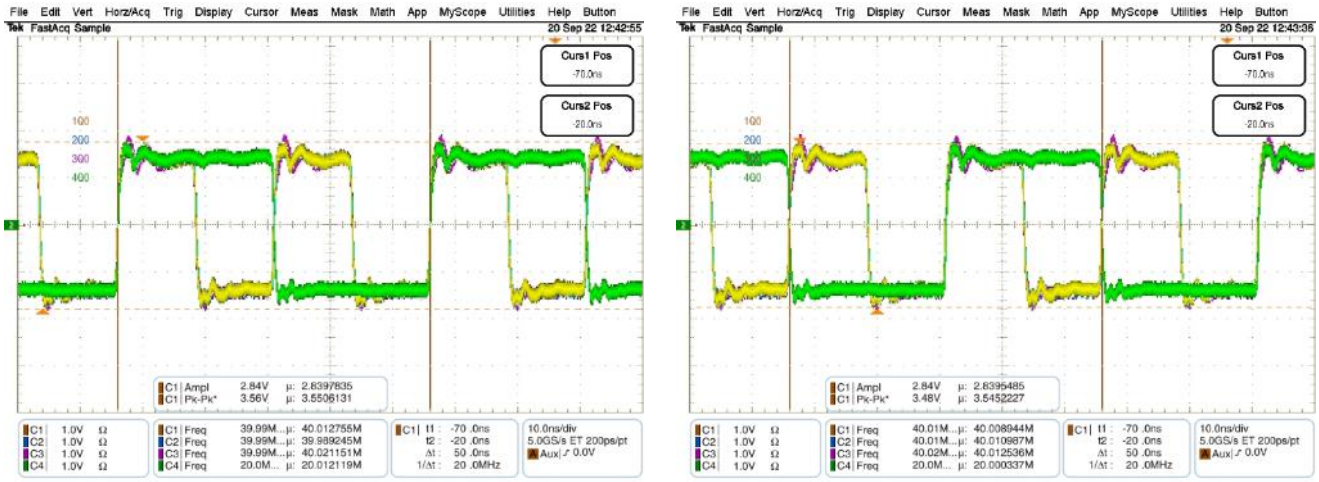

Figure 16a: O'scope waveforms: RadClock™ Output Signals: 1Q0, 2Q0, 3Q0, 4Q0

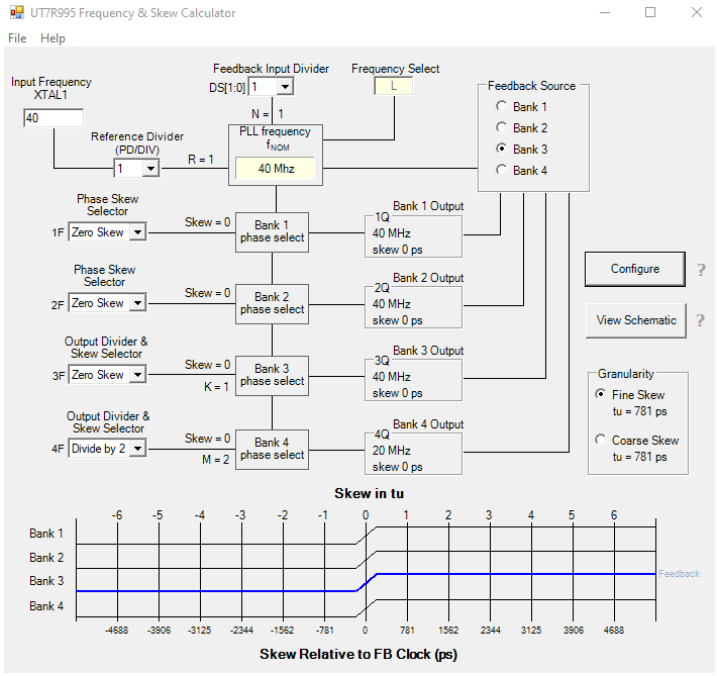

Figure 16b: RadClock™ Frequency & Skew Calculator - Settings

RadClock™ Settings								Clock Frequency (MHz)					Results	
TEST #	DS[1:0] (/N)	FS	PE/HD	PD*/ DIV (/R)	3F[1:0] (/K)	4F[1:0] (/M)	FB	XTAL1 (Ref. Clk.)	1Q [1:0]	2Q [1:0]	3Q [1:0]	4Q [1:0]	3Q[1:0] (FLIP?)	4Q[1:0] (FLIP?)
17C	LH (/N=4)	H	M	H (/R=1)	MM (/K=1)	LL (/M=2)	3Q1	40	160	160	160	80	N	Y

Notes:

1. Trigger = AUX (XTAL1)

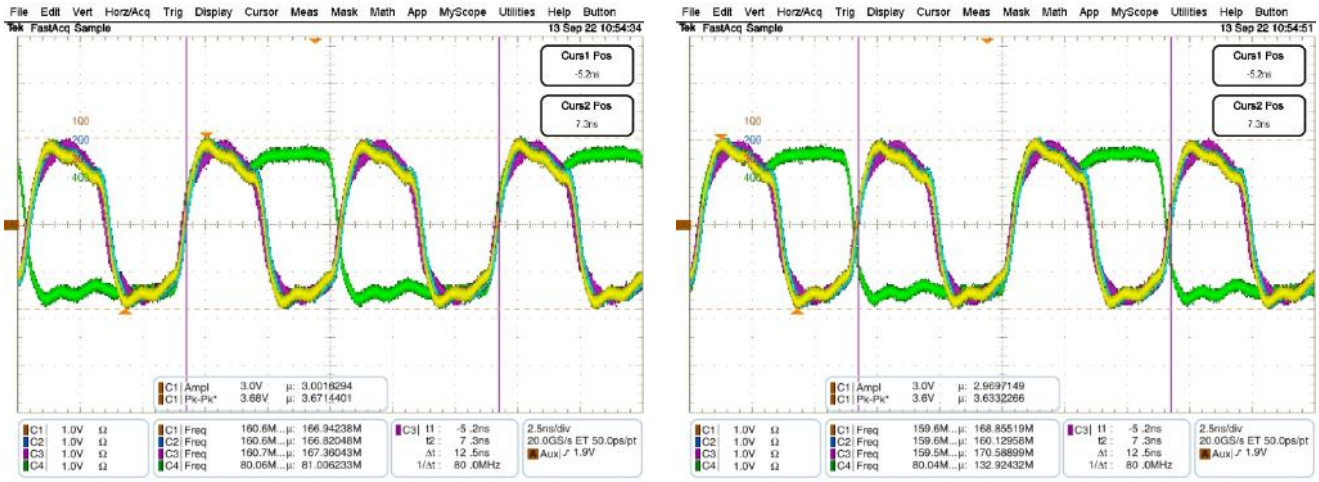

Figure 17a: O'scope waveforms: RadClock™ Output Signals: 1Q0, 2Q0, 3Q0, 4Q0

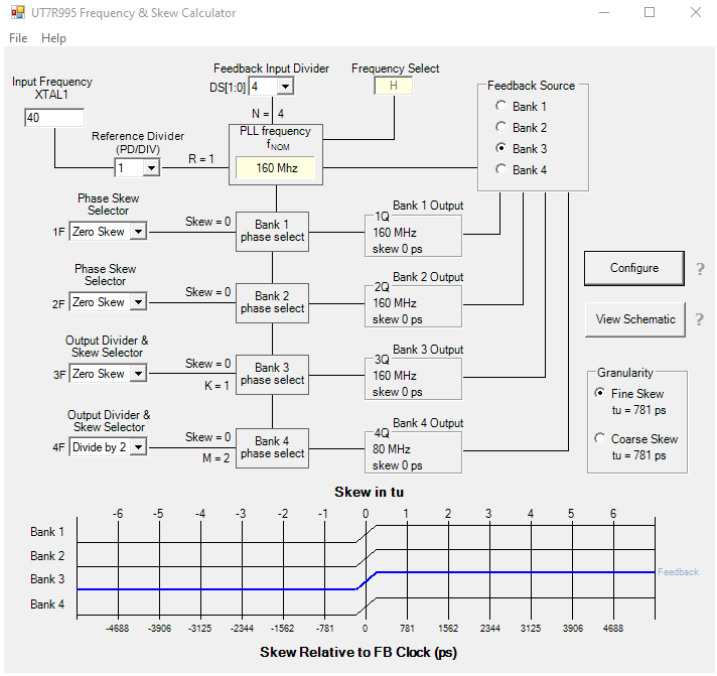

Figure 17b: RadClock™ Frequency & Skew Calculator - Settings

RadClock™ Settings								Clock Frequency (MHz)					Results	
TEST #	DS[1:0] (/N)	FS	PE/HD	PD*/ DIV (/R)	3F[1:0] (/K)	4F[1:0] (/M)	FB	XTAL1 (Ref. Clk.)	1Q [1:0]	2Q [1:0]	3Q [1:0]	4Q [1:0]	3Q[1:0] (FLIP?)	4Q[1:0] (FLIP?)
18B	LL (/N=2)	M	M	H (/R=1)	LL (/K=2)	MM (/M=1)	4Q1	40	80	80	40	80	Y	N

Notes:

1. Trigger = AUX (XTAL1)

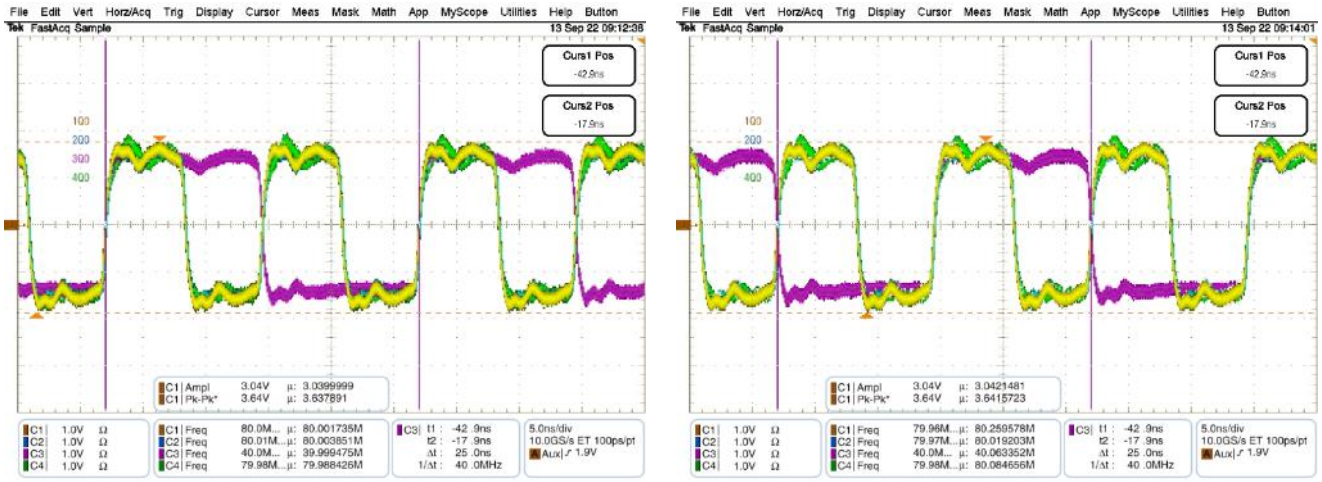

Figure 18a: O'scope waveforms: RadClock™ Output Signals: 1Q0, 2Q0, 3Q0, 4Q0

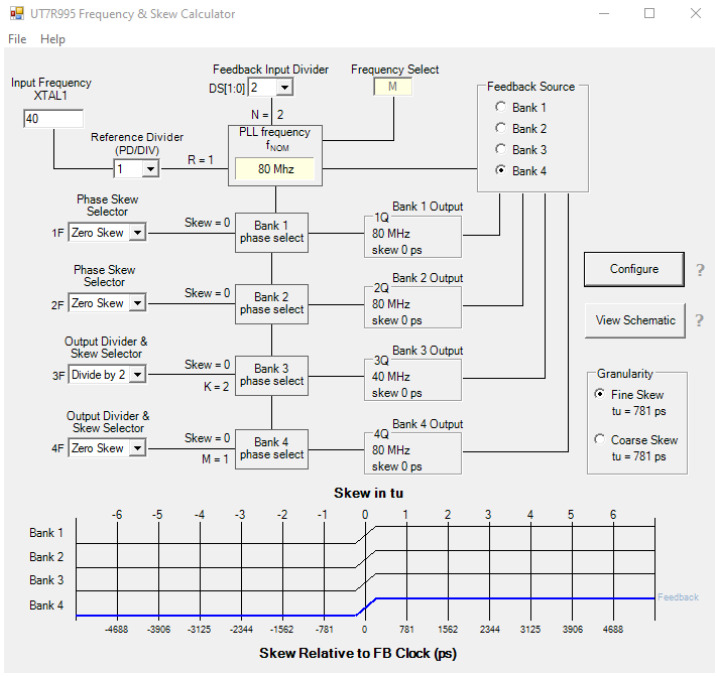

Figure 18b: RadClock™ Frequency & Skew Calculator - Settings

RadClock™ Settings								Clock Frequency (MHz)					Results	
TEST #	DS[1:0] (/N)	FS	PE/HD	PD*/ DIV (/R)	3F[1:0] (/K)	4F[1:0] (/M)	FB	XTAL1 (Ref. Clk.)	1Q [1:0]	2Q [1:0]	3Q [1:0]	4Q [1:0]	3Q[1:0] (FLIP?)	4Q[1:0] (FLIP?)
19B	LL (/N=2)	H	M	H (/R=1)	HH (/K=4)	LL (/M=2)	4Q1	40	160	160	40	80	Y	N

Notes:

1. Trigger = AUX (XTAL1)

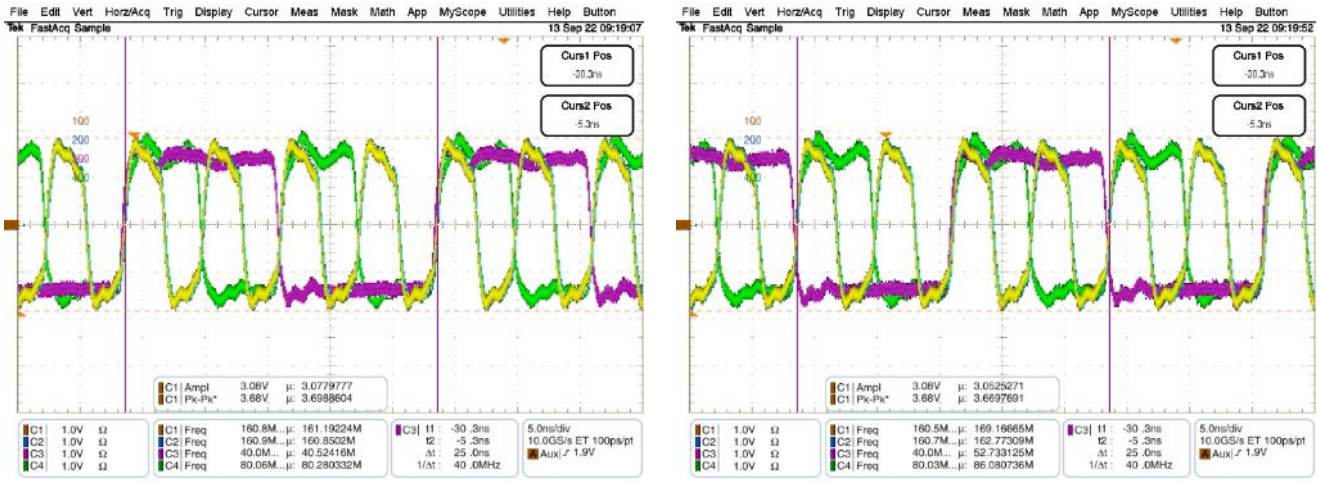

Figure 19a: O'scope waveforms: RadClock™ Output Signals: 1Q0, 2Q0, 3Q0, 4Q0

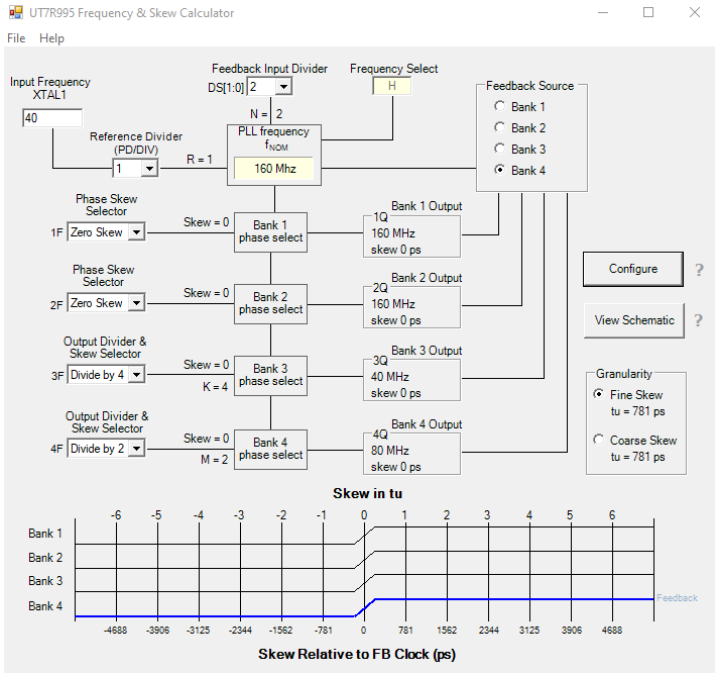

Figure 19b: RadClock™ Frequency & Skew Calculator - Settings

RadClock™ Settings								Clock Frequency (MHz)					Results	
TEST #	DS[1:0] (/N)	FS	PE/HD	PD*/ DIV (/R)	3F[1:0] (/K)	4F[1:0] (/M)	FB	XTAL1 (Ref. Clk.)	1Q [1:0]	2Q [1:0]	3Q [1:0]	4Q [1:0]	3Q[1:0] (FLIP?)	4Q[1:0] (FLIP?)
20D	MM (/N=1)	L	M	H (/R=1)	MM (/K=1)	MM (/M=1)	3Q1	40	40	40	40	40	N	N

Notes:

1. Trigger = AUX (XTAL1)

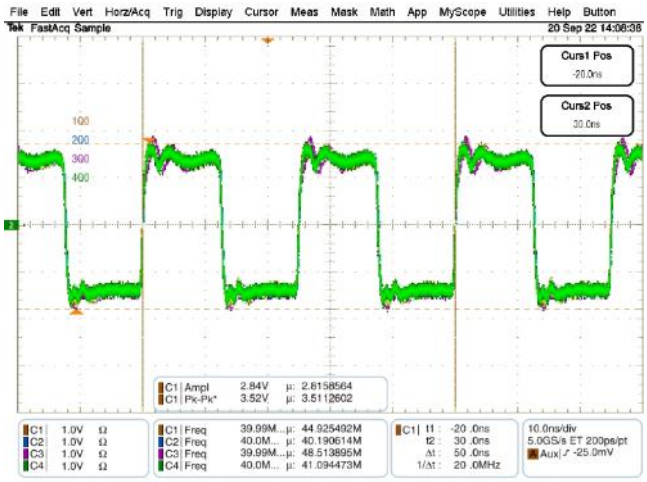

Figure 20a: O'scope waveforms: RadClock™ Output Signals: 1Q0, 2Q0, 3Q0, 4Q0

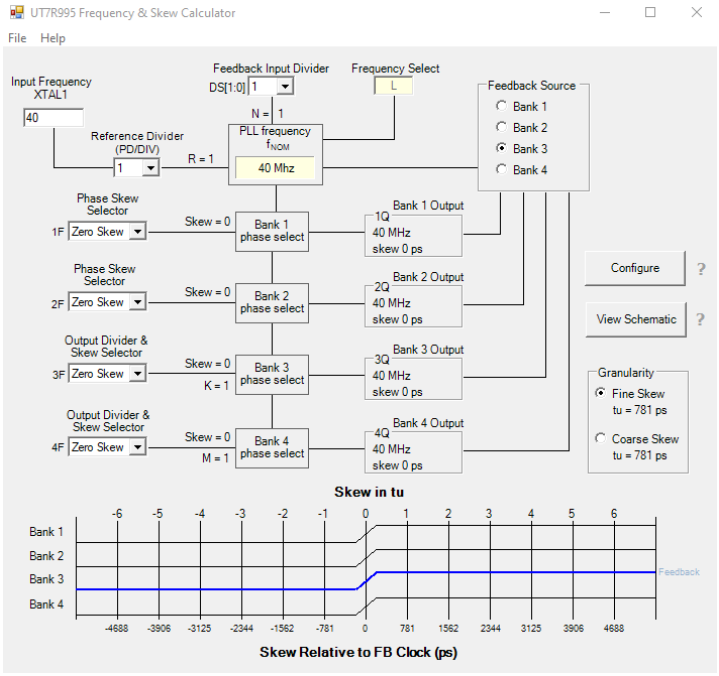

Figure 20b: RadClock™ Frequency & Skew Calculator - Settings

4.1 Measured Data - Discussion

Table 2: Summary of RadClock™ Test Settings and Measured Results

RadClock™ Settings								Clock Frequency (MHz)					Results	
TEST #	DS[1:0] (/N)	FS	PE/HD	PD*/ DIV (/R)	3F[1:0] (/K)	4F[1:0] (/M)	FB	XTAL1 (Ref. Clk.)	1Q [1:0]	2Q [1:0]	3Q [1:0]	4Q [1:0]	3Q[1:0] (FLIP?)	4Q[1:0] (FLIP?)
1A	LL (/N=2)	H	M	H (/R=1)	LL (/K=2)	LL (/M=2)	2Q1	60	120	120	60	60	Y	Y
2A	LL (/N=2)	M	M	H (/R=1)	LL (/K=2)	LL (/M=2)	2Q1	40	80	80	40	40	Y	Y
3A	LL (/N=2)	M	M	H (/R=1)	MM (/K=1)	LL (/M=2)	3Q1	40	80	80	80	40	N	Y
4A	LL (/N=2)	H	M	H (/R=1)	MM (/K=1)	LL (/M=2)	3Q1	80	160	160	160	80	N	Y
5A	LL (/N=2)	H	M	H (/R=1)	LL (/K=2)	LL (/M=2)	3Q1	40	160	160	80	80	N	N
6A	LL (/N=2)	M	M	H (/R=1)	MM (/K=1)	MM (/M=1)	3Q1	40	80	80	80	80	N	N
7A	LL (/N=2)	H	M	H (/R=1)	LL (/K=2)	MM (/M=1)	3Q1	40	160	160	80	160	N	N
8A	LL (/N=2)	H	M	H (/R=1)	HH (/K=4)	LL (/M=2)	3Q1	20	160	160	40	80	N	N
9A†	MM (/N=1)	M	M	M (/R=2)	HH (/K=4)	LL (/M=2)	3Q1	30	60	60	15	30	Y	N
10A	MM (/N=1)	M	M	H (/R=1)	LL (/K=2)	MM (/M=1)	3Q1	40	80	80	40	80	N	N
11A†	MM (/N=1)	L	M	M (/R=2)	LL (/K=2)	MM (/M=1)	3Q1	40	40	40	20	40	Y	N
12A	MM (/N=1)	H	M	H (/R=1)	HH (/K=4)	LL (/M=2)	3Q1	40	160	160	40	80	N	N
13A†	MM (/N=1)	M	M	M (/R=2)	HH (/K=4)	LL (/M=2)	3Q1	40	80	80	20	40	Y	N
14A	LL (/N=2)	H	M	M (/R=2)	HH (/K=4)	LL (/M=2)	3Q1	40	160	160	40	80	N	N
15C	LL (/N=2)	M	M	H (/R=1)	MM (/K=1)	LL (/M=2)	3Q1	40	80	80	80	40	N	Y
16C†	MM (/N=1)	L	M	H (/R=1)	MM (/K=1)	LL (/M=2)	3Q1	40	40	40	40	20	N	Y
17C	LH (/N=4)	H	M	H (/R=1)	MM (/K=1)	LL (/M=2)	3Q1	40	160	160	160	80	N	Y
18B	LL (/N=2)	M	M	H (/R=1)	LL (/K=2)	MM (/M=1)	4Q1	40	80	80	40	80	Y	N
19B	LL (/N=2)	H	M	H (/R=1)	HH (/K=4)	LL (/M=2)	4Q1	40	160	160	40	80	Y	N
20D	MM (/N=1)	L	M	H (/R=1)	MM (/K=1)	MM (/M=1)	3Q1	40	40	40	40	40	N	N

Notes:

1. O'scope Trigger = AUX (XTAL1) unless otherwise noted.
2. † O'scope Trigger = AUX (XTAL1) clock divided by 2.

The rightmost two columns of Table 2 (Results) show whether or not the Bank 3, 4 (3Q[1:0]; 4Q[1:0]) outputs changed state (from logic high/low to low/high or vice-versa) upon RadClock™ startup, as defined as the PD*/DIV Reset pin momentarily set to logic low (0V). A "FLIP" indicates different output logic states between different startup events. In one case, then, the startup logic state of the indicated Bank 3, 4 output clock phase would be inverted with-respect-to the RadClock™ XTAL1 reference clock input.

4.2 Additional Measured Data

Additional measurements were made using the RadClock™ evaluation board UT7R995-EVB, S/N 2023-003, for two of the previous UT7R995 RadClock™ configurations. PD*/DIV was held low (power-down) prior to a single trigger waveform capture on the first rising edge of Channel 1 (1Q0). This procedure was repeated either four times (Test 3A), or two times (Test 11A) to show the different startup states for outputs 3Q0 or 4Q0. The time scale for all plots is 50 µs/div. Note that the PLL lock time, t_{LOCK} electrical timing spec. is 0.5 ms (500 µs) max.

RadClock™ Settings								Clock Frequency (MHz)					Results	
TEST #	DS[1:0] (/N)	FS	PE/HD	PD*/ DIV (/R)	3F[1:0] (/K)	4F[1:0] (/M)	FB	XTAL1 (Ref. Clk.)	1Q [1:0]	2Q [1:0]	3Q [1:0]	4Q [1:0]	3Q[1:0] (FLIP?)	4Q[1:0] (FLIP?)
3A	LL (/N=2)	M	M	H (/R=1)	MM (/K=1)	LL (/M=2)	3Q1	40	80	80	80	40	N	Y

Notes:
1. Trigger = 1Q0; O'Scope Ch. 1, 80 MHz

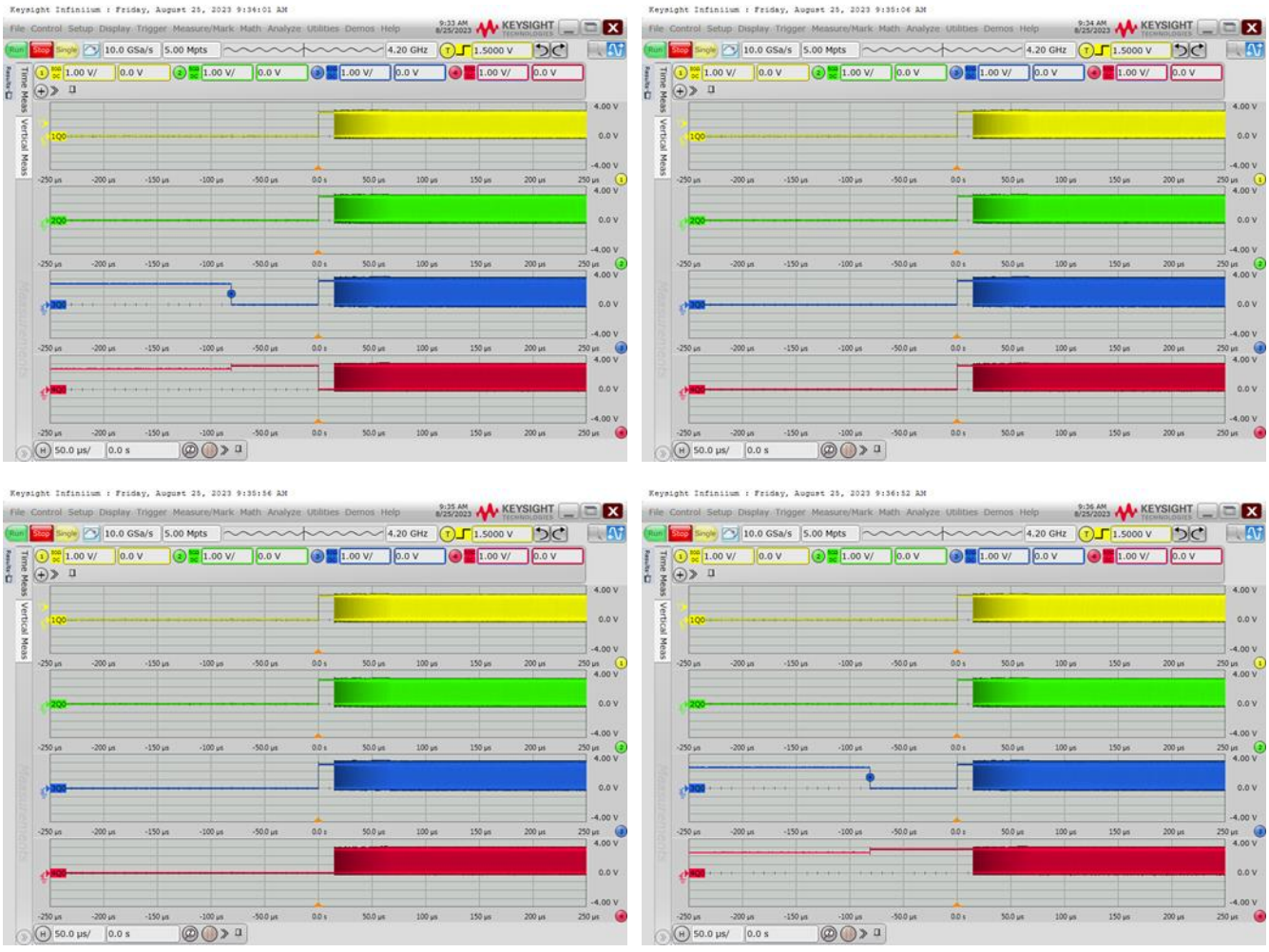

Figure 3a2: O'scope waveforms: RadClock™ Output Signals: 1Q0, 2Q0, 3Q0, 4Q0

RadClock™ Settings								Clock Frequency (MHz)					Results	
TEST #	DS[1:0] (/N)	FS	PE/HD	PD*/ DIV (/R)	3F[1:0] (/K)	4F[1:0] (/M)	FB	XTAL1 (Ref. Clk.)	1Q [1:0]	2Q [1:0]	3Q [1:0]	4Q [1:0]	3Q[1:0] (FLIP?)	4Q[1:0] (FLIP?)
11A	MM (/N=1)	L	M	M (/R=2)	LL (/K=2)	MM (/M=1)	3Q1	40	40	40	20	40	Y	N

Notes:
1. Trigger = 1Q0; O'Scope Ch. 1, 40 MHz

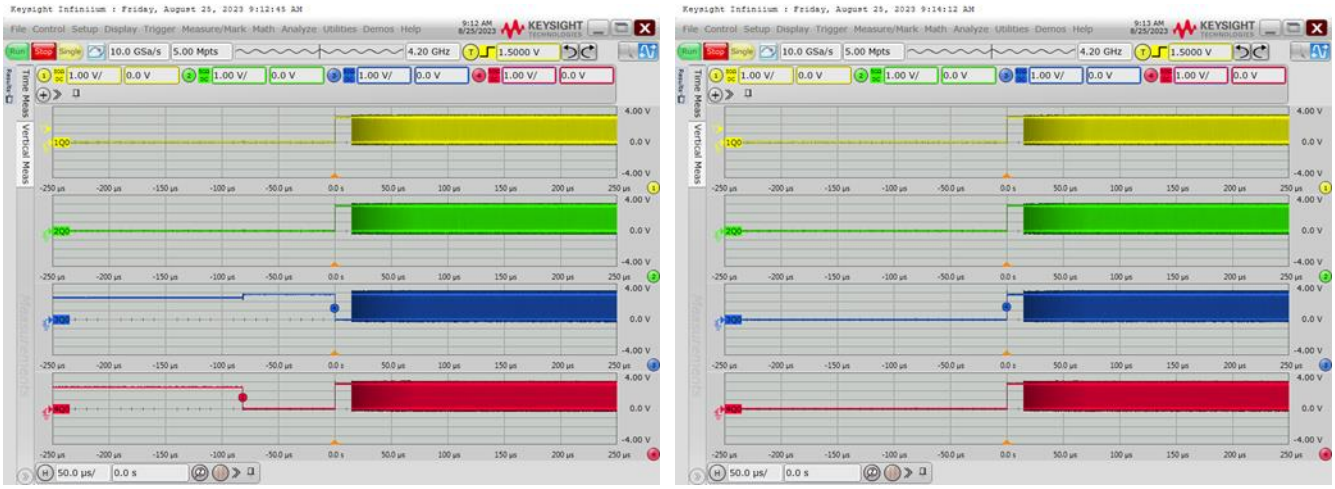

Figure 11a2: O'scope waveforms: RadClock™ Output Signals: 1Q0, 2Q0, 3Q0, 4Q0

5.0 Summary and Conclusions

This Application Note (AN) documents an observed startup condition when using the Bank 3 (/K), 4 (/M) output dividers, which is dependent on the RadClock™ overall configuration, including feedback (FB) path and divider settings. It has been empirically determined by measurements that in some instances, Bank 3 (/K) and Bank 4 (/M) output dividers with divide ratios other than /1 (i.e. /2 or /4) can result in output clock phase uncertainty at startup with-respect-to the input reference clock, XTAL1.

This information is provided as guidance when using the RadClock™ Bank 3 and/or Bank 4 output dividers with divide ratios other than /1. We recommend that product users check the corresponding clock outputs to determine if this issue exists for the selected user configuration. A general guideline is to assume that the Bank 3 (/K) and Bank 4 (/M) output clock dividers can initialize in either a logic low or high state at start-up. There is no workaround available for those use cases where this start-up indeterminacy behavior is observed.

Finally, there are four configurations given in this AN where the o'scope plots for either the Bank 3 (3Q0) or Bank 4 (4Q0) outputs show both logic low and logic high traces at the same time. These cases are for TEST #'s: 9A, 11A, 13A, and 16C. This is a result of the RadClock™ output divider ratios and FB connections yielding clock output frequencies of one-half of the reference clock input frequency. To show only a single a single logic state at a given time for these test cases, the o'scope input clock trigger is set to XTAL1 divided by two (/2).

The general output frequency calculations are given in the RadClock™ Datasheet, p.6, Table 6: "Calculating Output Frequency Settings." This Datasheet table is reproduced here for reference as Table 3.

Table 3: Calculating Output Frequency Settings

Configuration	Output Frequency		
Clock Output Connected to FB	1Q[1:0] [1] and 2Q[1:0] [1]	3Q[1:0]	4Q[1:0]
1Qn or 2Qn	(N/R) * f_{XTAL}	(N/R) * (1/K) * f_{XTAL}	(N/R) * (1/M) * f_{XTAL}
3Qn	(N/R) * K * f_{XTAL}	(N/R) * f_{XTAL}	(N/R) * (K/M) * f_{XTAL}
4Qn	(N/R) * M * f_{XTAL}	(N/R) * (M/K) * f_{XTAL}	(N/R) * f_{XTAL}

Note:

1. These outputs are undivided copies of the VCO clock. Therefore, the formulas in this column can be used to calculate the nominal VCO operating frequency (f_{NOM}) at a given reference frequency (f_{XTAL}) and the divider and feedback configuration. The user must select a configuration and a reference frequency that will generate a VCO frequency that is within the range specified by FS pin.

6.0 Appendix A - Test Equipment Setup

6.1 Test Equipment Setup – Sections 4.0 and 4.1 (Previous Data)

Test equipment setup for measured results as described in Sections 4.0 and 4.1 is shown in Figures 22 and 23, below.

Figure 22: Test Equipment Setup for Sections 4.0 and 4.1 – Test Bench

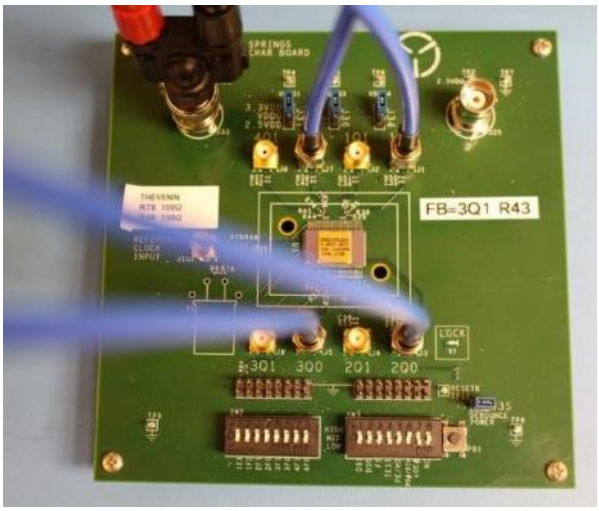

Figure 23: Test Equipment Setup for Sections 4.0 and 4.1 – UT7R995-EVB

6.1 Test Equipment Setup – Section 4.2 (New Data)

Test equipment setup for measured results as described in Section 4.2 is shown in Figures 24 and 25, below.

Figure 24: Test Equipment Setup for Section 4.2 – Test Bench

Figure 25: Test Equipment Setup for Section 4.2 – UT7R995-EVB

REVISION HISTORY

Date	Rev. #	Author	Change Description
09/21/2023	1.0.0	BRM	New