SDRAM to UT700 LEON 3FT Timing & Signal Integrity Analysis UT8SDMQ64M40/48 2.5 & 3.0Gb SDRAM

Table 1: Cross Reference of Applicable Products

Product Name	Manufacturer Part Number	SMD #	Device Type	Internal PIC Number
SDRAM	UT8SDMQ64M40/48	5962-10229/30	Memory	QS18/19
LEON 3FT	UT700	5962-13238	3FT Processor	WQ03
RadClock	UT7R955/C	5962-05214	Clock Generator	WD27/35

1.0 Overview

This application note examines the interconnect between CAES' 2.5Gb and 3.0Gb SDRAM modules and CAES' UT700 LEON 3FT SPARC™ V8 Microprocessor from both a timing and signal integrity perspective. Analysis is performed using a direct connection of the two devices while also discussing the possible benefits of using CAES' UT7R955 RadClock for buffering the SDRAM clock signal. Timing analyses of the interconnection are performed using datasheet specifications as well as utilizing extensive physical measurement which account for the timing variance due to signal properties. Additionally, variance in signal timing due to temperature, voltage and total dose irradiation are addressed. Simulation results are presented and compared to actual measurements. While physical measurements and simulations were performed using CAES' UT700 internal Matilda evaluation board, the signal integrity and timing analysis is expected to extend to other memory controlling devices.

For simplicity, the UT700 LEON 3FT SPARC™ V8 Microprocessor will hereafter be referred to as LEON. Reference to the SDRAM module will be with respect to the 3.0Gb SDRAM as this is considered worst case from a timing and signal integrity perspective.

2.0 Background

The internal configuration of CAES' SDRAM module is complex. This complexity is necessary to provide our customers with the desired memory density and bus widths in a single hermitically sealed device. CAES' QML (Qualified Manufacturers List) Q level qualified SDRAM devices meets the all the stringent mechanical qualification requirements in the form of a device SMD (Standard Microelectronic Drawing) issued by DLA (Defense Land and Maritime). Like many engineering design choices, this complexity results in a tradeoff between board space savings and performance. The internal configuration necessary to meet Aerospace's and DLA's group D mechanical requirements adds additional line impedances which affects signal integrity. This complexity also creates difficulty in providing an accurate IBIS (Input/output Buffer Information Specification) model. Improvements have been made by creation of an S-Parameter model. Given these tradeoffs, CAES believes the x40 and x48 bus width SDRAM modules provide an enhanced solution over the alternative of using separate x8 devices which of course would present its own signal and timing design challenges. The information and data presented in this application note intends to alleviate concerns with using CAES' 2.5Gb x40 and 3.0Gb x48 SDRAM processor memory solution.

3.0 Applicable Documents and Equipment

CAES datasheets:
UT700 LEON 3FT SPARC™ V8 Microprocessor
UT8SDMQ64M40/48 2.5&3.0-Gigabit SDRAM MCMs
UT7R995 & UT7R995C RadClockTM

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Measurement equipment:
Teledyne LeCroy WaveRunner 625Zi 40Gs/sec Oscilloscope
GGB Industries Inc Model 12C Picoprobe (2)
CAES internal UT700 Matilda evaluation board

4.0 Timing Analysis

4.1 SDRAM to UT700 LEON SDRAM port direct connection

Background information: CAES' Standard Products Organization offers a standalone 2.5Gb and 3.0Gb SDRAM QCOTS (Quantified Commercial Off The Shelf) MCM (multi-chip module) memory device. The SDRAM modules were developed to provide the aerospace industry the option of a QML Q level qualified data processing memory solution in a single hermetic package. The device is offered in both x40 and x48 bus width configuration.

Both the LEON and SDRAM products are tested to meet all datasheet and SMD specifications across full operating temperature and voltage ranges for all non proto devices. Additionally, sample testing is performed to verify devices remain within these specifications after burn-in, dynamic life and irradiation testing (end of life).

During developmental characterization, CAES ideally sets specification limits, including AC timing parameters, to provide a minimum statistical Cpk value of two ideally resulting in a six sigma margin to the mean. During final tri-temperature device testing, all specifications are guaranteed as published in the datasheets and SMDs unless otherwise noted. Therefore, inherent margin is built into the process and testing. While many of the specifications discussed below overlap, typically there are hundreds of picoseconds to nanoseconds of margin to every timing parameter tested. This is typical, and there is no guarantee that a device limit did not pass at the given specified value. If a parameter passed at the given limit, it would likely occur during one of the worst case temperatures (−40C & +105C) and worst case operating voltage(3.0V & 3.6V). Therefore, it is reasonable to suppose at closer to nominal voltage and temperatures , margin exists.

SDRAM to LEON direct connection datasheet timing analysis: A direct connection to CAES' LEON is feasible; however, timing analysis for individual customer specific system requirements should be verified. The LEON can operate up to a maximum frequency of 166MHz. CAES' SDRAM's maximum operating frequency is 100MHz. The LEON input system clock to SDCLK output is either a fin/1 or fin/2 which means the SDRAM port output clock is either the same frequency as the LEON clock or divided by two respectively. This results in two possible fastest operations. The first is using the fin/1 whereby providing both the LEON and SDRAM a 100MHz clock. The second is using the fin/2 providing the LEON with 166MHz clock and the SDRAM an 83MHz clock. Datasheet timing analysis will be shown for 100MHz and 75MHz SDRAM operation. 75MHz was chosen for hardware and physical measurement correlation while also being relatively close to 83MHz.

The SDRAM device require a minimum address (tAS), data (tDS), and control input (tCMS) setup times to the rising edge of its SDRAM CLK input. Figure #1 is a detailed datasheet timing analysis of the SDRAM to LEON at 100MHz clock operation. The aforementioned SDRAM setup times all overlap the specifications of the LEON SDRAM memory port control outputs. For example, the LEON SDCLK to address valid output maximum time (t1a) is specified at a maximum of 8.5ns. When running at 100MHz frequency or 10ns period clock cycle, this leaves a remaining 1.5ns before the next rising clock edge which is the required SDRAM address setup time (thus the specification between the two devices overlap). The other input specifications are similar.

Running at lesser frequencies, results in providing margin for all SDRAM setup specifications. Figure #2 is a detailed datasheet timing analysis of running the SDCLK at 75MHz or 13.3ns cycle. The worst case address setup time would

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be increased to 4.8ns (1.5ns plus the additional 3.3ns clock cycle increase) which gives margin to the 1.5ns tAS

SDRAM specification. While slower clock frequency (less than 100MHz) increases all the SDRAM signal setup times, it does not provide additional margin for any of the SDRAM input signal hold time requirements. In order to achieve margin for the hold time requirements, the following section examines the addition of a clock generator circuit.

4.2 SDRAM to UT700 LEON SDRAM port using RadClock interconnect

SDRAM to LEON connection timing analysis using a clock generator: Some systems designers are required to provide timing margin to the specifications. In such cases, implementing a clock generator circuit similar to CAES' UT7R995 RadClock which can skew the clock signal in a negative direction provides a solution. This solution is only applicable when using clock frequencies less than 100MHz where setup time is gained by the longer SDRAM clock input cycle. By skewing the SDRAM clock input back in time relative to the other SDRAM address, data, and control signals, the margin gained to the setup times can be skewed towards the SDRAM hold time requirements. Ideally, dividing the extra clock cycle time by two results in an even distribution of margin to both setup and hold time requirements.

In the previous 75MHz example, the typical setup time was increased by 3.3ns by increasing the SDCLK clock cycle from 10ns to 13.3ns. By using the RadClock, the extra 3.3ns can be ideally divided in half by shifting the SDRAM clock 1.65ns in the negative direction (prior to LEON SDCLK output). The following example is an ideal timing analysis using ideal signals meant to show the theory of applying a clock buffer. Due to the loading of the SDRAM module which distorts the clock ideal rise and fall times, a timing analysis of the real world signals will be performed latter in the publication.

The RadClock is capable of shifting a received clock a maximum of six time units in either the positive or negative direction. For the purposes of this analysis, the clock would ideally be shifted or skewed 1.65ns in the negative direction. The first step is to calculate the RadClock time unit as given by the RadClock UT7R995 datasheet as:

$$tu = \frac{1}{f \text{ NOM} * \text{MF}}$$

Where tu = time unit: fNOM = clock frequency: MF = multiplication factor given by datasheet Therefore: tu = .83ns for fNOM of 75MHz and MF of 16. The ideal shift in the example can be almost exactly obtained by a −2tu shift resulting in −1.66ns skew. Depending on the frequency, that may not always be the case, but a reasonably close option should be available. The timing diagram of Figure 3 shows the results of skewing the SDRAM clock input −1.65ns. All the SDRAM required hold times are now provided with additional margin as a result of using the RadClock to adjust the clock. While the skew provides additional margin to the SDRAM hold time requirements for all input signals, it does create a tradeoff for the LEON data input required hold time (t6a) of 1.5ns. As the timing diagram shows t6a timing is now reduced to 1.05ns which does not meet the LEON required data hold time of 1.5ns. One solution is to only skew the clock one time unit (−1tu) or 0.83ns resulting in less margin for SDRAM required signal hold times, but bringing the LEON data hold time within specification. However, as mention earlier, this analysis assumes ideal signals. The follow section concludes that this is not a concern as the actual clock signal rise time provides its own skew self-correcting for data being read by the LEON.
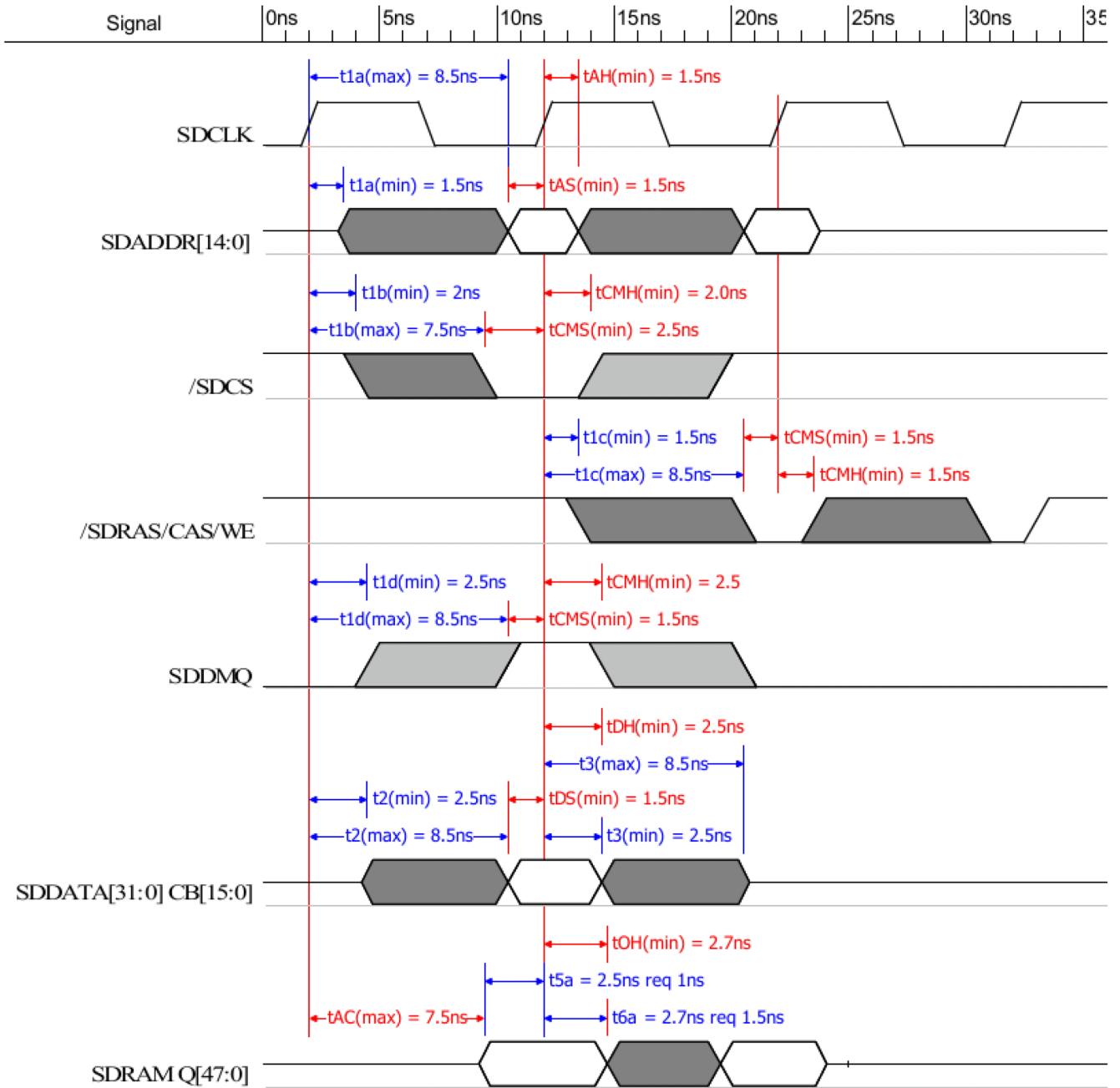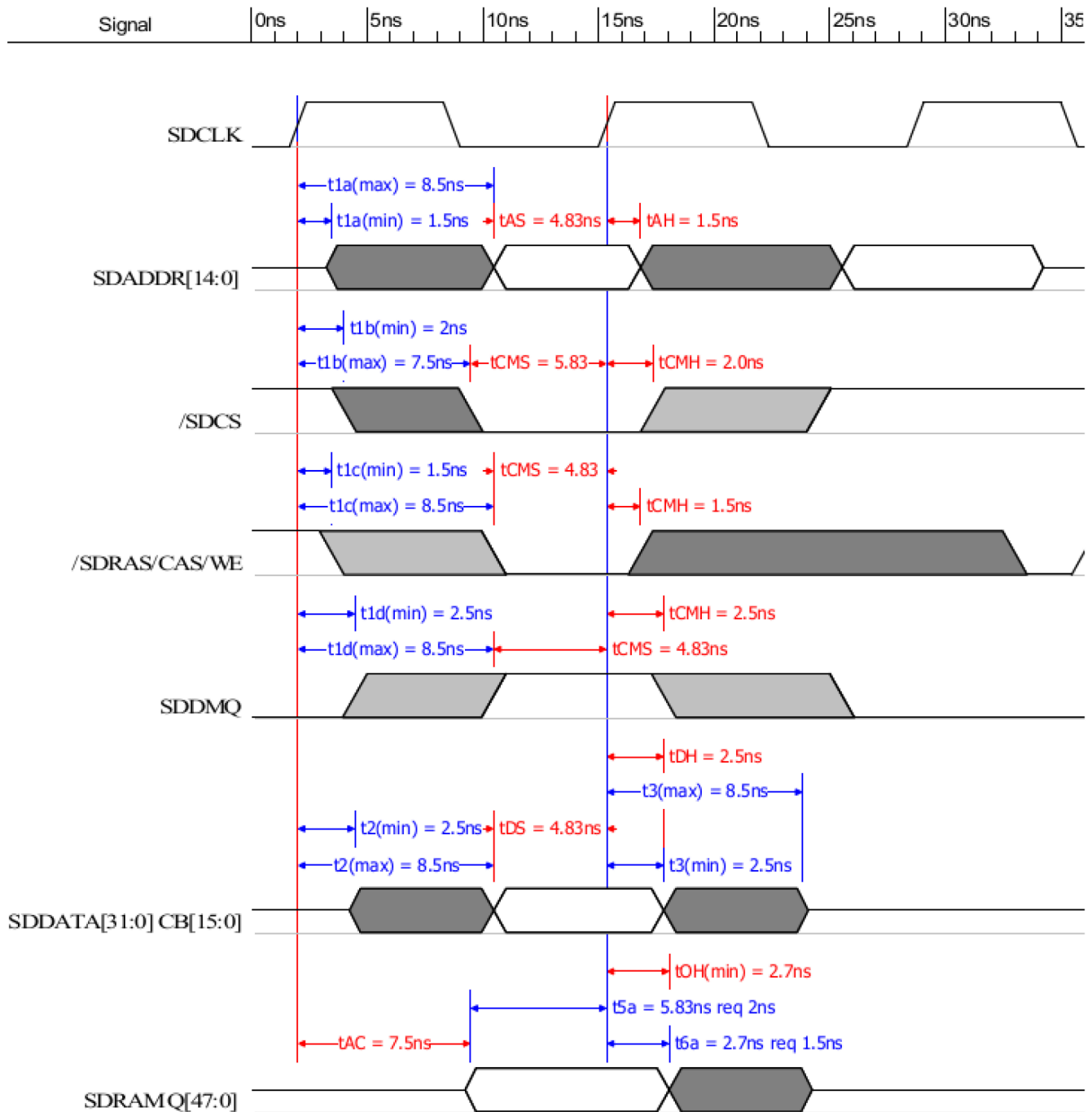
APPLICATION NOTE

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Figure 1: 100MHz datasheet timing analysis LEON to SDRAM direct connection

LEON UT700 specification given in blue
SDRAM UT8SDMQ64M48 specification given in red

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Figure 2: 75MHz datasheet timing analysis LEON to SDRAM direct connection

LEON UT700 specification given in blue
SDRAM UT8SDMQ64M48 specification given in red

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SDRAM to UT700 LEON 3FT Timing & Signal Integrity Analysis UT8SDMQ64M40/48 2.5 & 3.0Gb SDRAM
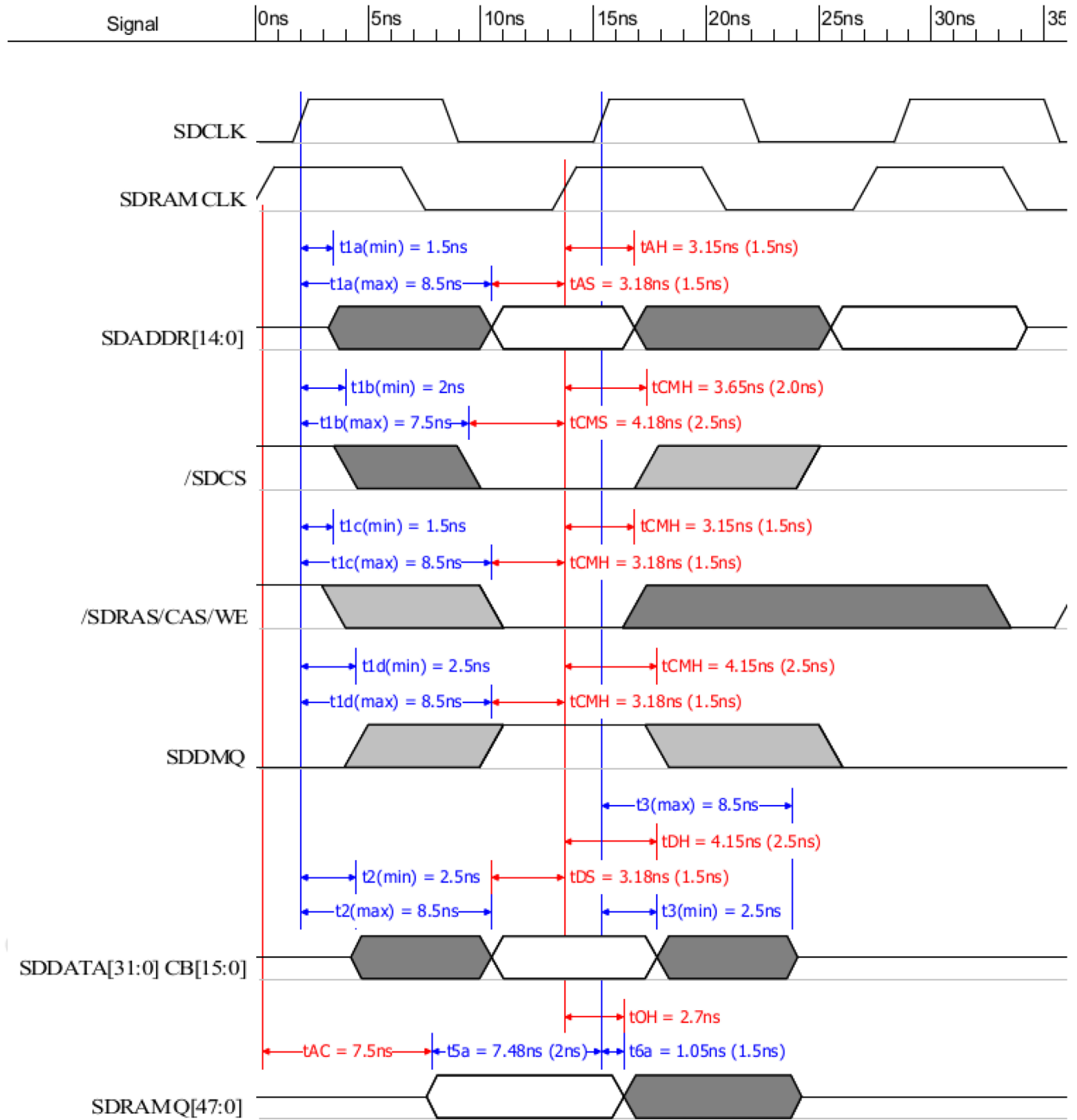
Figure 3: 75MHz datasheet timing with RadClock −1.65ns skew to SDRAM

LEON UT700 specification given in blue

SDRAM actuals given in red with requirements in parenthesis (xxns) when applicable

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5.0 SDRAM Signal Integrity

5.1 SDRAM Package Layout

From a signal integrity standpoint, reviewing the block diagram (Figure 4) and package layout (Figure 5) provides insight into simulation results. The package is arranged in a five or six active die configuration. Each active die is an individual full functioning 512Mb x 8 SDRAM device. Additionally, each active die is accompanied by a smaller signal routing die. The five or six die inputs are bussed together to create a single x40 or x48 bus width memory device respectively. The package is a dual cavity package containing three active die in the top cavity and two or three active die in the bottom cavity. For the purpose of the remainder of this paper, only the six active die module is considered as this represents the worst case for signal integrity and timing. The trace routing is such that each of the three die in the top are paired with one die in the bottom cavity to create three distinct pairs of different length daisy chain signal paths (Figure 6).

All control and input signals are bussed together with the exception of the DQMx (data mask) and data I/O pins. The bussed input signals use similarly matched package routing lengths. The fastest and highest priority signal with respect to both functionality and signal integrity is the SDCLK input signal. The SDCLK signal is the focus of the following simulations and measurements.

5.2 HyperLynx simulations SDRAM to UT700

Using CAES' LEON IBIS and SDRAM S-Parm models as well as the Matilda UT700 evaluation board design files, the following HyperLynx circuit was created and simulations performed. While the Matilda evaluation board does make use of the RadClock, the simulations were performed as a direct connection with the RadClock removed from the circuit. This was done in order to correlate with the actual circuit measurements presented later as the RadClock was physically bypassed. For accuracy, the board design files were used to create the transmission line impedances pre and post RadClock circuit. A wire stackup was then inserted to achieve the impedance of the physical wire used to bypass the RadClock during the actual measurements.

Simulation circuit and results at 75MHz are shown in figures 7-12. The simulation results show that the clock signal at the SDRAM package pin has large reflections. However, the signal integrity at each die does not show the large reflection and are almost completely monotonic. As noted earlier, there are three distinct signal paths with matching signal characteristics. It is important to note the delay between the outgoing SDCLK signal of the LEON to the 50% signal transition at the die. This delay becomes significant in evaluating actual interconnect timing.

Simulations were performed at 100MHz and results shown on figure 13-17. Note the attenuation of the signals reduce the voltage swing to approximately 3.0V. Resistor at R105 was replaced with a 10 ohm resistor and new simulation resulted in full voltage swing of approximately 3.3V as shown on figure 14. In retrospect a resistance of 15 ohms would have probably been a better solution, but physical measurements were taken with R105 = 10 ohms.
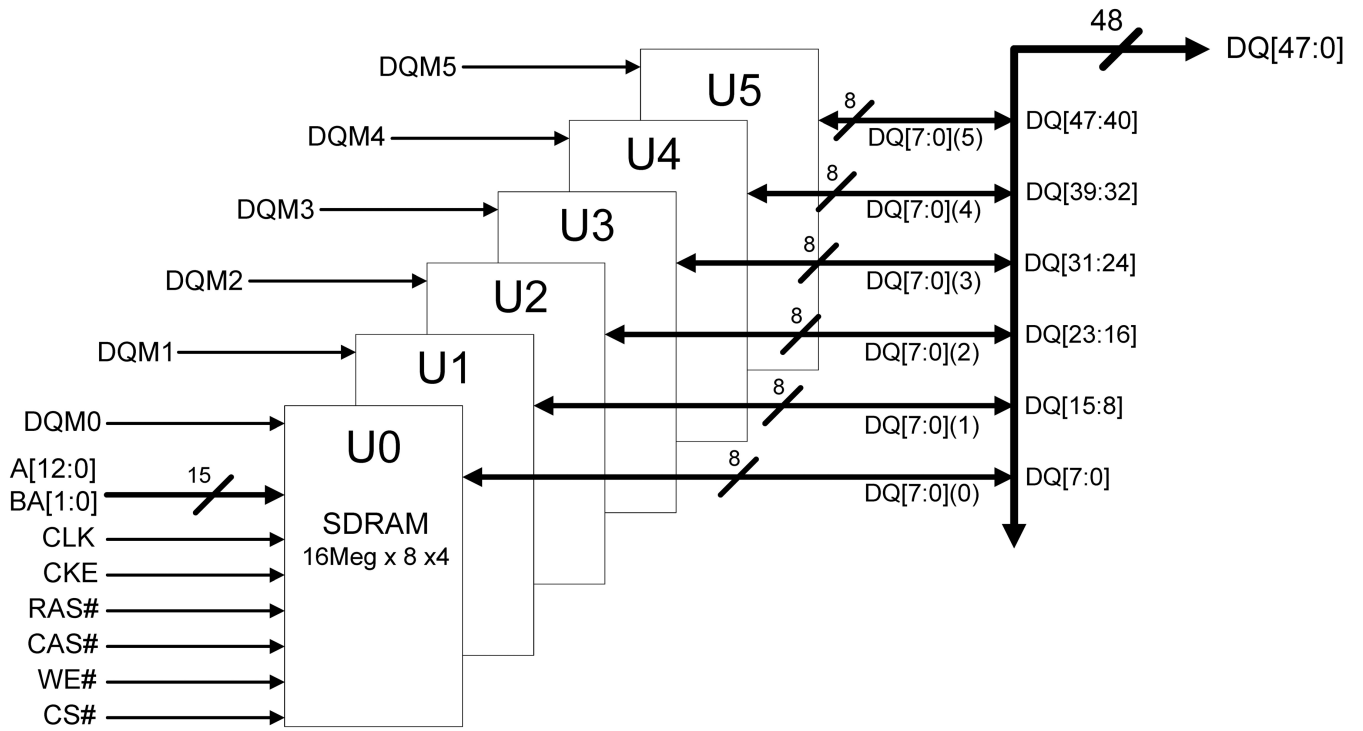
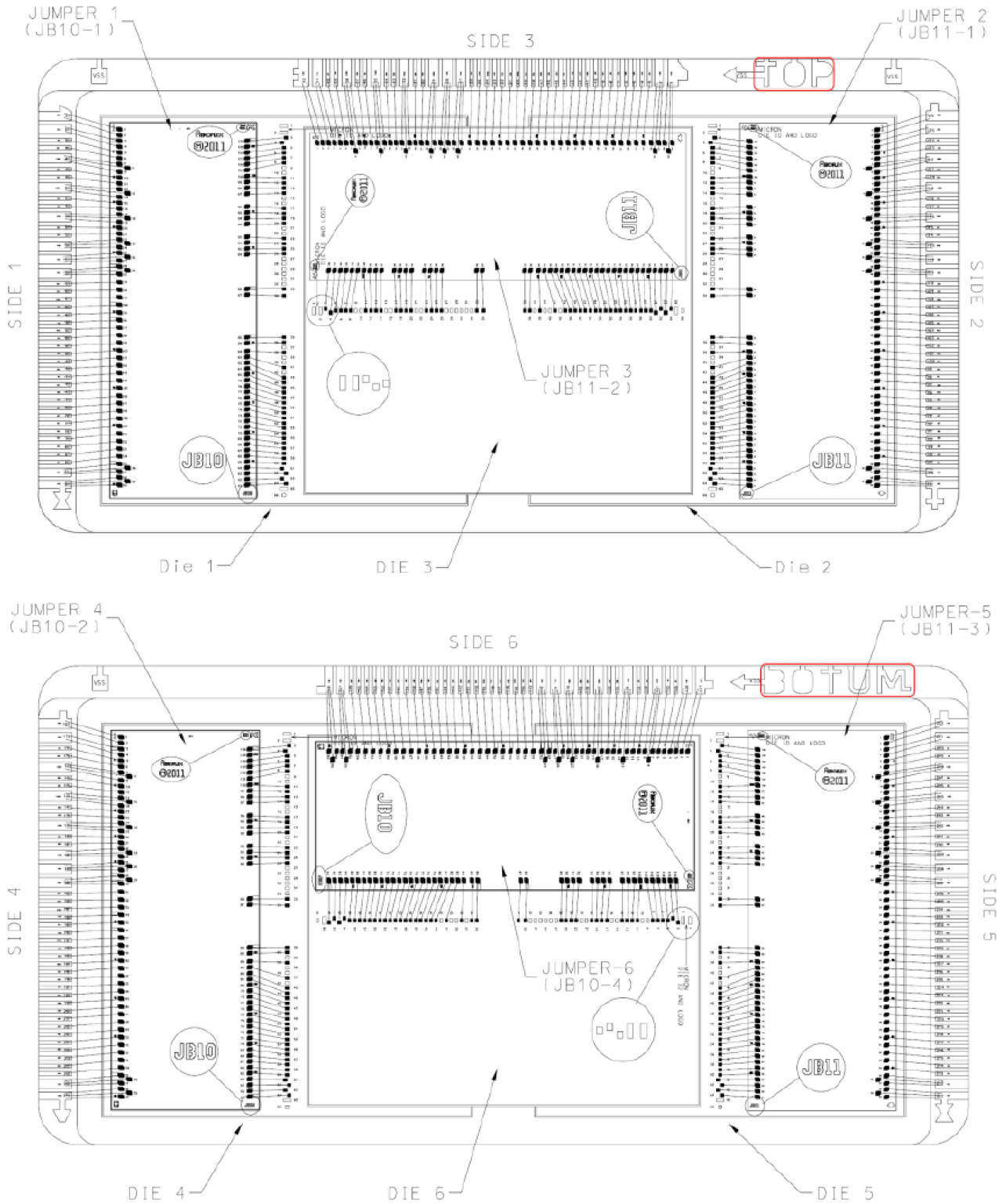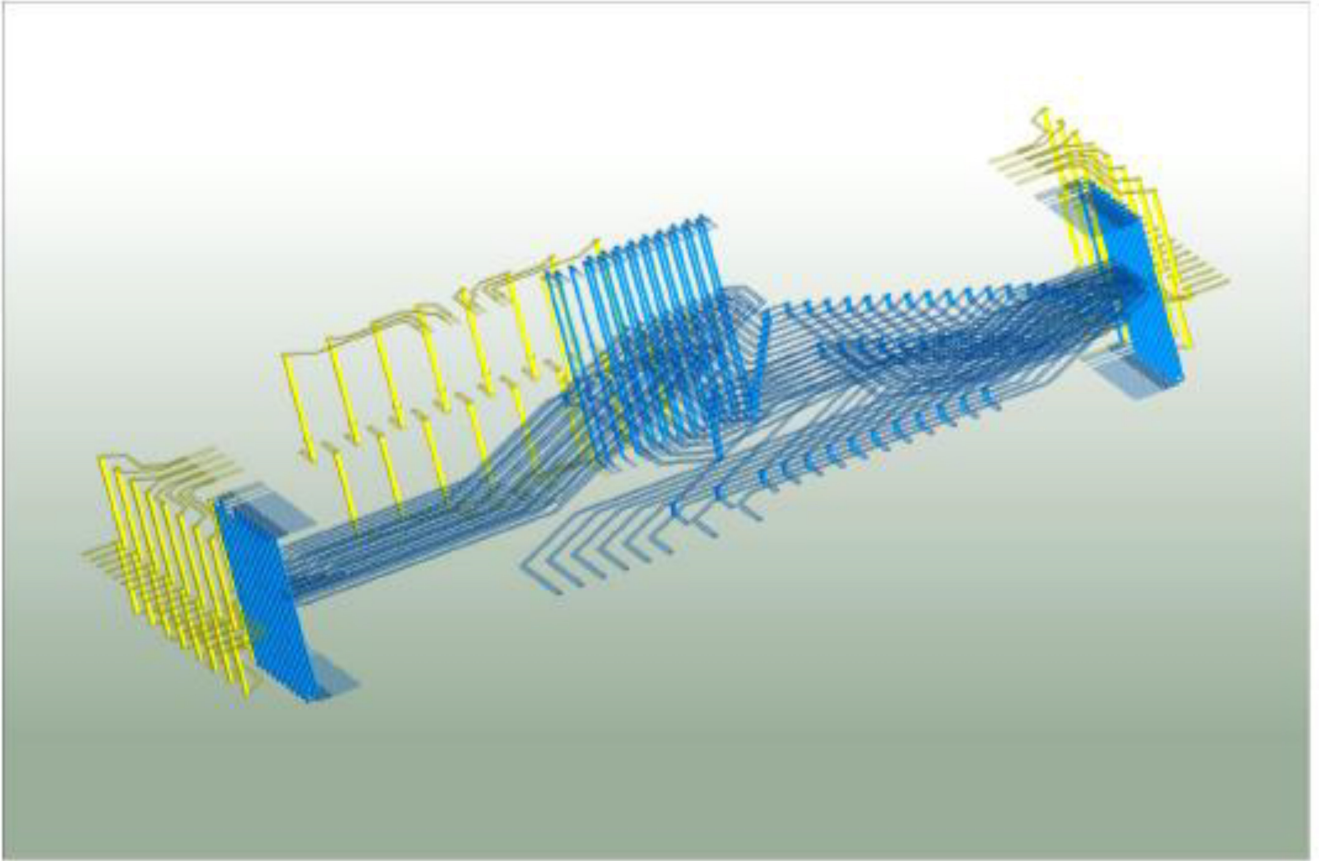Figure 4: UT8SDMQ64M48 6 die MCM functional block diagram

Figure 5: Top and Bottom Cavity Layout Configuration

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Signal Routing, Isometric

AD [12:2], BA[1:0], CASB, CKE, CLK, CSB, RASB, WEB
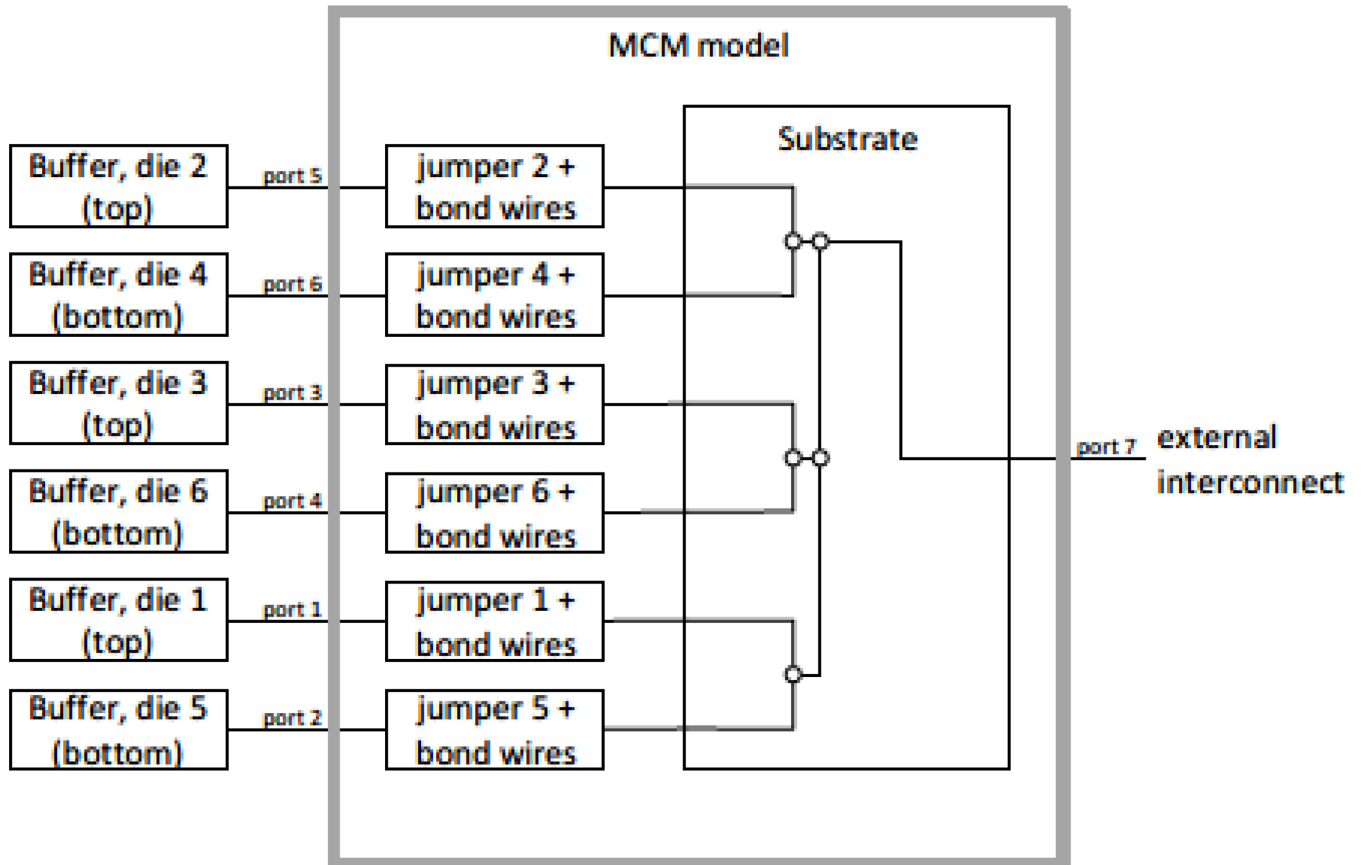
Figure 6: Package Routing and Resulting IBIS Layout

Designfile:UT700_dir_conn_matilda_board_files_S_PARM_model.ffs<H:\MyDocs\Memories\SDRAM\Matilda_board_sims_June_2018\>HyperLynx LineSim v9.4.1
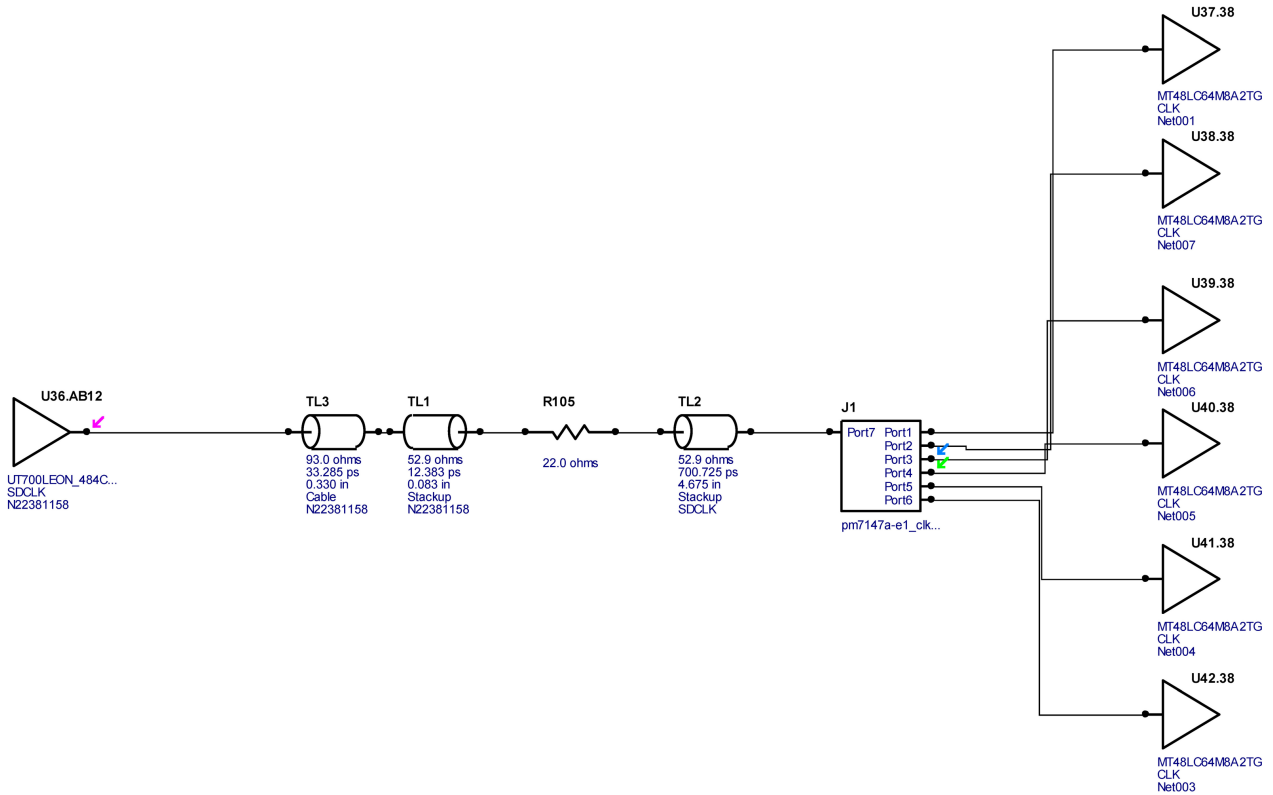
Figure 7: Simulation schematic using LEON and SDRAM S-Parm IBIS model

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OSCILLOSCOPE
Design file: UT700_DIR_CONN_MATILDA_BOARD_FILES_S_PARM_MODEL.FFS
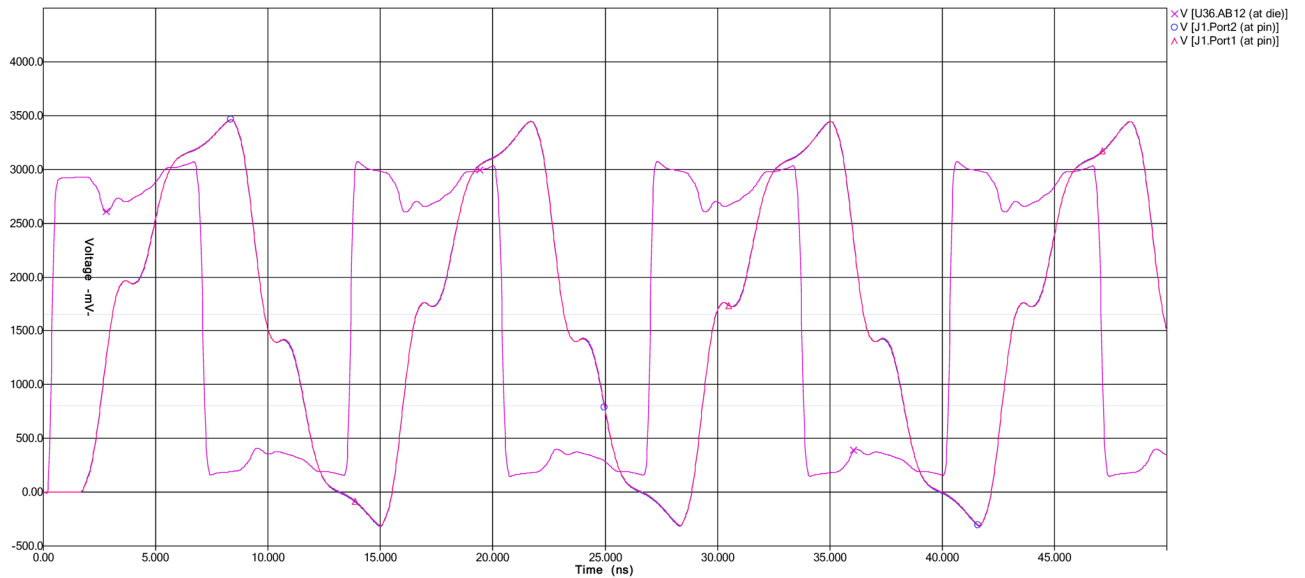Designer: Leslie, Mike (SSA)
HyperLynx v9.4.1
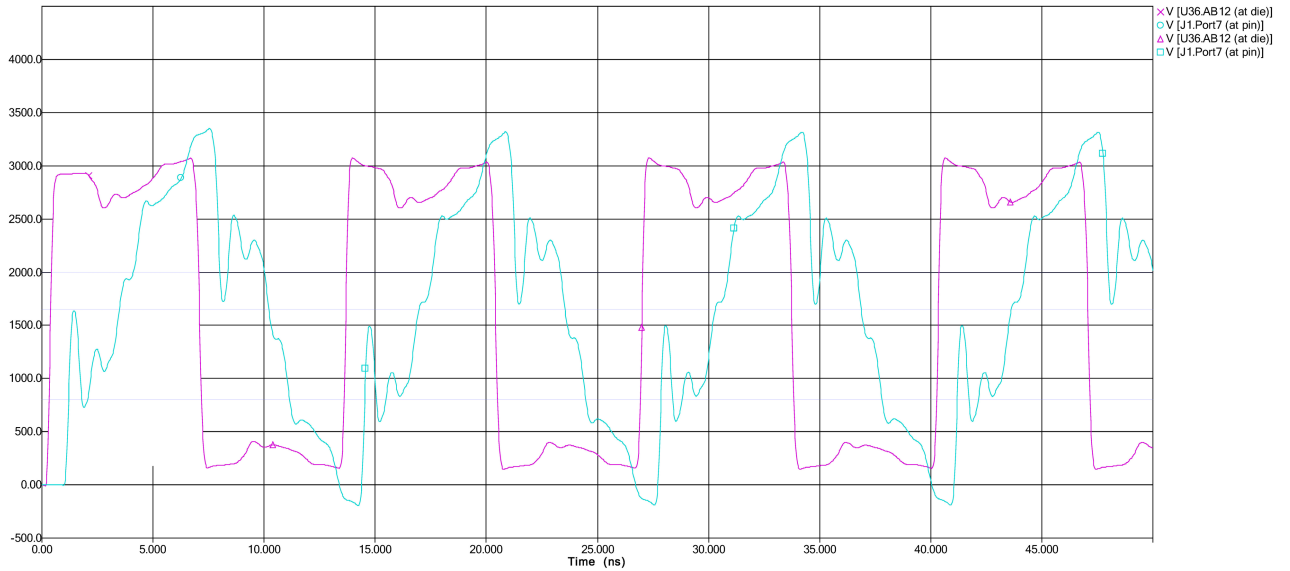
Figure 8: 75MHz simulation LEON SDCLK output (red) and SDRAM SDCLK input (teal)
Date: Friday Feb. 1, 2019 Time: 15:06:18
Net name: N22381158
Show Latest Waveform = YES, Show Previous Waveform = YES

SDRAM to UT700 LEON 3FT Timing & Signal Integrity Analysis UT8SDMQ64M40/48 2.5 & 3.0Gb SDRAM

OSCILLOSCOPE
Design file: UT700_DIR_CONN_MATILDA_BOARD_FILES_S_PARM_MODEL.FFS
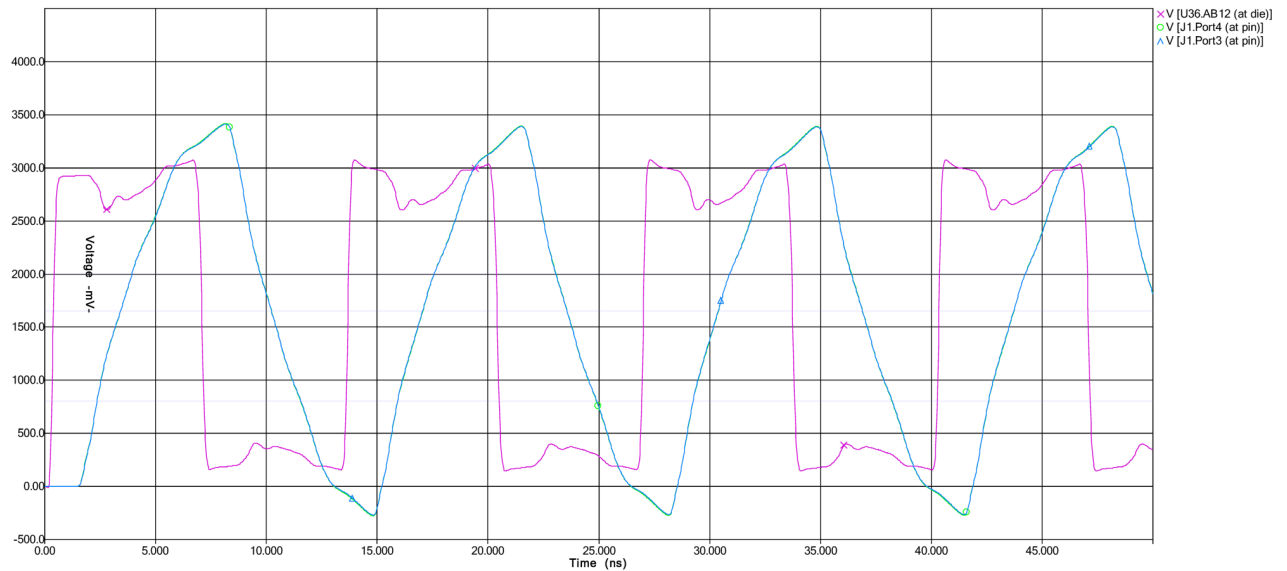Designer: Leslie, Mike (SSA)
HyperLynx v9.4.1
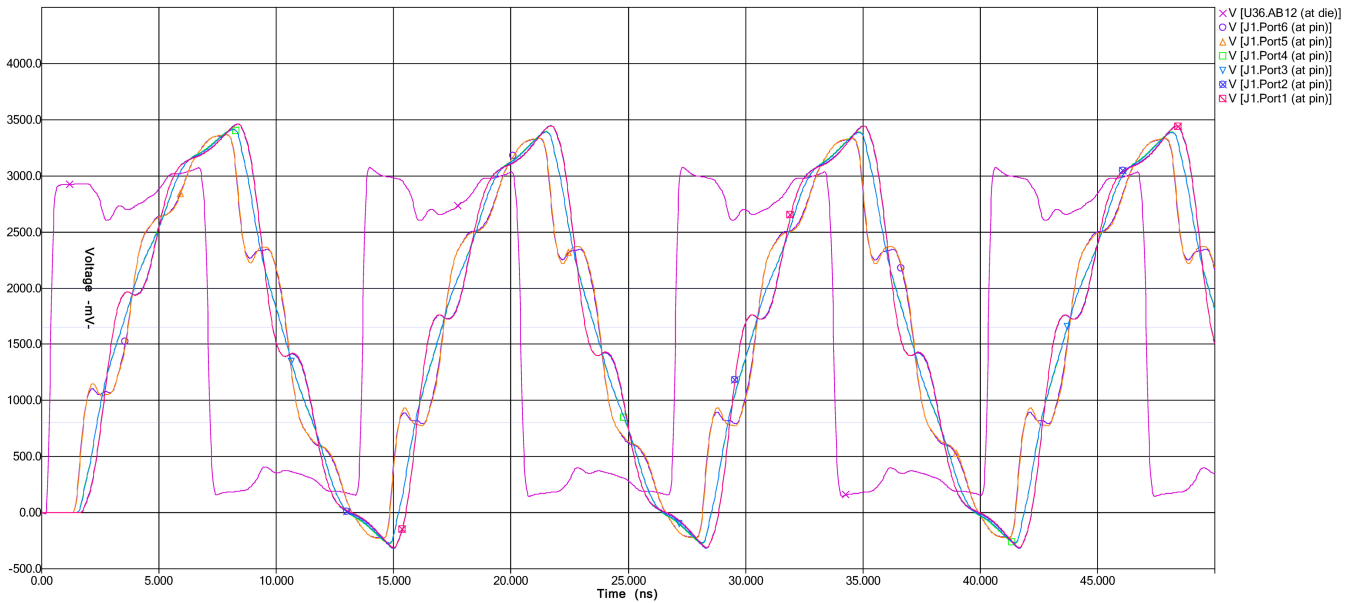
Figure 9: 75MHz simulation LEON SDCLK output (red) SDRAM SDCLK input at die (1-6)
Date: Friday Feb. 1, 2019 Time: 15:19:28
Net name: N22381158
Show Latest Waveform = YES, Show Previous Waveform = YES

SDRAM to UT700 LEON 3FT Timing & Signal Integrity Analysis UT8SDMQ64M40/48 2.5 & 3.0Gb SDRAM

OSCILLOSCOPE
Design file: UT700_DIR_CONN_MATILDA_BOARD_FILES_S_PARM_MODEL.FFS
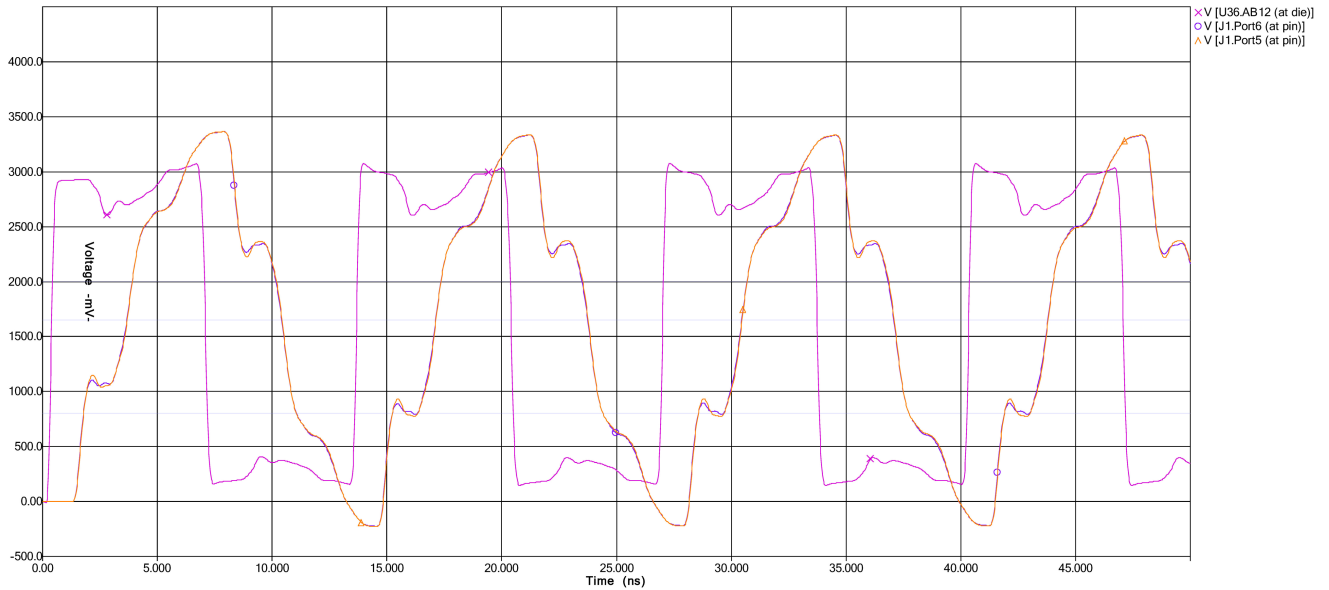Designer: Leslie, Mike (SSA)
HyperLynx v9.4.1

Figure 10: 75MHz simulation LEON SDCLK output (red) SDRAM SDCLK input at die (1&5)
Date: Friday Feb. 1, 2019 Time: 15:25:05
Net name: N22381158
Show Latest Waveform = YES, Show Previous Waveform = YES

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OSCILLOSCOPE
Design file: UT700_DIR_CONN_MATILDA_BOARD_FILES_S_PARM_MODEL.FFS
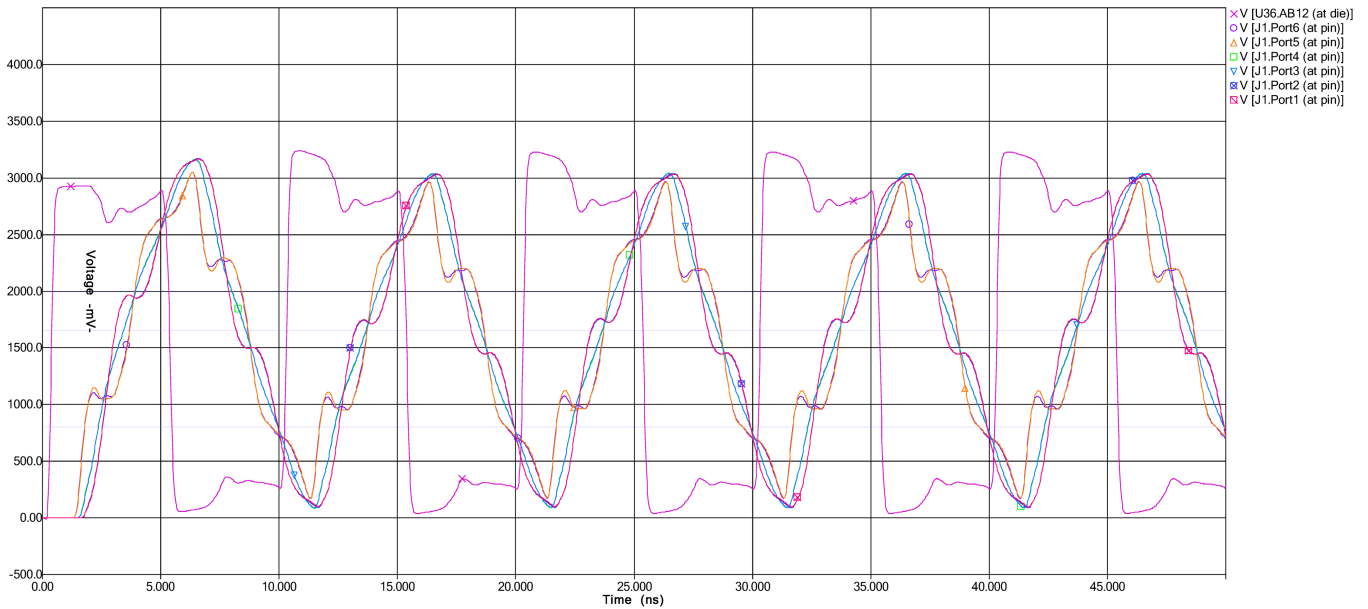Designer: Leslie, Mike (SSA)
HyperLynx v9.4.1

Figure 11: 75MHz simulation LEON SDCLK output (red) SDRAM SDCLK input at die (3&6)
Date: Friday Feb. 1, 2019 Time: 15:27:44
Net name: N22381158
Show Latest Waveform = YES, Show Previous Waveform = YES

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OSCILLOSCOPE
Design file: UT700_DIR_CONN_MATILDA_BOARD_FILES_S_PARM_MODEL.FFS
Designer: Leslie, Mike (SSA)
HyperLynx v9.4.1

Figure 12: 75MHz simulation LEON SDCLK output (red) SDRAM SDCLK input at die (2&4)
Date: Friday Feb. 1, 2019 Time: 15:29:08
Net name: N22381158
Show Latest Waveform = YES, Show Previous Waveform = YES

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OSCILLOSCOPE
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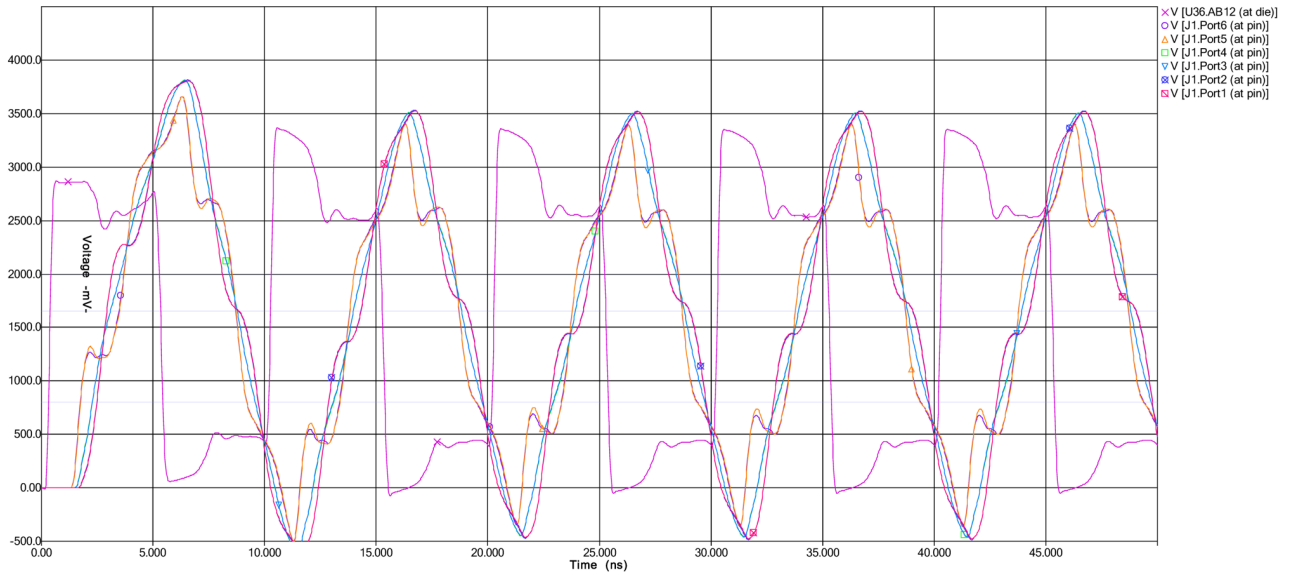Designer: Leslie, Mike (SSA)
HyperLynx v9.4.1

Figure 13: 100 MHz Simulation LEON SDCLK output (red) SDRAM SDCLK input at die (1-6) R105 = 22 ohms
Date: Friday Feb. 1, 2019 Time: 15:38:33
Net name: N22381158
Show Latest Waveform = YES, Show Previous Waveform = YES

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OSCILLOSCOPE
Design file: UT700_DIR_CONN_MATILDA_BOARD_FILES_S_PARM_MODEL.FFS
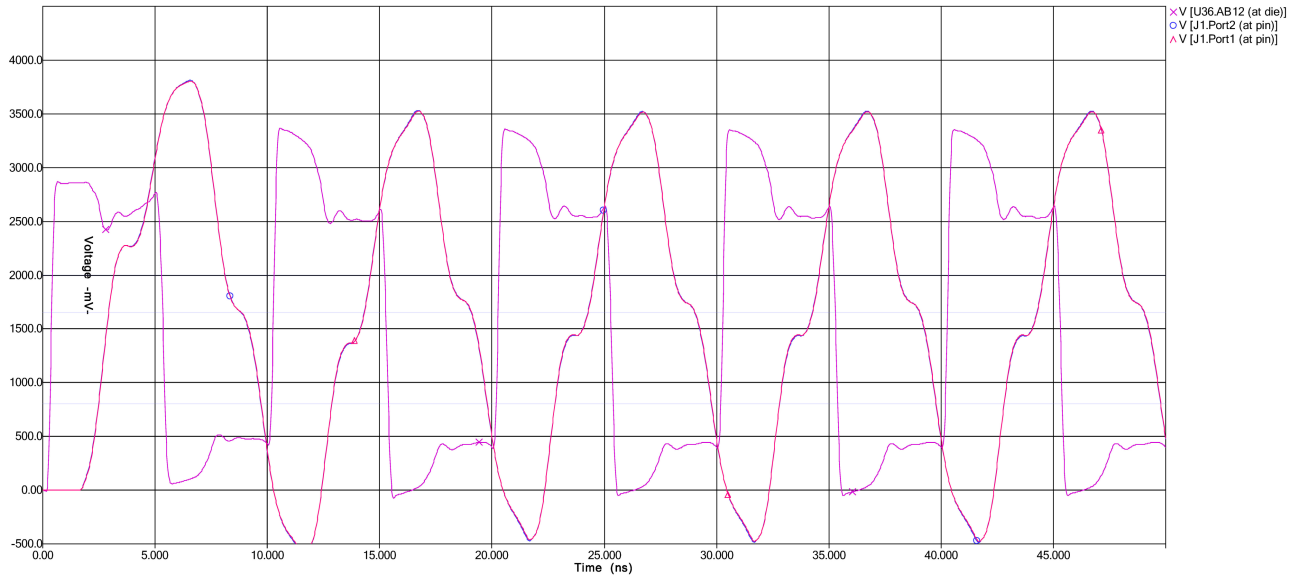Designer: Leslie, Mike (SSA)
HyperLynx v9.4.1

Figure 14: 100 MHz Simulation LEON SDCLK output (red) SDRAM SDCLK input at die (1-6) R105 = 10 ohms
Date: Friday Feb. 1, 2019 Time: 15:40:22
Net name: N22381158
Show Latest Waveform = YES, Show Previous Waveform = YES

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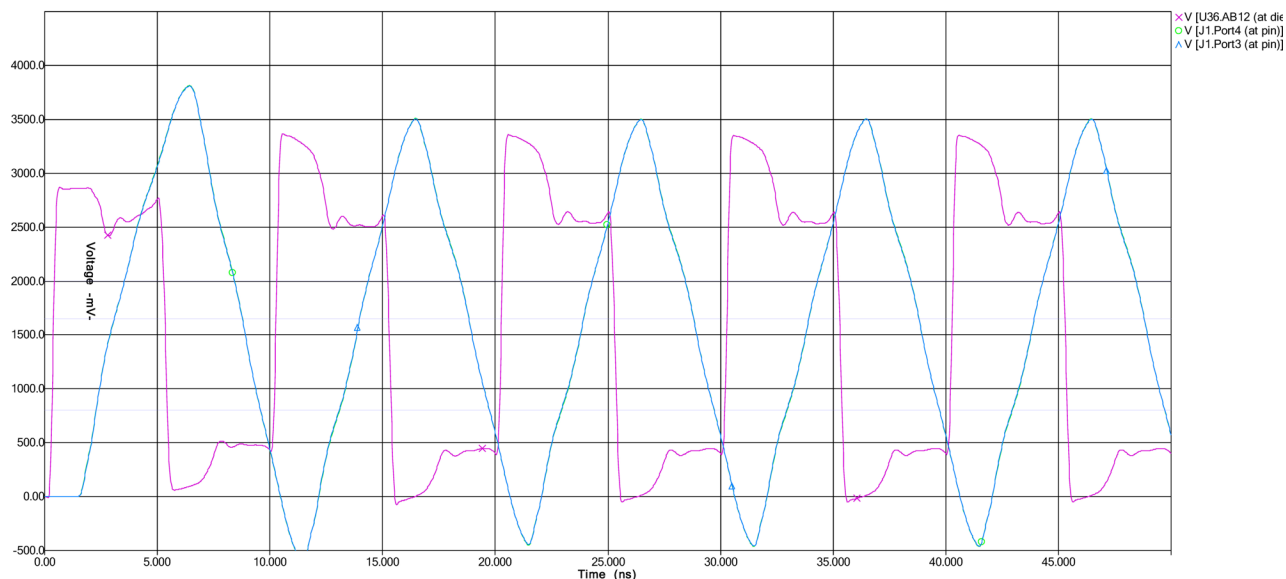Designer: Leslie, Mike (SSA)
HyperLynx v9.4.1

Figure 15: 100 MHz Simulation LEON SDCLK output (red) SDRAM SDCLK input at die (1&5) R105 = 10 ohms
Date: Friday Feb. 1, 2019 Time: 15:42:31
Net name: N22381158
Show Latest Waveform = YES, Show Previous Waveform = YES

SDRAM to UT700 LEON 3FT Timing & Signal Integrity Analysis UT8SDMQ64M40/48 2.5 & 3.0Gb SDRAM

OSCILLOSCOPE
Design file: UT700_DIR_CONN_MATILDA_BOARD_FILES_S_PARM_MODEL.FFS
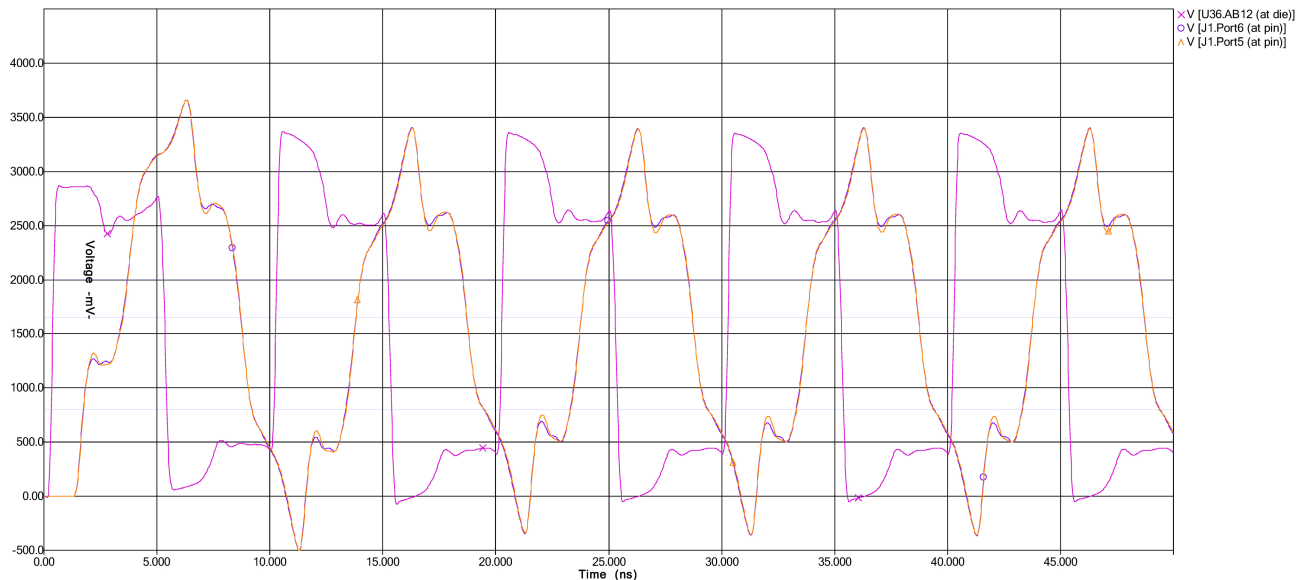Designer: Leslie, Mike (SSA)
HyperLynx v9.4.1

Figure 16: 100 MHz Simulation LEON SDCLK output (red) SDRAM SDCLK input at die (3&6) R105 = 10 ohms
Date: Friday Feb. 1, 2019 Time: 15:55:05
Net name: N22381158
Show Latest Waveform = YES, Show Previous Waveform = YES

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OSCILLOSCOPE
Design file: UT700_DIR_CONN_MATILDA_BOARD_FILES_S_PARM_MODEL.FFS
Designer: Leslie, Mike (SSA)
HyperLynx v9.4.1Date

Figure 17: 100 MHz Simulation LEON SDCLK output (red) SDRAM SDCLK input at die (2&4) R105 = 10 ohms
Date: Friday Feb. 1, 2019 Time: 15:56:30
Net name: N22381158
Show Latest Waveform = YES, Show Previous Waveform = YES

6.0 Matilda evaluation board SDRAM signals physical measurements

Physical signal measurements were performed using CAES' internal UT700 Matilda evaluation board which features the UT700 LEON microprocessor, UT7R955 RadClock, and UT8SMDQ64M48 SDRAM. As noted earlier, the RadClock was physically bypassed using approximately a 0.33inch 30 gauge wire to jumper XTAL1 directly to 1Q0 (reference Figure 12). The RadClock pin to 1Q0 was lifted while the input pin XTAL1 was also lifted and pulled low. An unlidded functional SDRAM device was mounted onto the evaluation board in order to evaluate the signal integrity and timing directly at the active SDRAM's die pads. Two low capacitance (0.1pF) active 12C PicoProbes were used to acquire measurements without significantly altering the circuit. Since the SDRAM module makes use of a dual cavity package, only the three top cavity die were accessible to probe. In previous evaluations, it is known that the signal integrity is worst case at die number two which is closest path to the package pin and results in more prominent reflections. A Teledyne LeCroy WaveRunner 625Zi 40Gs/sec sample rate oscilloscope was used which is capable of 25ps resolution.

The oscilloscope measurements presented hereafter are intended for the purposes evaluating typical interconnect timing and signal integrity. The timing of all relevant SDRAM signals was captured for both setup and hold times during applicable SDRAM read or write operations. Measurements were taken at 75MHz with series resistor R109 = 22 ohms (this correlates to R105 for simulations) and again at 100MHz with R109 = 10 ohms. It was verified that flight time due to the various daisy chain paths was negligible. Note that all clock signals at the die are completely monotonic with only a small reflection observed on die 2 suspected to be worst case. All measurements are taken with respect to die 2 considered to be worst case for signal integrity. The timing captured varies significantly from the specifications as these measurements are typical device functionality and measurements are made at approximately

50% signal swing or VDD/2 which is closer to the actual device input switching threshold. Characterization data shows that VIL typical is 1.12V and VIH is 1.48V. The minimum VIL worst case −40C and VDD = 3.0V is 1.01V and maximum VIH at worst case was 1.69V. Specifications are set based on characterization data measurements across full temperature, voltage, and specified VIL/VIH levels as measurement points. Additionally, a 2cpk to the mean minimum margin is desired for setting specification limits. The data is compiled onto the timing diagrams of Figure 33 and 34 respectively. The SDRAM clock was offset 2.75ns which represents the approximate rise time of the clock signal to the typical input switching threshold of VDD/2.

Note: The PicoProbes do not activate the x10 input multiplier of scope even though they are 10x probes. Therefore the voltage scale needs multiplied by a factor of 10 (i.e. 330mV = 3.3V).

6.1 Physical measurements results at 75MHz

Figure 18: Matilda evaluation board SDRAM circuit schematic.

Figure 19: 25MHz system clock used to calibrate both PicoProbes prior to measurements.

Figure 20: LEON SDRAM clock output measurement at series resistor R109 and clock input pin of the SDRAM. Note the reflections are far less than that of the simulations.

Figure 21: Clock signal measurement at pads of die 1 and die 2 as shown in Figure 5. This represents the best and worst case clock signals at the die pads. While the reflections of the simulations at the die pads are noticeable, they are not evident on the physical measurements. The resolution of the scope and the sample rate is sufficient to capture a minimum of 25ps. This is evident in the following captures where small signal ripples and disturbances are faster than the expected clock reflection.

Note that there is a little disturbance on die 2, but timing is simultaneous throughout the expected input switching threshold of 1.0V − 1.7V based on worst case tri-temperature and full operating voltage characterization. Therefore, it is reasonable to conclude that timing at die 2 is applicable to all SDRAM die.

Figure 22: LEON output of A(0) at die 2. Measures tAS and tAH requirements of the SDRAM. The capture is a measurement of the setup time. Hold time was measured using cursors. Hold time captures generally not shown in the interest of brevity.

Figure 23: LEON output of SDCS0 at die 2. This correlates to tCMS and tCMH with respect to the SDRAM specification for setup and hold time of the /CS.

Figure 24: LEON output of SDCAS at die 2. This correlates to tCMS and tCMH with respect to the SDRAM specification for setup and hold time of the /RAS, /CAS and /WE. Separate measurements of all three indicated there was no appreciable difference in timing between the three.

Figure 25: Data input to SDRAM during a LEON SDRAM write command. This correlates to SDRAM parameters tDS and tDH. Only rising data could be captured as evaluation write command was single word and data returns low.

Figure 26: Data output of SDRAM during a LEON SDRAM read command. This correlates to the SDRAM parameters tAC (data out access time) and tOH (data out hold time). From the LEON receiving data perspective, it correlates to LEON parameters t5a (data setup time) and t6a (data hold time) The 2.75ns skew due to SDRAM rise time is applicable to these parameters.

6.2 Physical measurement results at 100MHz

Figure 27: 25MHz system clock used to calibrate both PicoProbes prior to measurements.

Figure 28: LEON output of A(0) at die 2 which is tAS and tAH requirements of the SDRAM . The signal is a measurement of the setup time. Hold time was measured using cursors but not shown in the interest of brevity.

Figure 29: LEON output of SDCS0 at die 2. This correlates to tCMS and tCMH with respect to the SDRAM specification for setup and hold time of the /CS.

Figure 30: LEON output of SDCAS at die 2. This correlates to tCMS and tCMH with respect to the SDRAM specification for setup and hold time of the /RAS, CAS and /WE. Separate measurements of all three indicated there was no appreciable difference in timing between the three.

Figure 31: Data input to SDRAM during a LEON SDRAM write command. This correlates to SDRAM parameters tDS and tDH. Only rising data could be captured as evaluation write command was single word and data returns low.

Figure 32: Data output of SDRAM during a LEON SDRAM read command. This correlates to the SDRAM parameters tAC (data out access time) and tOH (data out hold time). From the LEON receiving data perspective, it correlates to LEON parameters t5a (data setup time) and t6a (data hold time) The 2.75ns skew due to SDRAM rise time is applicable to these parameters.

Jumper wire installed to bypass RadClock
Pin 31 lifted and R105replaced with 0ohm resistor
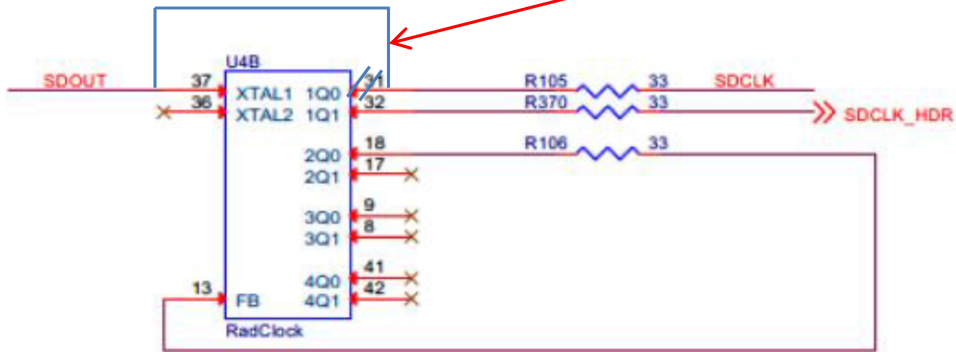
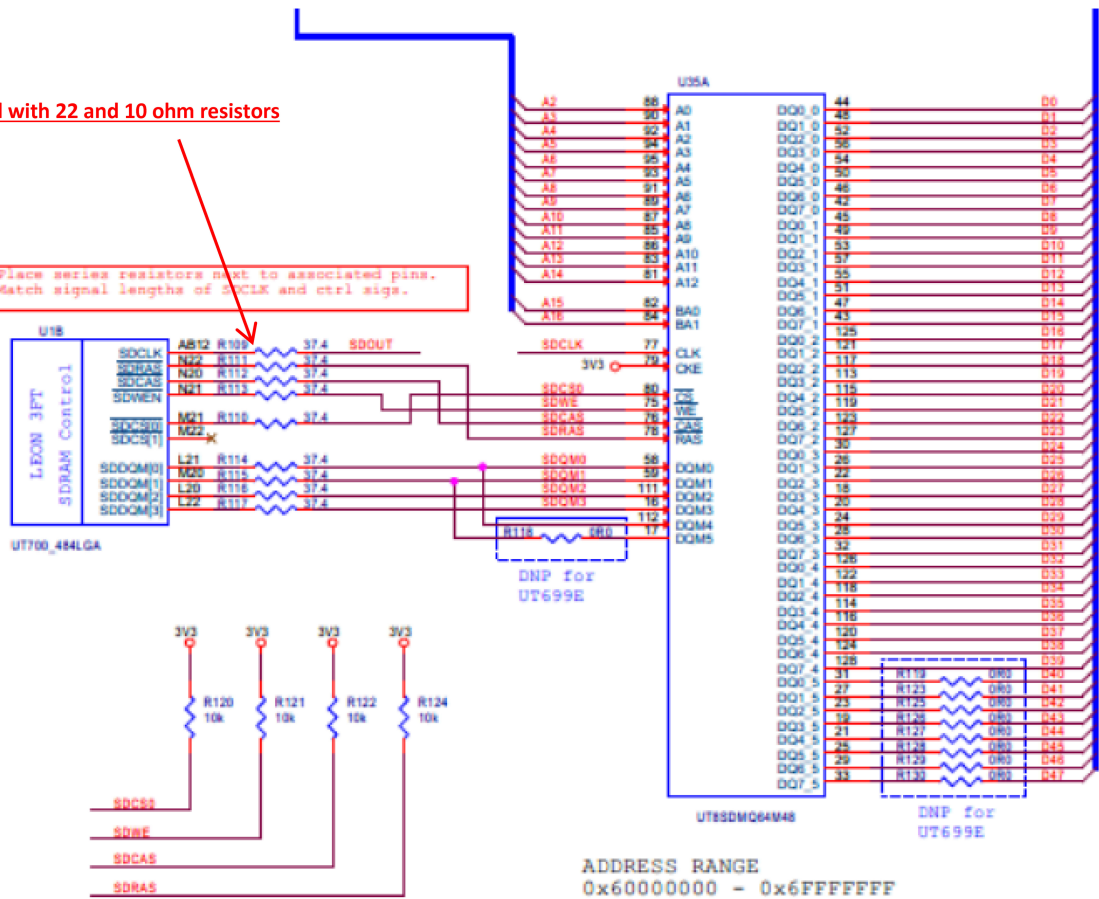**R109 replaced with 22 and 10 ohm resistors**

Figure 18: Matilda evaluation board SDRAM schematic

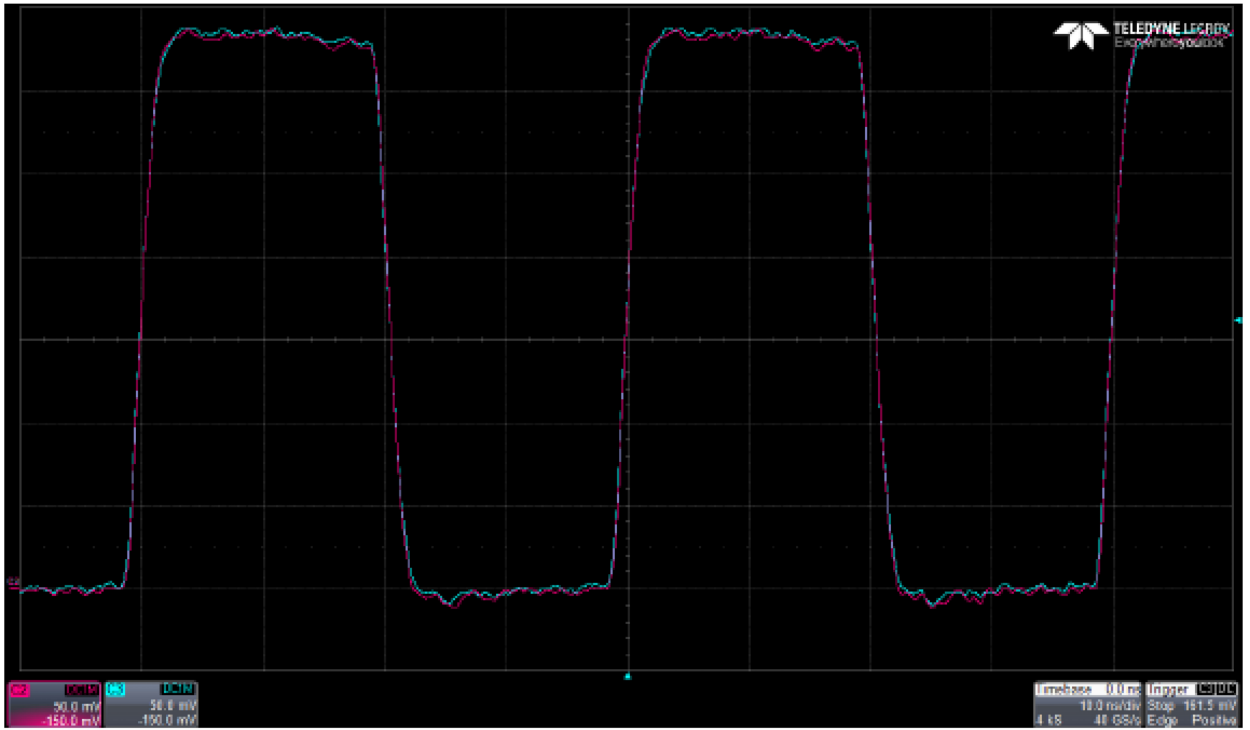# SDRAM to UT700 LEON 3FT Timing & Signal Integrity Analysis UT8SDMQ64M40/48 2.5 & 3.0Gb SDRAM

Figure 19: Pre-measurement scope probe calibration using 25MHz system clock
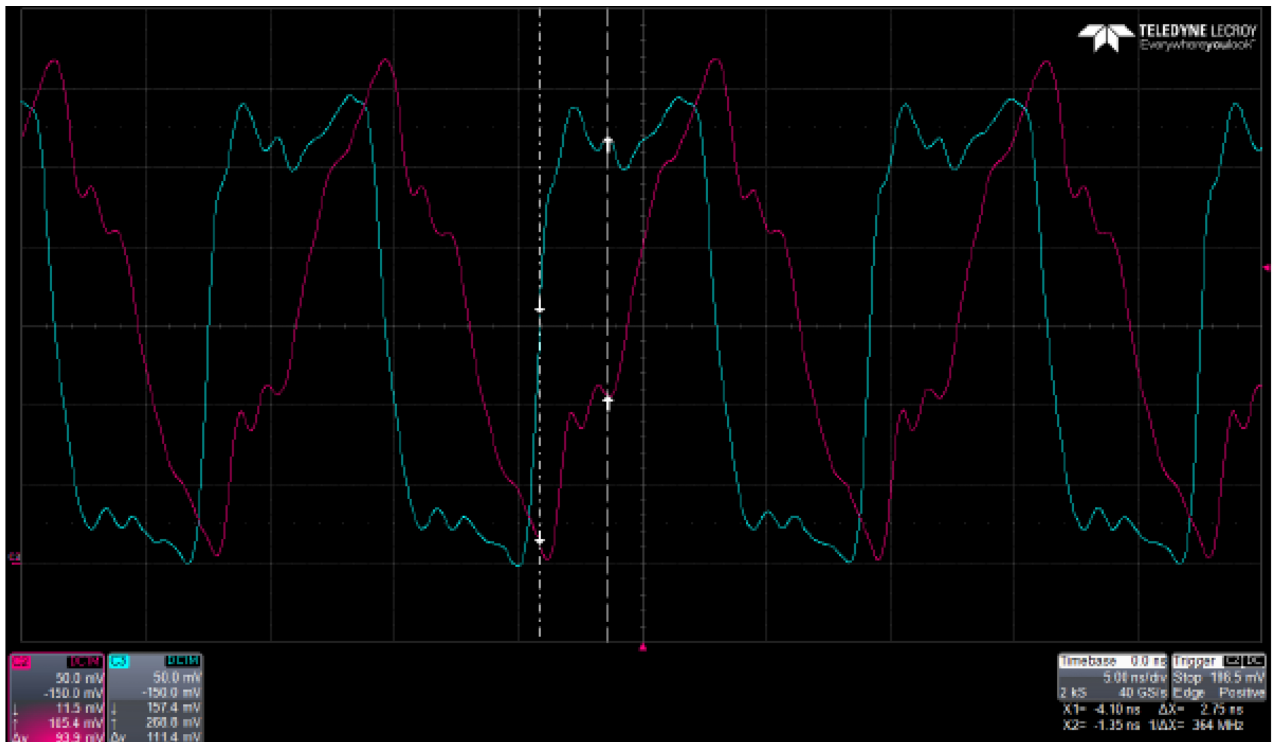
Note: Resolution available as seen by signal ringing

Figure 20: 75MHz CH2 SDRAM SDCLK pin at LEON side of R109,
CH3 SDCLK at SDRAM input pin; 2.75ns delay at 50%

SDRAM to UT700 LEON 3FT Timing & Signal Integrity Analysis UT8SDMQ64M40/48 2.5 & 3.0Gb SDRAM
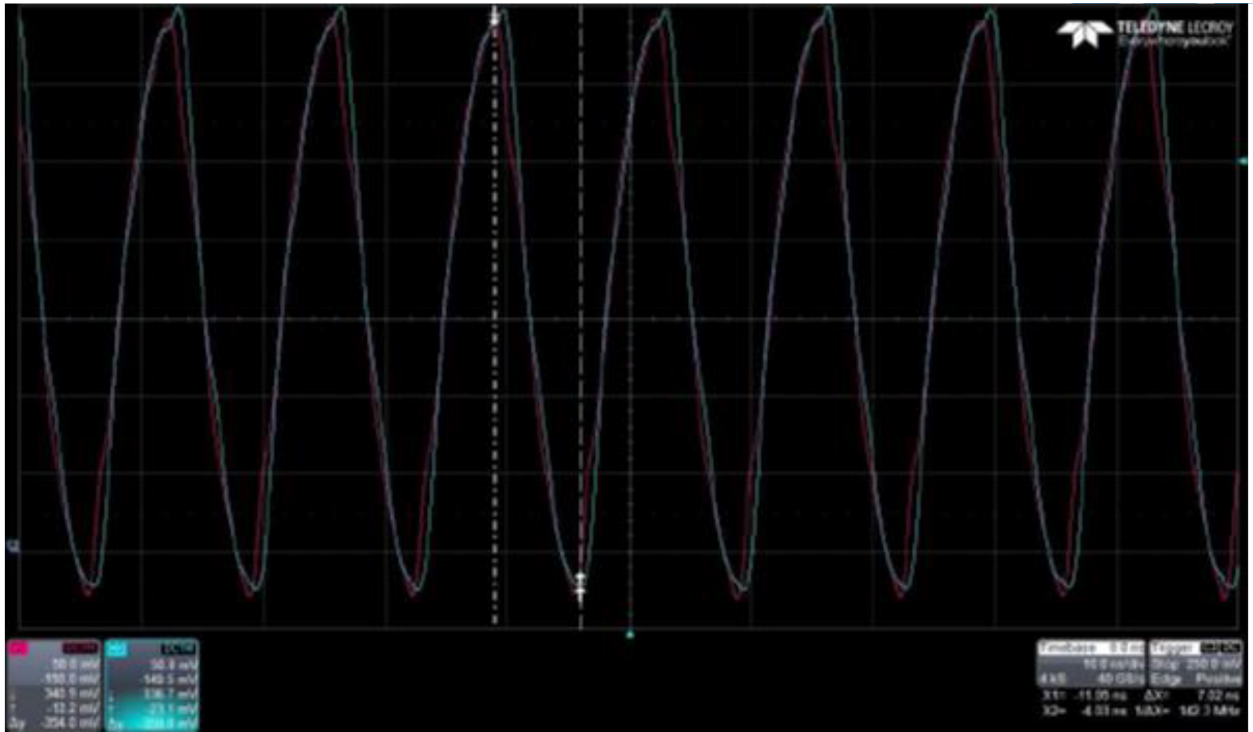
Figure 21: 75MHz CH2 CLK pad at die 2; CH3 CLK pad at die 1

Note: Die 2 results in small reflection and is worst case.
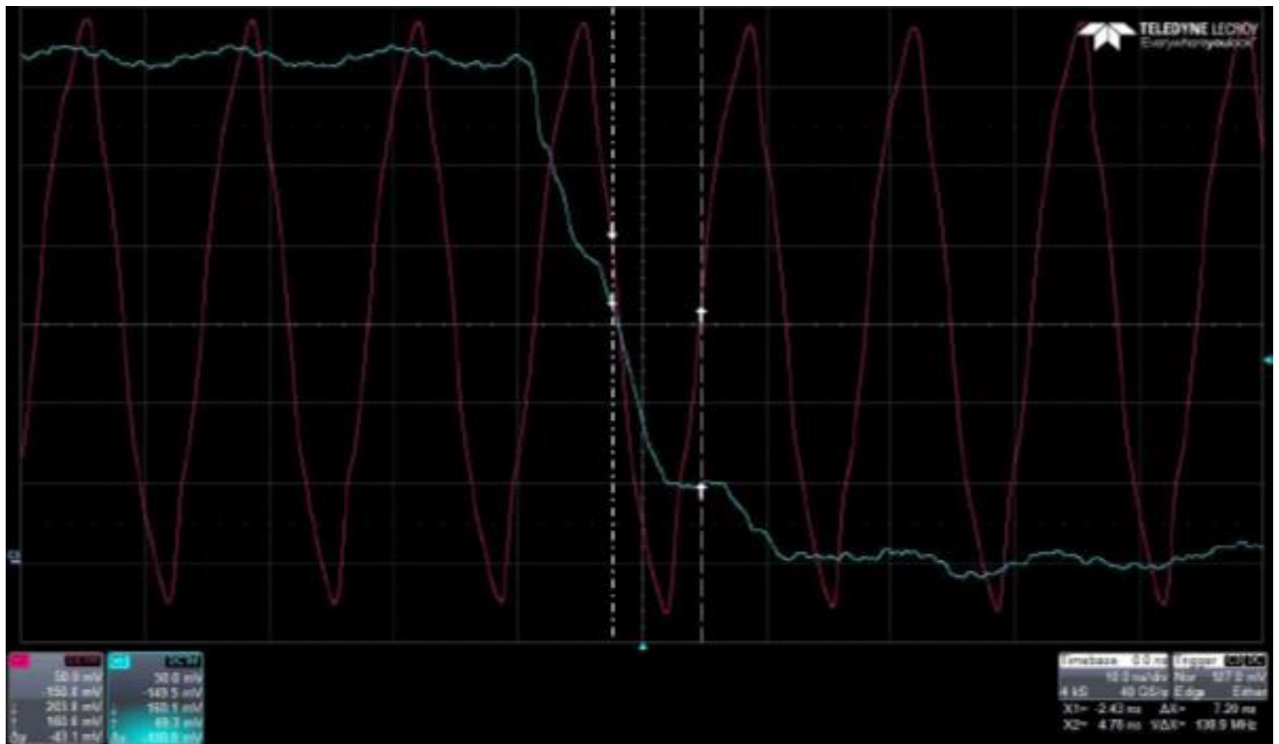
Figure 22: 75MHz CH2 die 2 CLK pad; CH3 die 2 ADDR(A0)
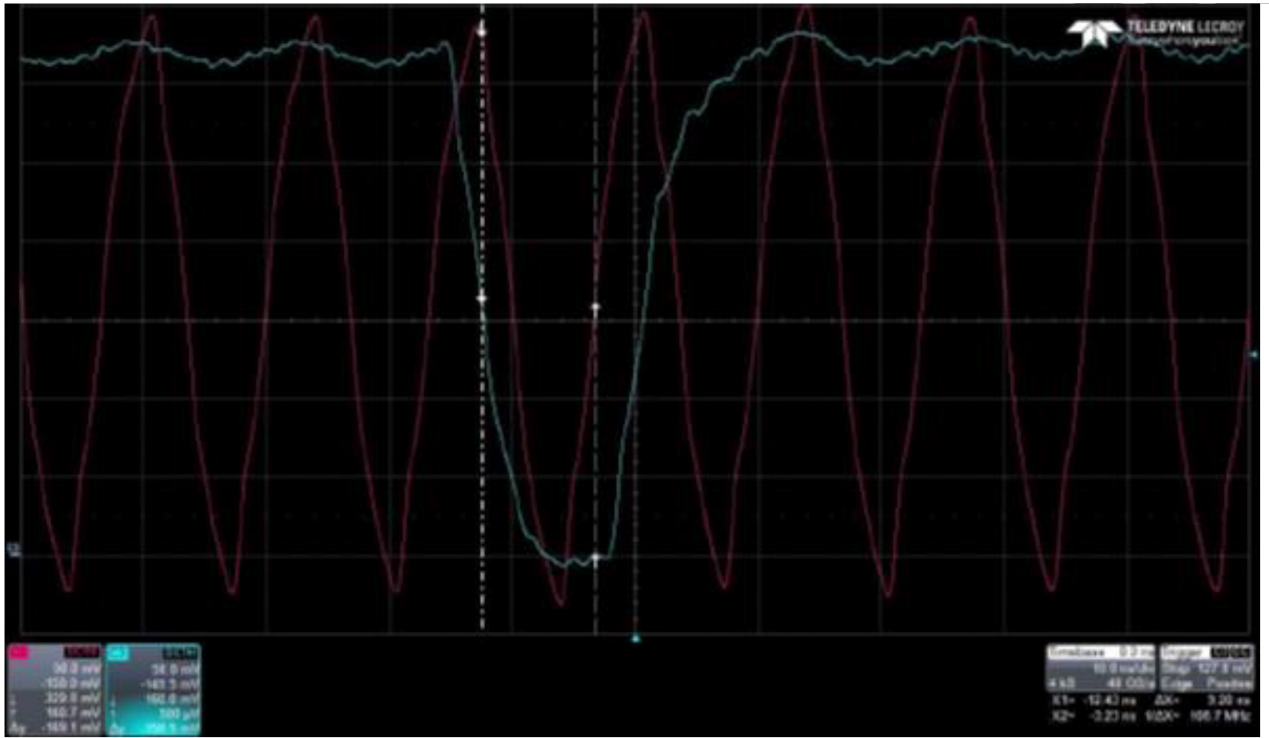tAS address setup time = 7.2ns; tAH address hold time = 6.13ns

Figure 23: 75MHz CH2 die 2 CLK pad; CH3 SDCS0
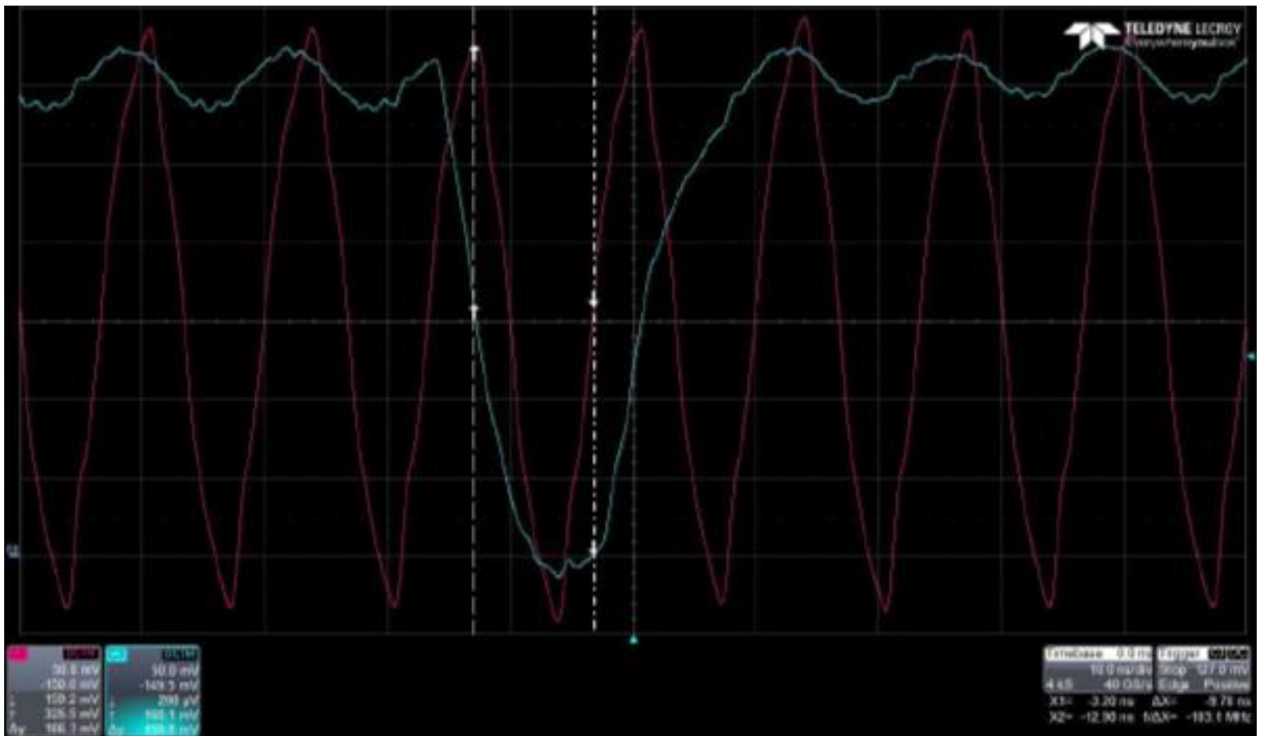tCMS /CS setup time = 9.2ns; tCMH /CS hold time = 4.1ns

Figure 24: 75MHz CH2 die 2 CLK pad; CH3 die 2 SDCAS
tCMS /CAS setup time = 9.7ns; tCMH CAS hold time = 4.1ns
Evaluation of /RAS and /WE have the same signal timing as /CAS

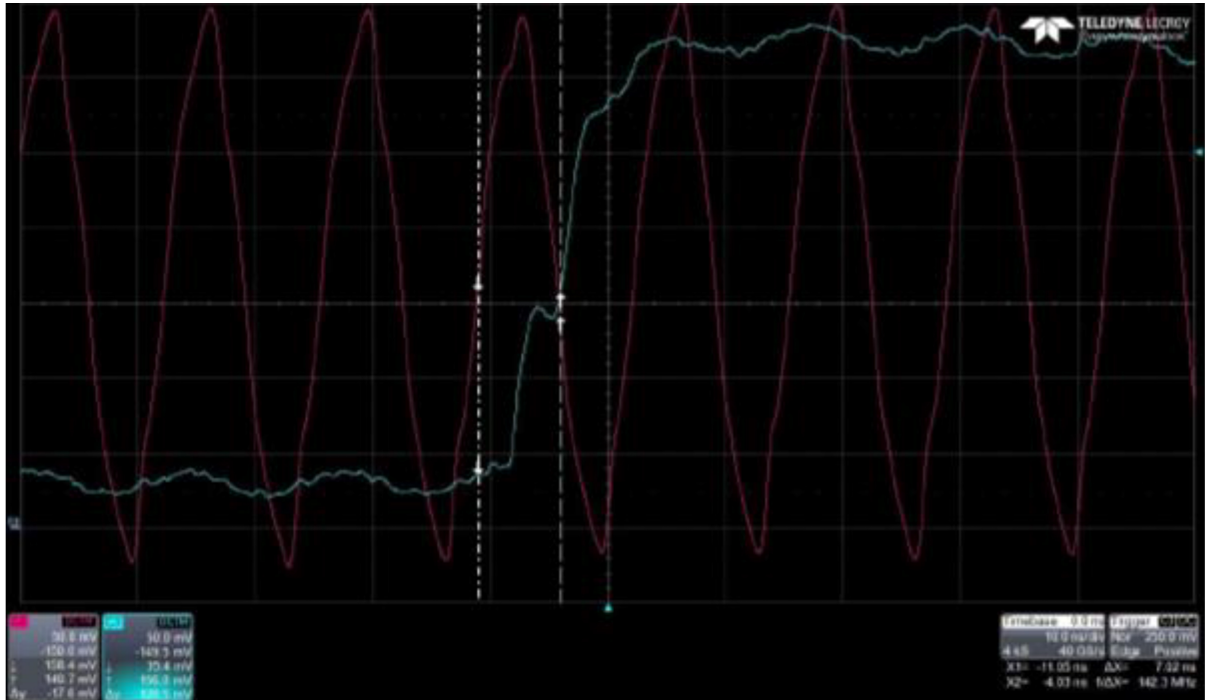# SDRAM to UT700 LEON 3FT Timing & Signal Integrity Analysis UT8SDMQ64M40/48 2.5 & 3.0Gb SDRAM

Figure 25: 75MHz CH2 die 2 CLK pad; CH3 die 2 DQ3
LEON write command to SDRAM
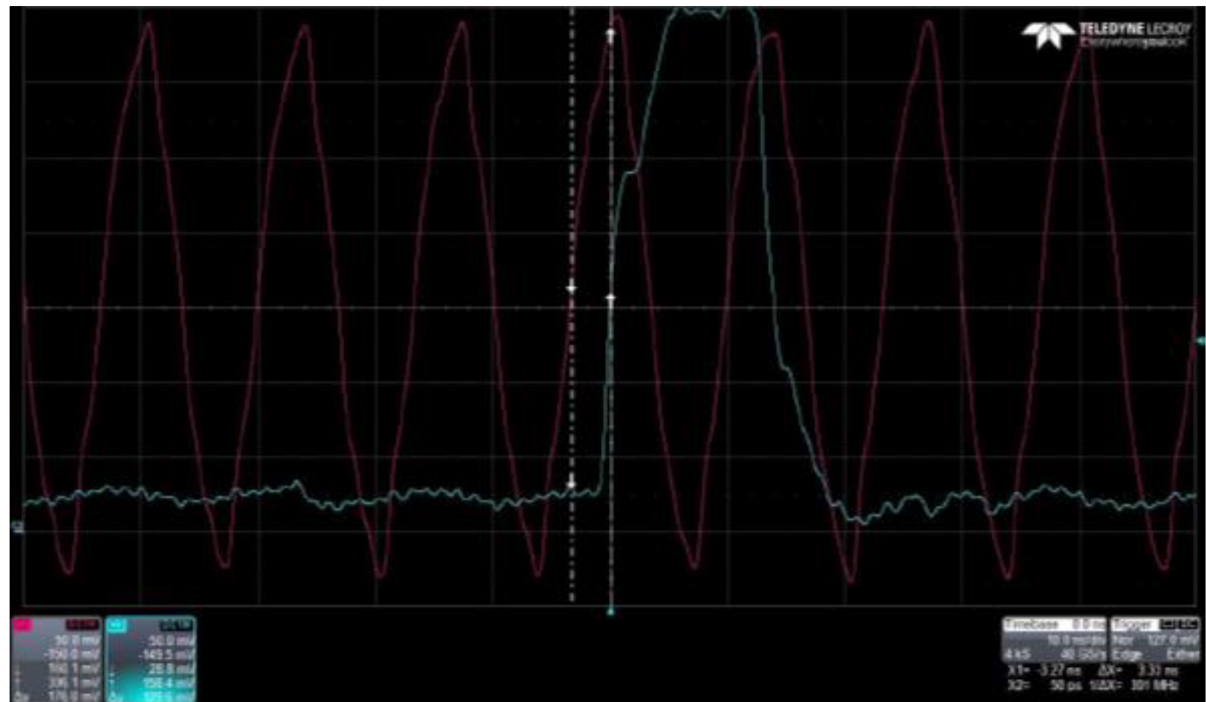tDS = data setup time = 6.3ns, tDH data hold time = 7.0n

Figure 26: 75MHz CH2 die 2 CLK pad; CH3 die 2 DQ3
LEON read command from SDRAM
LEON t5a = data setup time = 9.43 − 2.75 = 6.68ns,
t6a data hold time = 3.3 + 2.75ns = 6.05ns

Figure 27: Pre-measurement scope probe calibration using 25MHz system clock
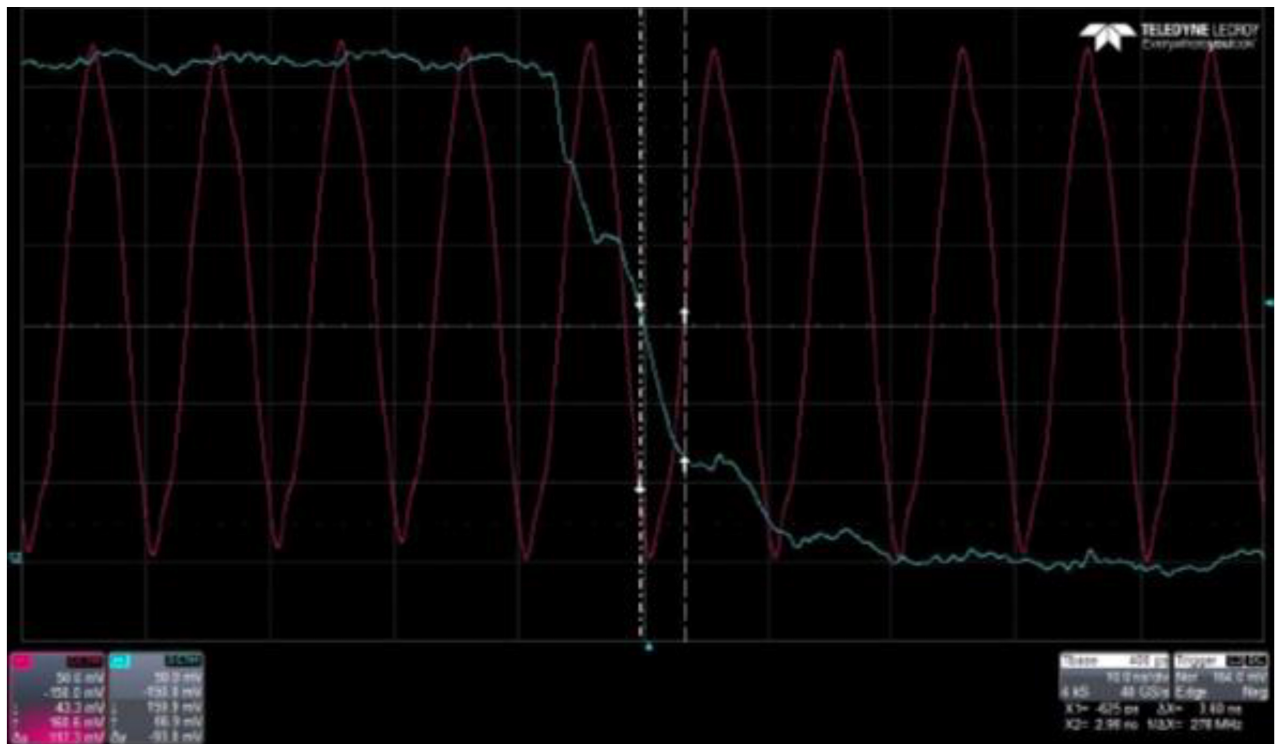
Note: Resolution available as seen by signal ringing

Figure 28: 100MHz CH2 CLK pad at die 2; CH3 ADDR (A0) pad at die 2
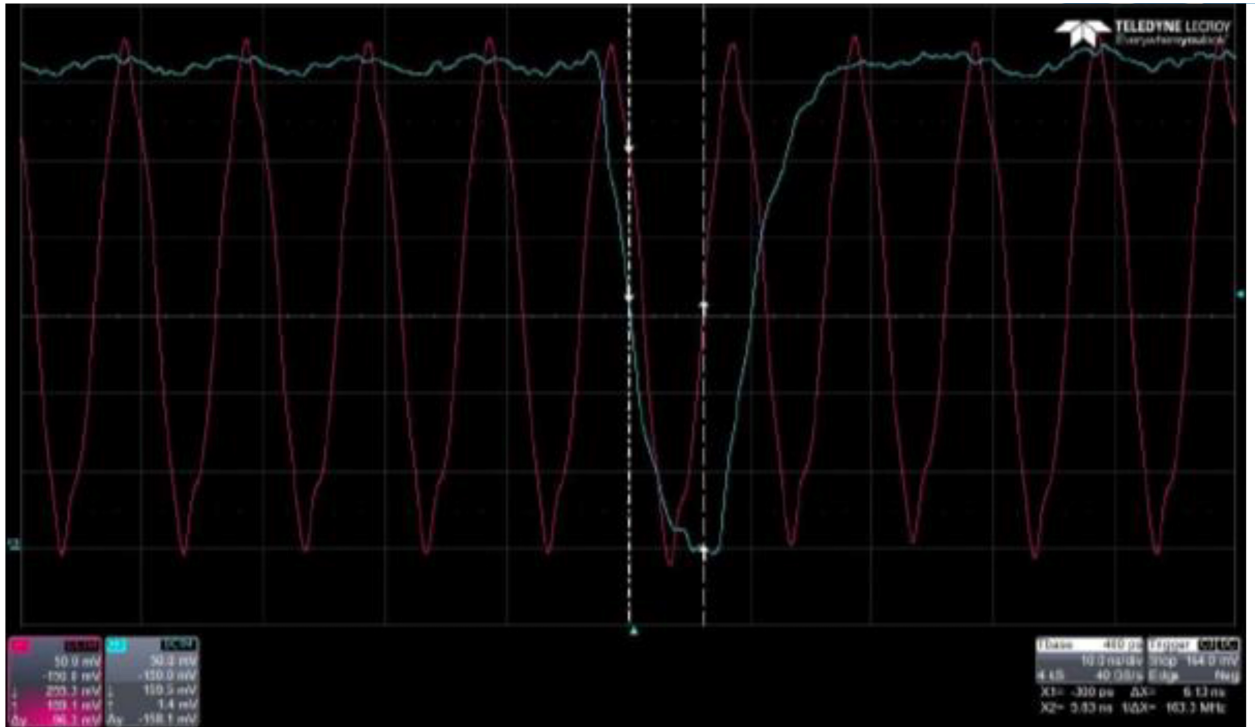tAS = 3.6ns, tAH = 6.4ns @ 50% signal levels 1.6V

Figure 29: 100MHz CH2 die 2 CLK pad; CH3 SDCS0
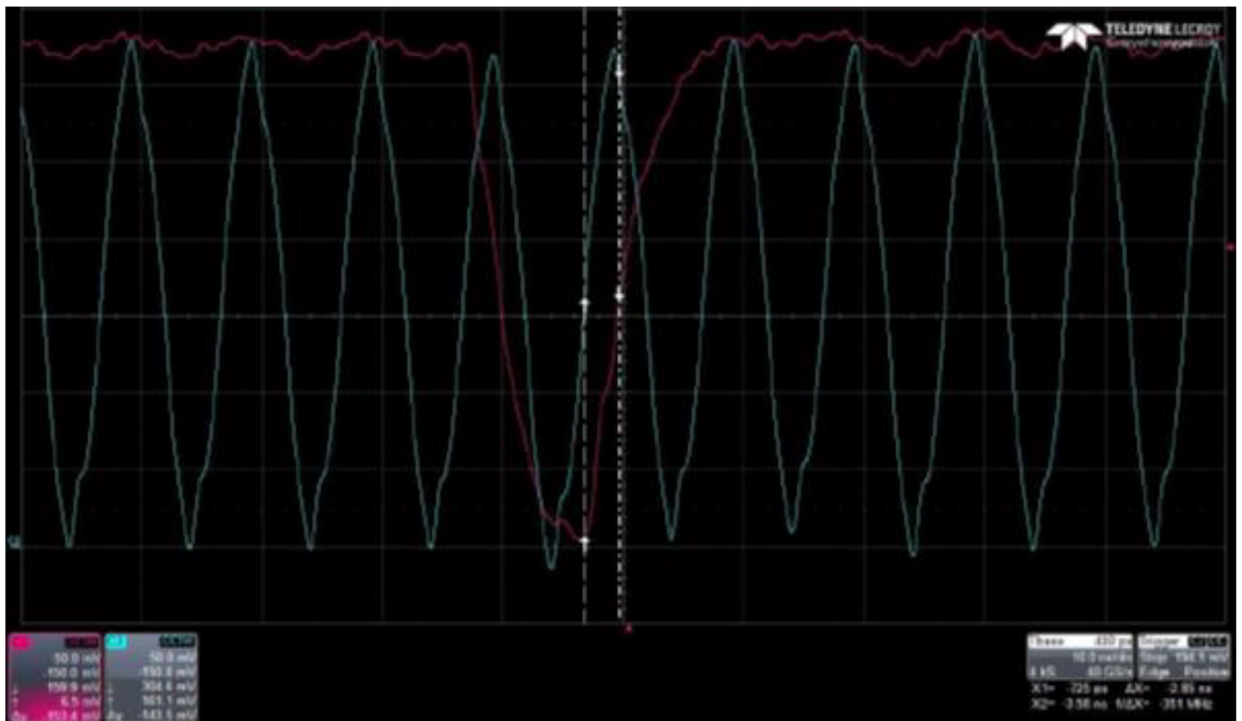tCMS /CS setup time = 6.13ns; tCMH /CS hold time = 4.08ns

Figure 30: CH2 die 2 CLK pad; CH3 die 2 SDCAS
tCMS /CAS setup time = 7.0ns; tCMH CAS hold time = 2.85ns
Evaluation of /RAS and /WE have the same approximate timing as /CAS

SDRAM to UT700 LEON 3FT Timing & Signal Integrity Analysis UT8SDMQ64M40/48 2.5 & 3.0Gb SDRAM
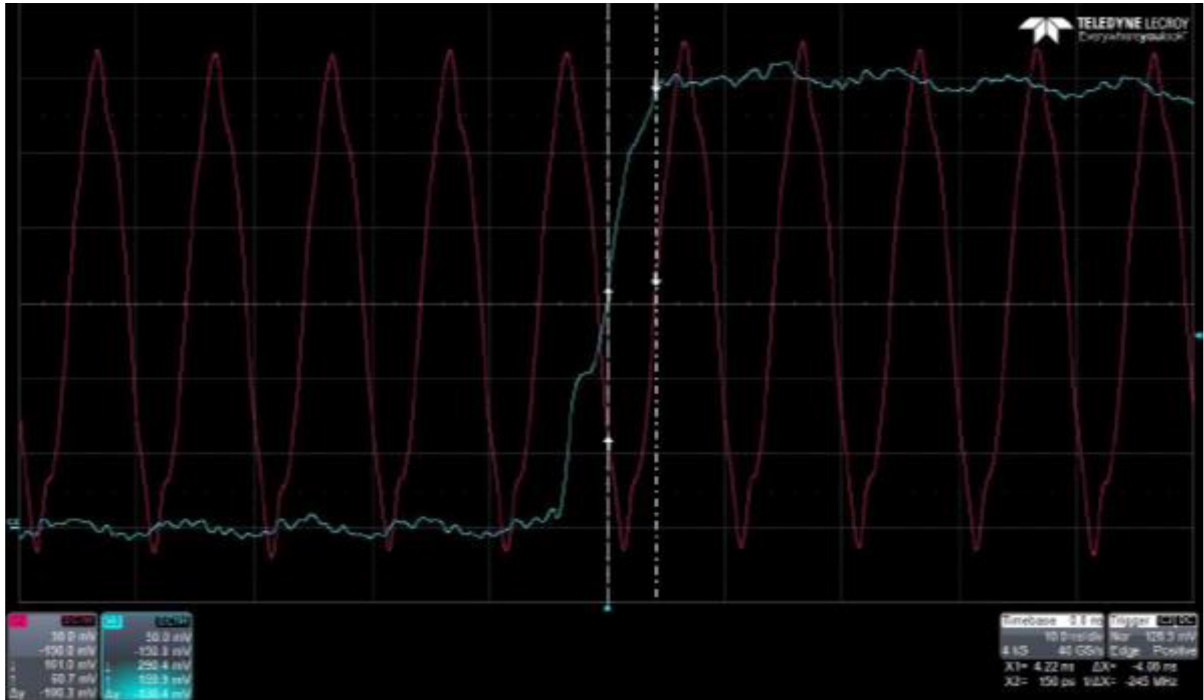

Figure 31: CH2 die 2 CLK pad; CH3 die 2 DQ7
LEON write command to SDRAM
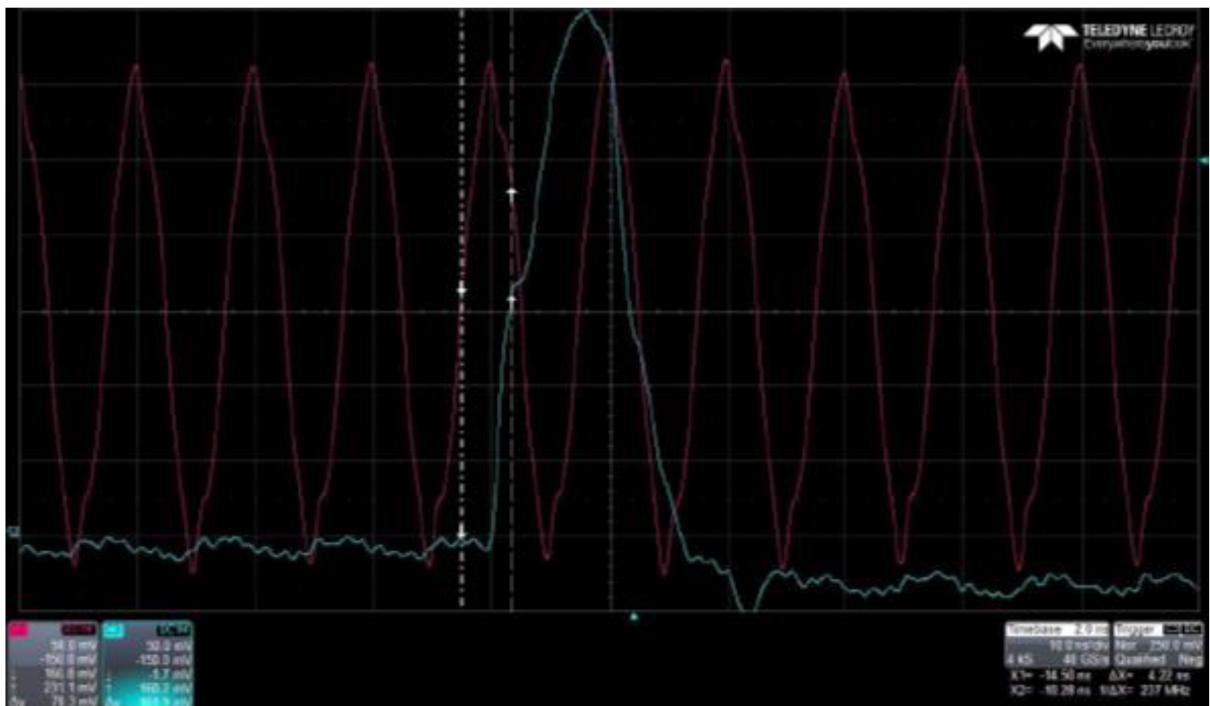tDS = data setup time = 5.85ns, tDH data hold time = 4.08ns

Figure 32: CH2 die 2 CLK pad; CH3 die 2 DQ7
LEON read command from SDRAM
LEON t5a = data setup time = 5.6 − 2.75 = 2.85ns,
t6a data hold time = 3.22 + 2.75ns = 5.97ns

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Figure 33: 75MHz Matilda evaluation board timing analysis Rs = 22ohms
Datasheet parameters are given in (parenthesis)

*Note: The shortest hold time results when switching data 0 to 1 of 3.3ns which results in the longest setup time of 10ns. The longest hold time results when switching data from 1 to 0 of 3.9ns which results in the shortest setup time of 9.43ns. For the timing diagram both worst cases are applied.

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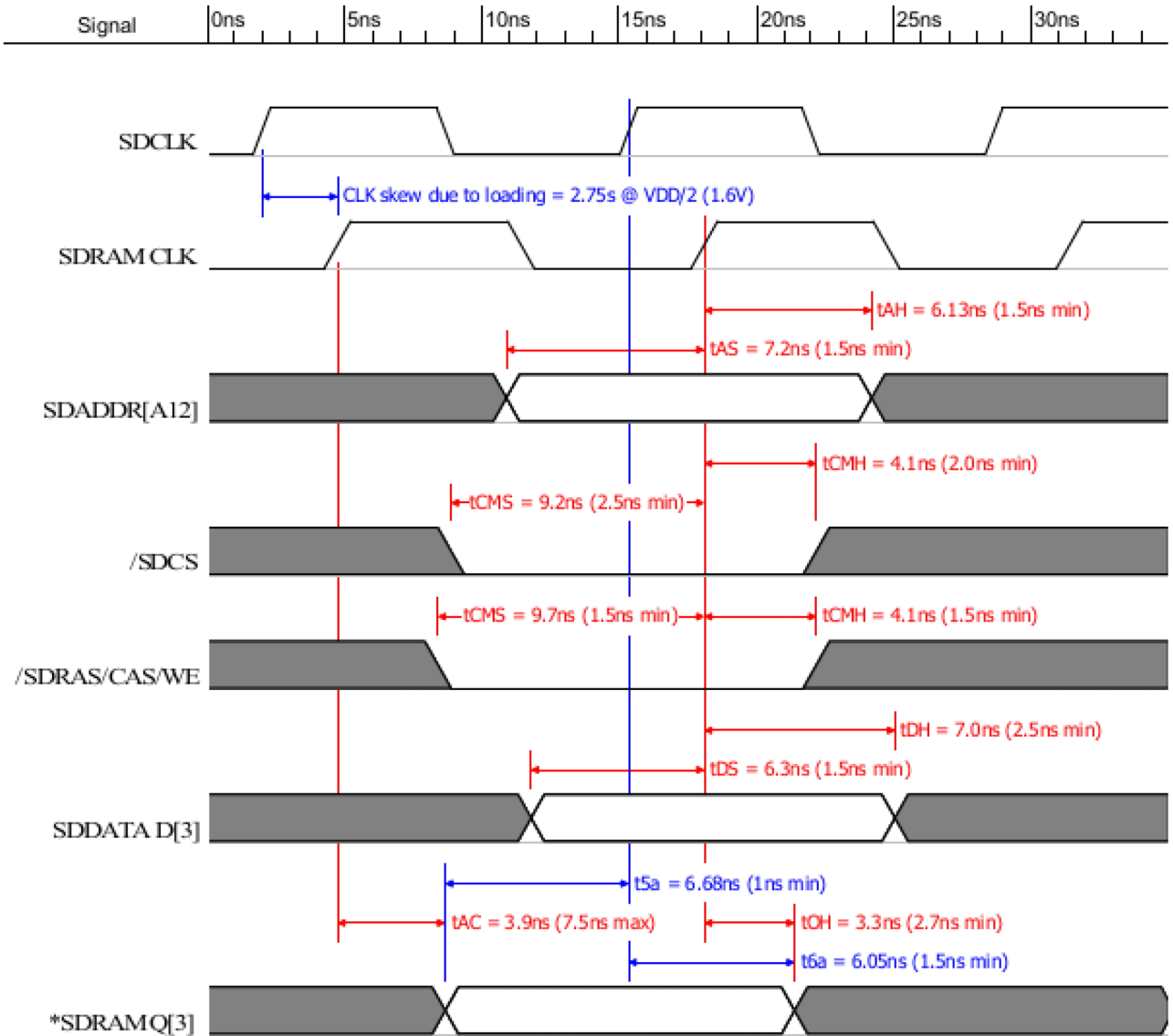# SDRAM to UT700 LEON 3FT Timing & Signal Integrity Analysis UT8SDMQ64M40/48 2.5 & 3.0Gb SDRAM
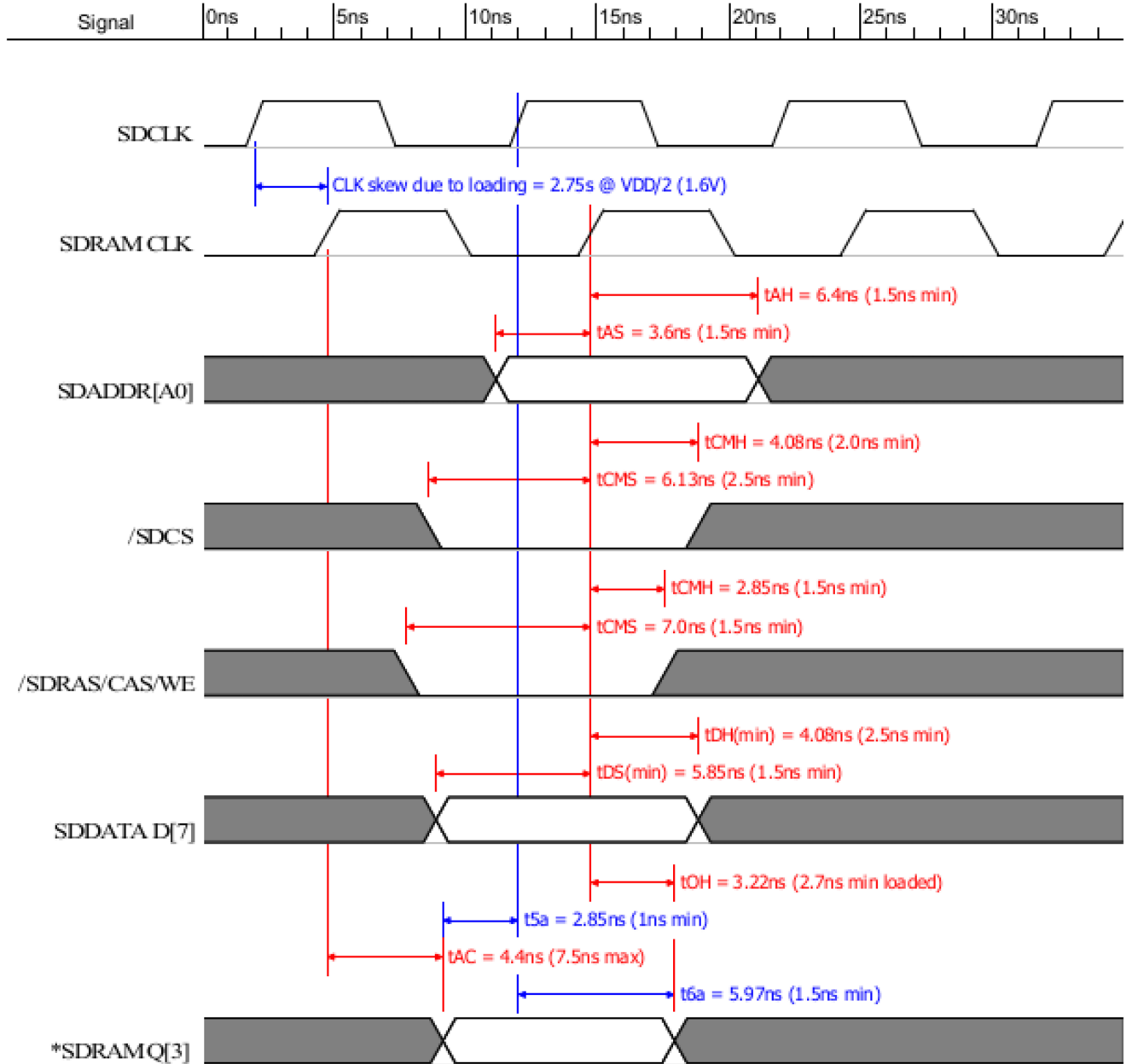
Figure 34: 100MHz Matilda evaluation board timing analysis Rs = 10ohms
Datasheet parameters are given in (parenthesis)

*Note: The shortest hold time results when switching data 0 to 1 of 3.22ns which results in the longest setup time. The longest hold time results when switching data from 1 to 0 of 4.4ns which results in the shortest setup time of 2.85ns when accounting for the 2.75ns clock rise time. For the timing diagram both worst cases are applied.

7.0 Worst case timing analysis (WCA)

Characterization data at minimum, nominal and maximum operating temperatures and voltages as well as pre and post TID for both the SDRAM and LEON UT700 were extrapolated to estimate the worst case timing variance expected due to full operating conditions and life. These worst case shifts are then applied to the previous typical measurement (Figure 33) to determine worst case expected timing variance as a result of full operating conditions and TID. All timing parameters with the exception of when the LEON is acquiring data from the SDRAM are based off the UT700 characterization data. When the UT700 is reading data from the SDRAM, the SDRAM access timing data was used.

7.1 tAC (SDRAM data out access time)

In order to account for the variance of all 48 DQ[47:0] on all die across full operating voltage and temperature, characterization data of the 6 die SDRAM product UT8SDMQ64M48 was used. tAC data was extracted from a 42 piece SDRAM sample. The characterization test performs a search for both minimum and maximum access time of all 48 DQ[47:0] outputs at both minimum (3V) and maximum (3.6V) operating voltages.

During the testing only the minimum and maximum values captured of all 48 DQ[47:0] signals are reported. Therefore, the data represents the worst case corners across voltage and temperature of all 48 DQ[47:0]. It is not known by reviewing the reported data which individual data I/O was reported, therefore it is not known if the min at 25°C is the same data I/O reported as the min at either or both −40°C and +105°C. Regardless, the distribution of the access timing of the SDRAM as a function of temperature is relatively tight.

The mean, min and max data for each of the 42 piece sample are captured as a function of temperature for both 3.0 and 3.6V. The 3.3V typical was extrapolated (since device(s) are not tested at nominal voltage) from this data making the reasonable assumption that access time shifts linearly as a function of supply voltage.

Extrapolated SDRAM data time tAC as a function of temp

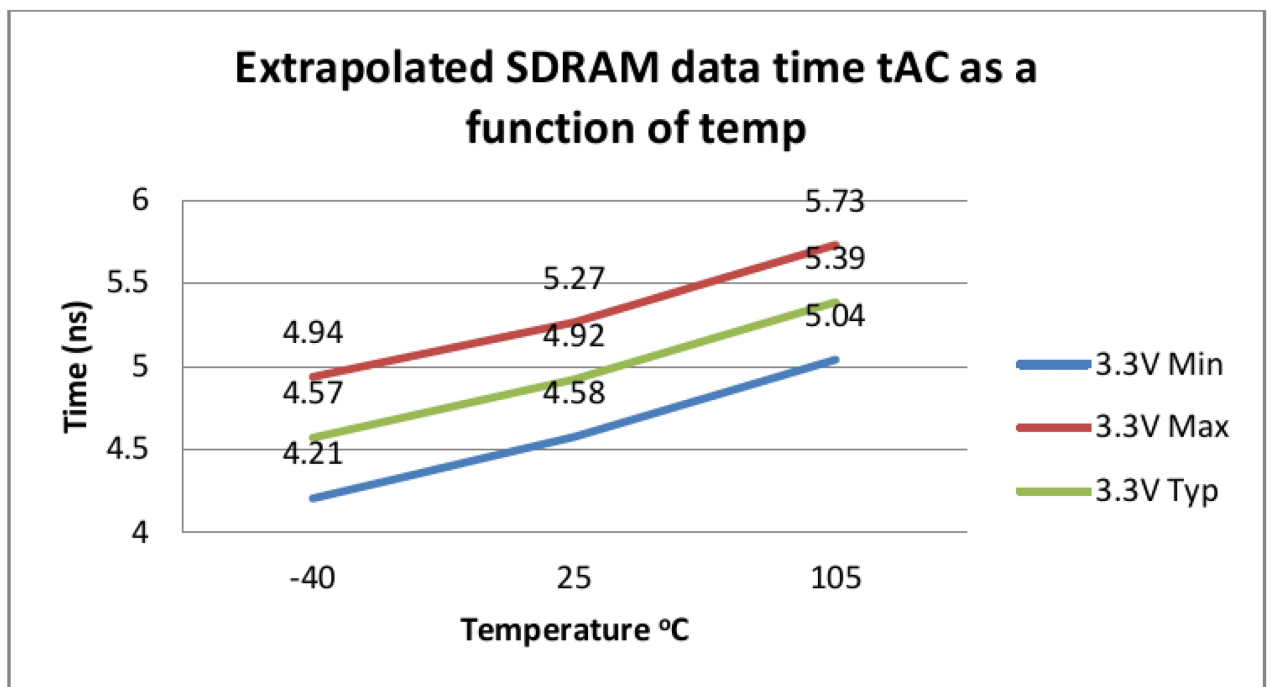# SDRAM to UT700 LEON 3FT Timing & Signal Integrity Analysis UT8SDMQ64M40/48 2.5 & 3.0Gb SDRAM
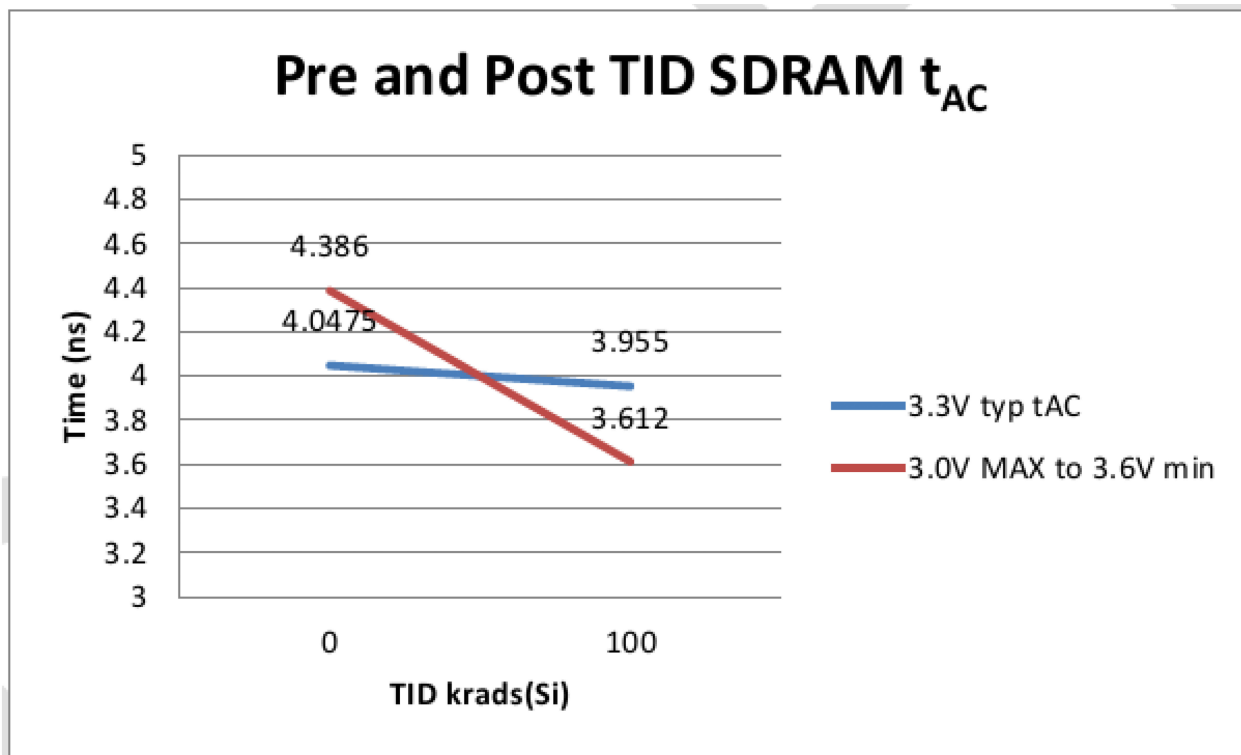
The worst case data across full voltage and temperature is plotted below. This data represents the minimum data of all the minimums and the maximum data of all the maximums. This represents the total worst case shifts of all 48 DQ[47:0] of the complete 42 piece sample across full voltage and temperature.
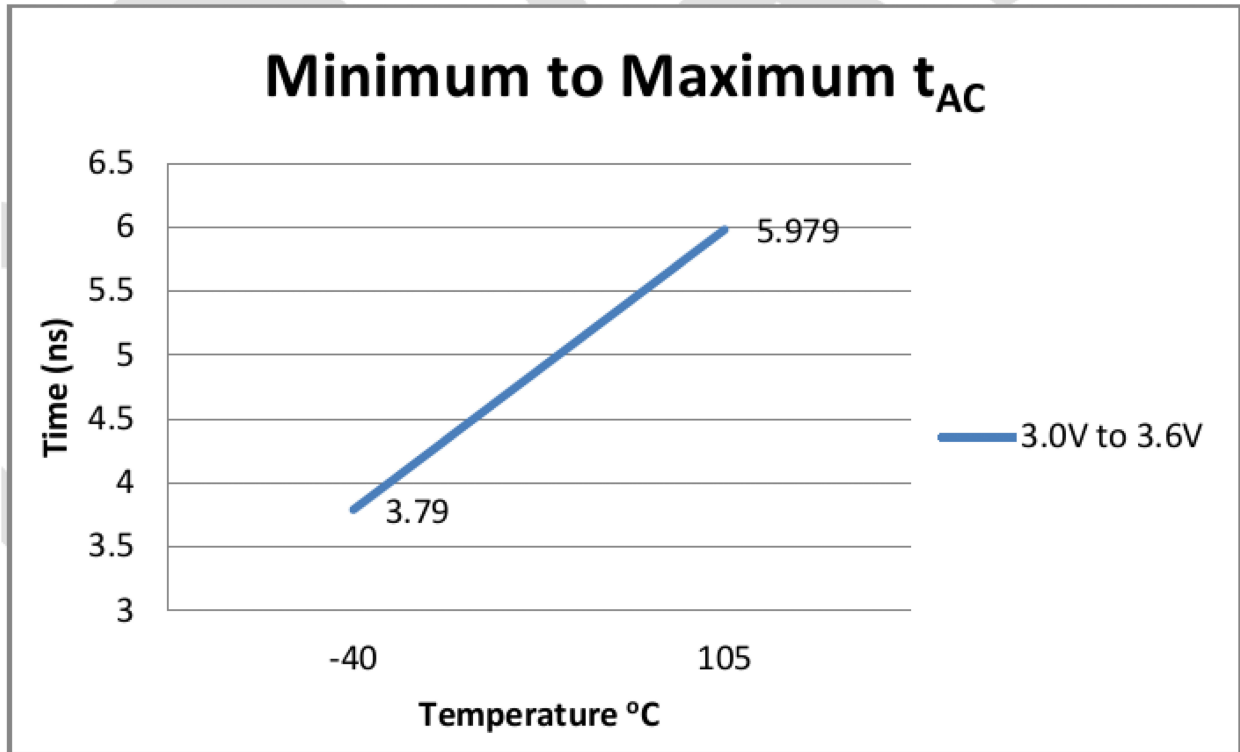
For both plots, the data is similar with respect to typical voltage at room temperature to be approximately 4.9ns. The access time of the board measurement was around 3.3ns. The variance is due to the extra loading of the tester electronics ~ 40pF and additionally the test program measurement method measures t=0 at the code initiation of the clock signal and not VDD/2 which was used for the board measurements. The min of the minimum values is 3.79ns and the max of the maximum was 5.97ns. This represents a 2.19ns total variance with respect to full voltage and temperature range. Since that is the total variance, it is reasonable to assume the variance would be distributed evenly about the mean. Therefore the variance is 1.1ns about the mean for temperature and voltage. These worst case shifts will be applied to the timing diagrams once TID effects are considered.

Pre and post irradiation data was evaluated for tAC as a function of total dose. Pre and post TID testing is performed at room temperature only on a single die package device specifically designed for TID testing. As a result, the device timing is faster than seen in the multi-die package and closer to what is measured at the 50% signal timing of the Matilda evaluation board measurements. The below plot was constructed from a 24 piece TID test sample.

SDRAM to UT700 LEON 3FT Timing & Signal Integrity Analysis UT8SDMQ64M40/48 2.5 & 3.0Gb SDRAM
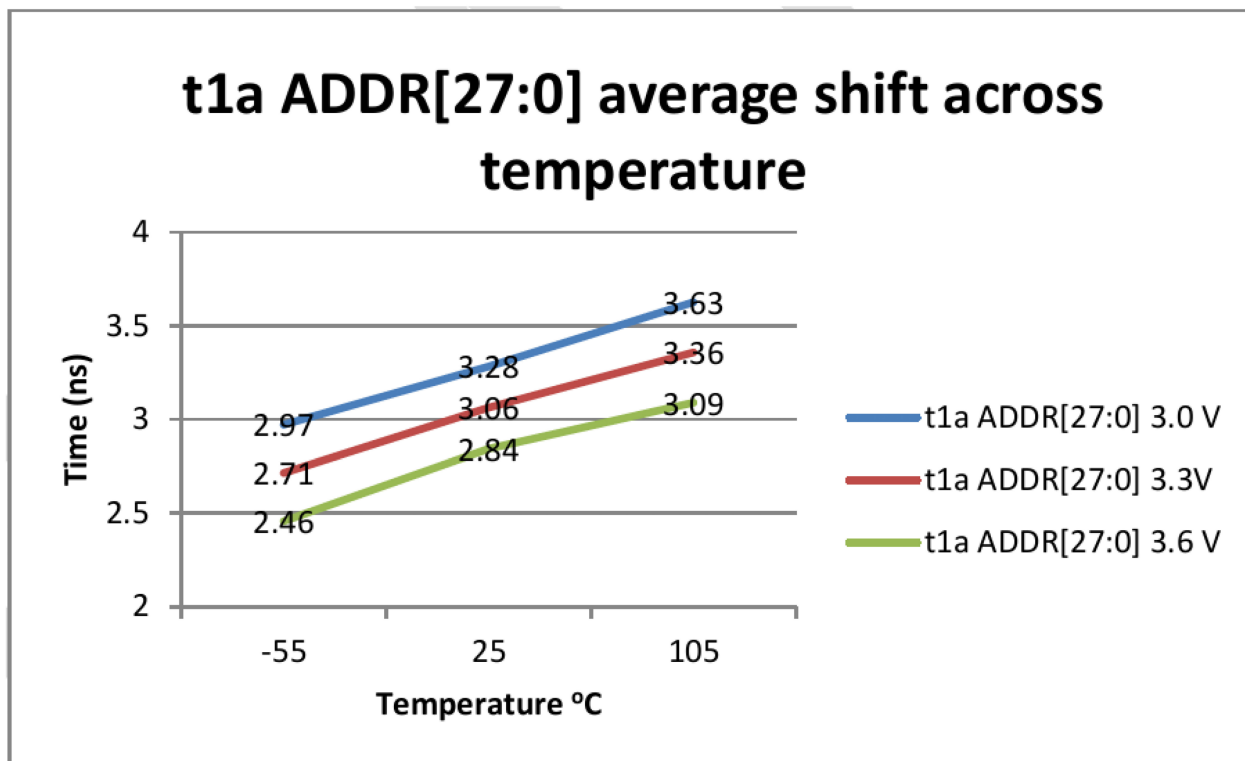

From the tri-temperature data it was calculated that the worst case shift across voltage and temperature is +/− 1.1ns about the mean. As a function of TID, the access time only decreases by the typical value of 92.5ps which is expected as Vt shifts lower due to radiation effects. Worst case min and max numbers are used for this parameter since there is no insight into individual pins. From the TID sample, the fastest (min of all minimums) and slowest (max of all maximums) were plotted to calculate the total shift of the sample with respect to full voltage range and TID as 4.386ns − 3.612ns = 774ps. Therefore it is concluded that the SDRAM access time tAC shifts with respect to TID and temperature across full voltage range conservatively could shift 1.874ns (1.1ns + 774ps) in the faster direction and 1.1ns in the slower direction. These values are added to the worst case timing analysis timing diagram of Figure 22 for SDRAM Q[3] plot.

7.2 t1a AC Characterization (SDCLK to ADDR valid)

For the remaining worst case analyses a tri-temperature 30 piece and 22 piece LEON TID samples were used. This characterization data is measured and reported on every address, data and control pin (LEON).

The first plot is for general reference. The average minimum (3.0V), mean, and maximum (3.6V) timing values of all ADRR[27:0] pins for all 30 pieces was plotted as a function of temperature. Since 3.3V is not tested, 3.3V was extrapolated assuming output time is linear as a function of voltage.

SDRAM to UT700 LEON 3FT Timing & Signal Integrity Analysis UT8SDMQ64M40/48 2.5 & 3.0Gb SDRAM

t1a ADDR[27:0] average shift across temperature

Legend:
- t1a ADDR[27:0] 3.0 V
- t1a ADDR[27:0] 3.3V
- t1a ADDR[27:0] 3.6 V

The following plot is used for the WCA. It shows the min of all the minimums of all the address pins ADDR[27:0] across full operating voltage and temperature. Inversely it shows the max of the entire maximums across voltage and temperature. The average calculated typical timing is used at 25C.

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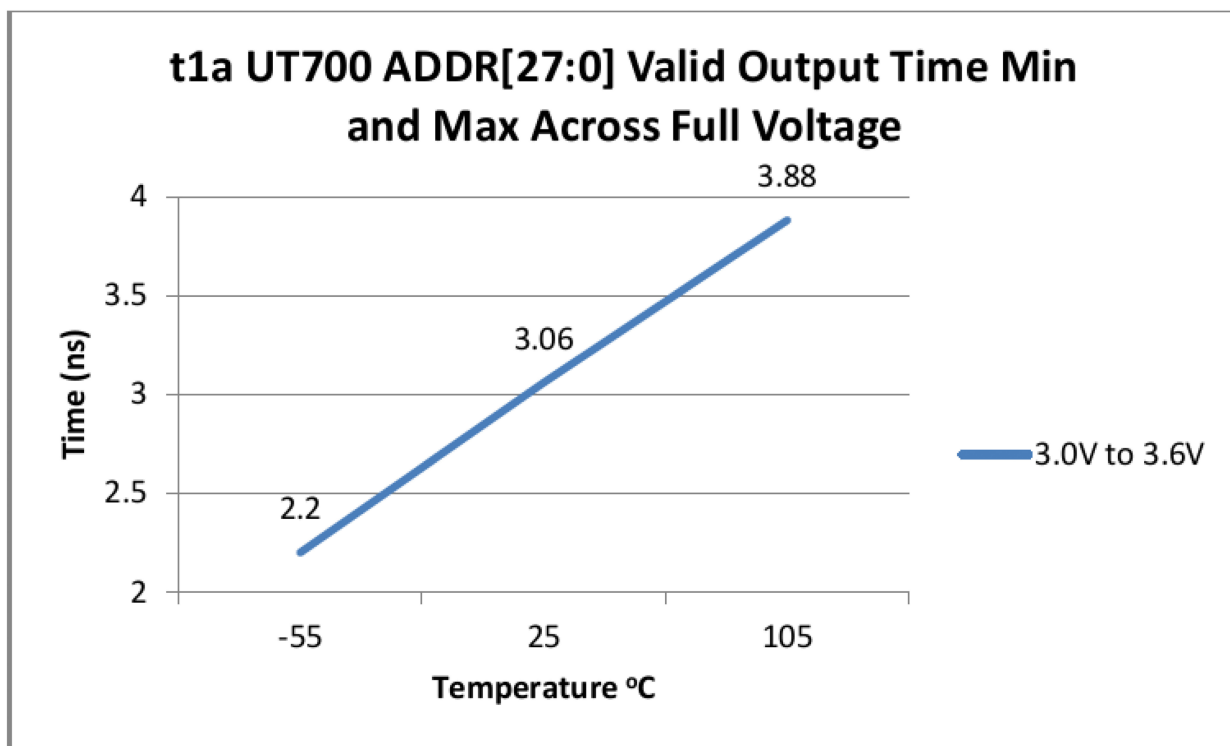
The fastest valid address signal at max voltage at −55°C of ADDR[27:0] for all 30 devices was 2.2ns and the slowest at min VDD and +105°C was 3.88ns.

The variance in timing with respect to TID was also evaluated. Characterization data was analyzed. In every instant the device performed faster at post irradiation. The difference between the min, max, and mean were calculated. The average shift in min (205ps), max (232ps) and mean (249ps). The largest individual shift observed occurred at max condition of 301ps. Therefore, this value is applied to the minimum temperature time above.

The total shift of all address outputs ADDR[27:0] with respect to voltage, temperature and TID in the faster direction is calculated from the typical 3.3V as 3.06ns − 2.2ns = 820ps + (301ps for TID) = 1.16ns. For the slower direction it is just the shift above 3.88 − 3.06 = 820ps. These variances are applied to Figure 22.

APPLICATION NOTE

7.3 t1b AC Characterization (SDCLK to /SDCS valid)
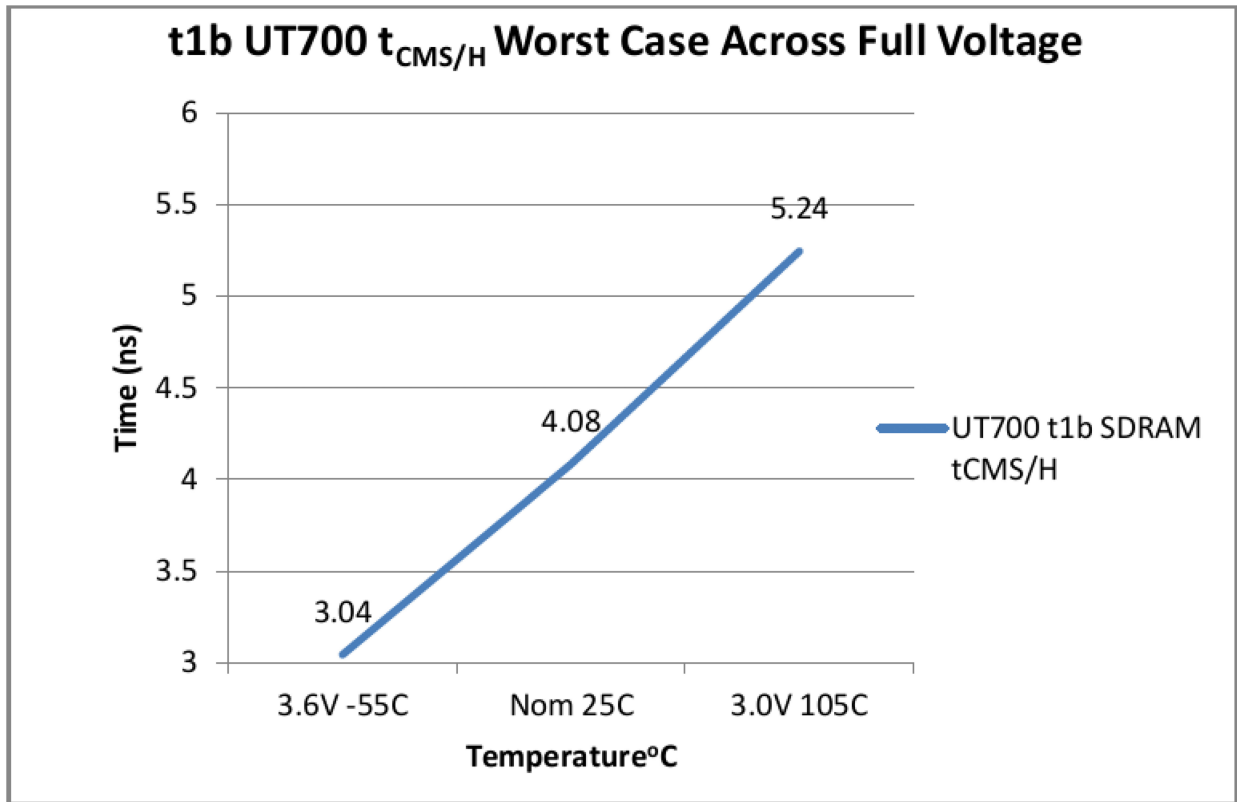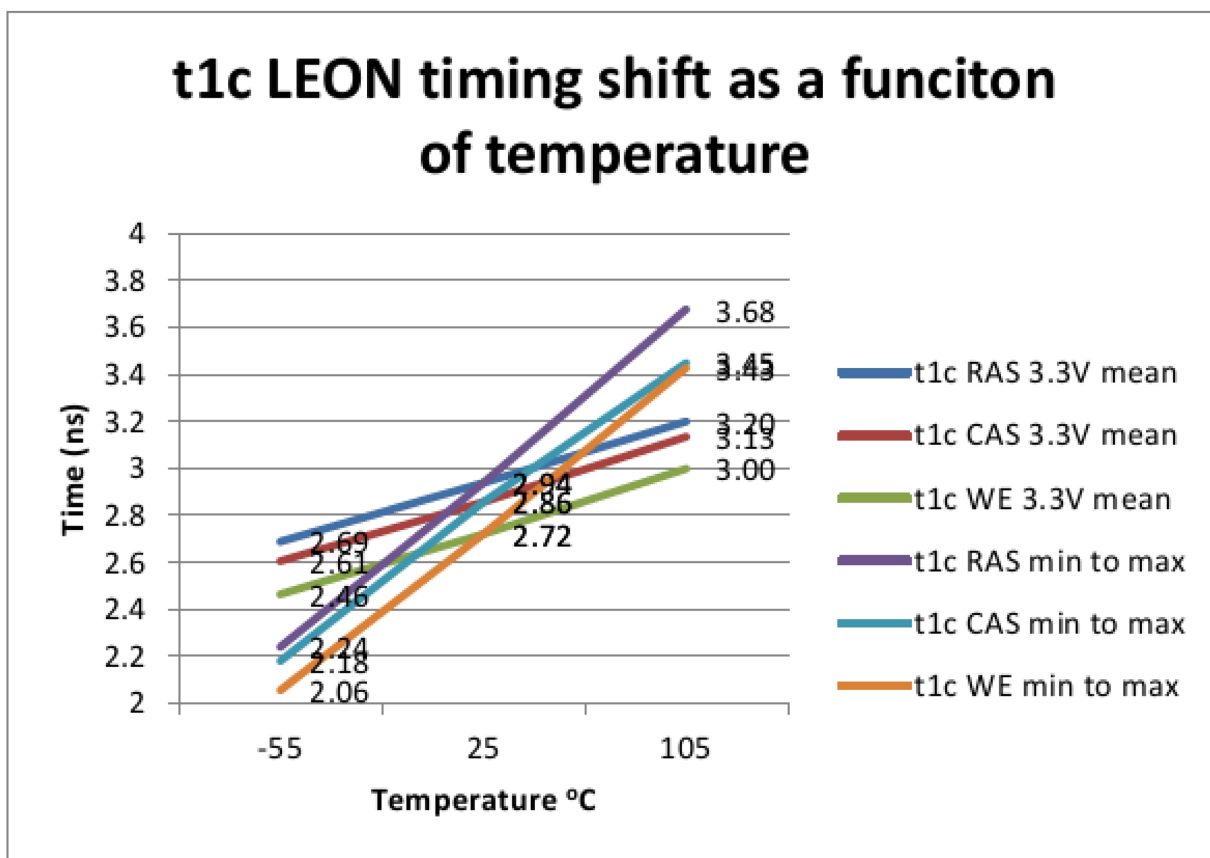

The shift applied as a function of TID is 53ps faster and 66ps slower

The worst case shift as a function of the two UT700 /SDCS outputs across full voltage and temperature range to include end of life would be 4.08ns (typ room timing) – 3.04 worst case fast timing and + 53ps end of life = 1.093ns. In the slower direction this would be 5.24 max time – 4.08 mean time + 66ps TID variance 1.226ns . These values are applied to Figure 22.

7.4 t1c AC Characterization (SDCLK to RAS, CAS, /WE valid)

t1c LEON timing shift as a funciton of temperature

Time (ns) vs Temperature °C

Values: 3.68, 3.45, 3.43, 3.20, 3.19, 3.13, 3.00, 2.94, 2.86, 2.72, 2.69, 2.61, 2.46, 2.24, 2.18, 2.06

Legend:
- t1c RAS 3.3V mean
- t1c CAS 3.3V mean
- t1c WE 3.3V mean
- t1c RAS min to max
- t1c CAS min to max
- t1c WE min to max

The shift of RAS, CAS, and WE as a function of TID is fairly negligible. The worst case shift with respect to all minimums, all maximums is 79ps faster and 38ps slower.

Therefore applying the worst case shift of all three signals against the mean of each signal and applying the worst case TID shift of all three to arrive and worst case shift for all three is:

The shift of all three signal from the mean due to low temperature was faster by 680 − 700ps, the shift due to high temperature from the mean was 590 − 740ps slower. Applying the TID end of life the fastest shift from the mean would be 700ps + 79ps = 779ps and slower by 740ps + 38 = 778ps

Therefore, +/− 780ps is added to the timing analysis of Figure 22.

7.5 t2 AC Characterization (SDCLK to data out valid)

The DATA[31:0] and CB[15:0] were analyzed for data out times. The LEON characterization data is taken with the tester load of 40pF and apt to be far less than that of the SDRAM load.

The data had some variance output to output, but the mean of all the outputs at room was calculated at 5.16ns. This value will equate to the mean of the Matilda board measurements. The min of all the minimums and max of all maximums values were acquired across full temperature and voltage and used as worst case shift from the mean. The plot is shown below and resulted in a shift due to all outputs as a function of temperature and voltage as 5.16−2.70 = 2.46ns and 7.11 − 5.16 = 1.95ns.

SDRAM to UT700 LEON 3FT Timing & Signal Integrity Analysis UT8SDMQ64M40/48 2.5 & 3.0Gb SDRAM

t2 DQ[47:0] min of mins, typ of mean, max of maxes across full voltage
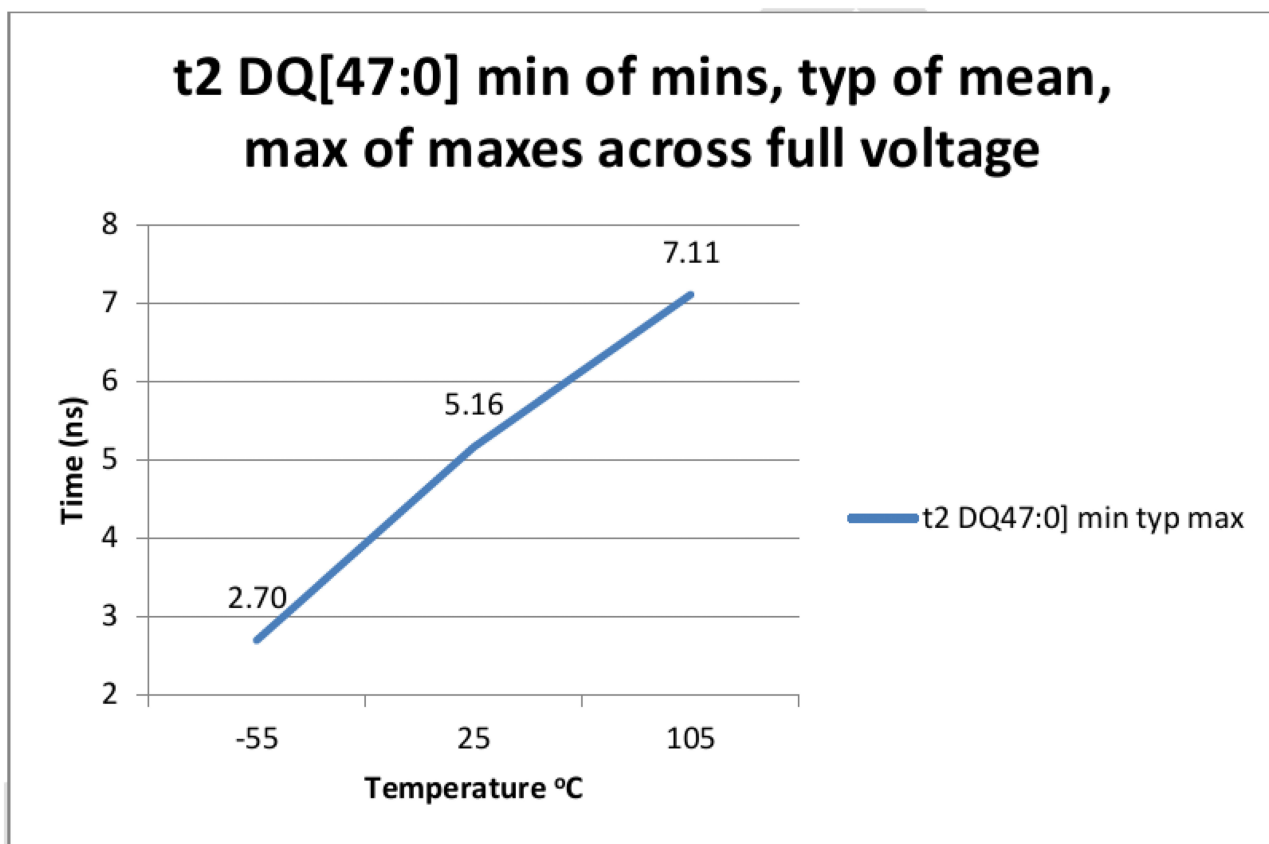
Again the variance due to TID was predominantly in the negative direction and negligible. The worst case shift in the faster direction was 172ps while the worst case in the slower was 102ps.

Therefore, the shift applied to the mean as a result of outputs, voltage, temperature, and TID is 2.63ns faster and 2.05ns slower.

For the SDRAM data in hold time, an actual Matilda board measurement was not able to be taken as the data is pulled down and only data driving high can be seen. The UT700 is not burst write capable and data will continue to drive for several additional clock cycles until the next data can be accessed. Therefore, hold time is not a concern.
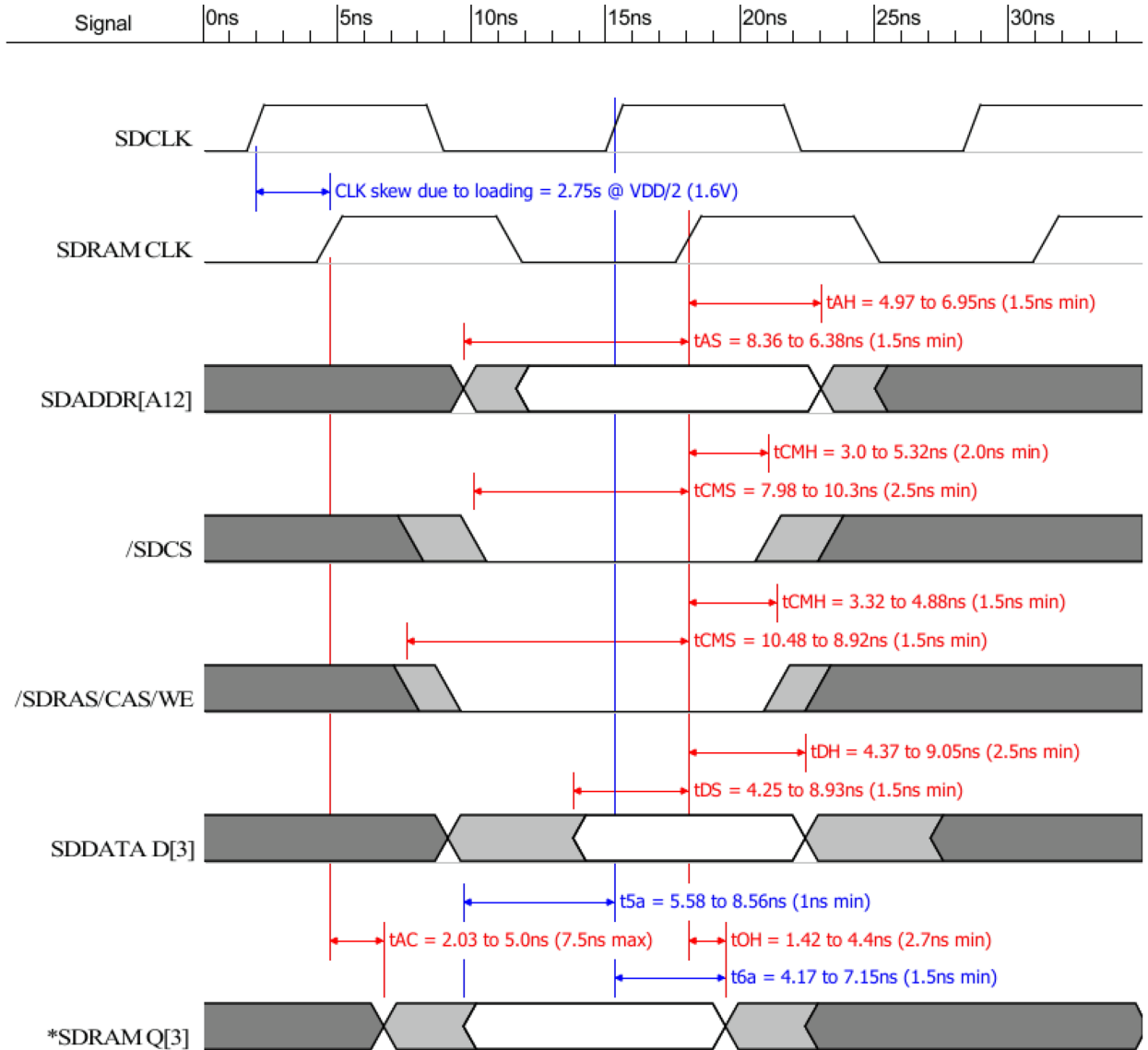
Figure 35: 75MHz Matilda evaluation board timing analysis Rs = 22 ohms and worst case expected timing variance due to voltage, temperature and irradiation.

Figure 36: 100MHz Matilda evaluation board timing analysis Rs = 10 ohms and worst case expected timing variance due to voltage, temperature and irradiation.

SDRAM to UT700 LEON 3FT Timing & Signal Integrity Analysis UT8SDMQ64M40/48 2.5 & 3.0Gb SDRAM
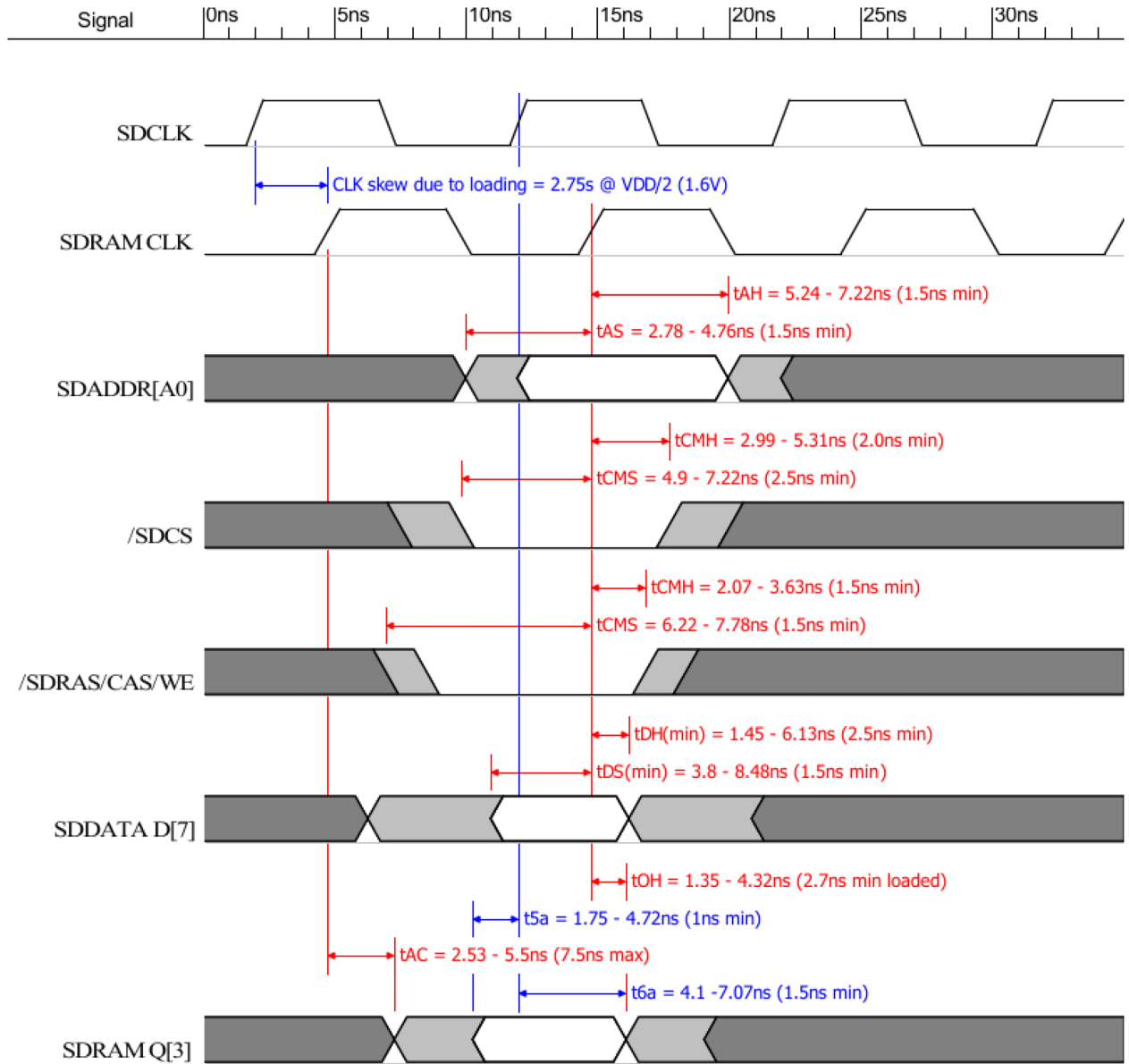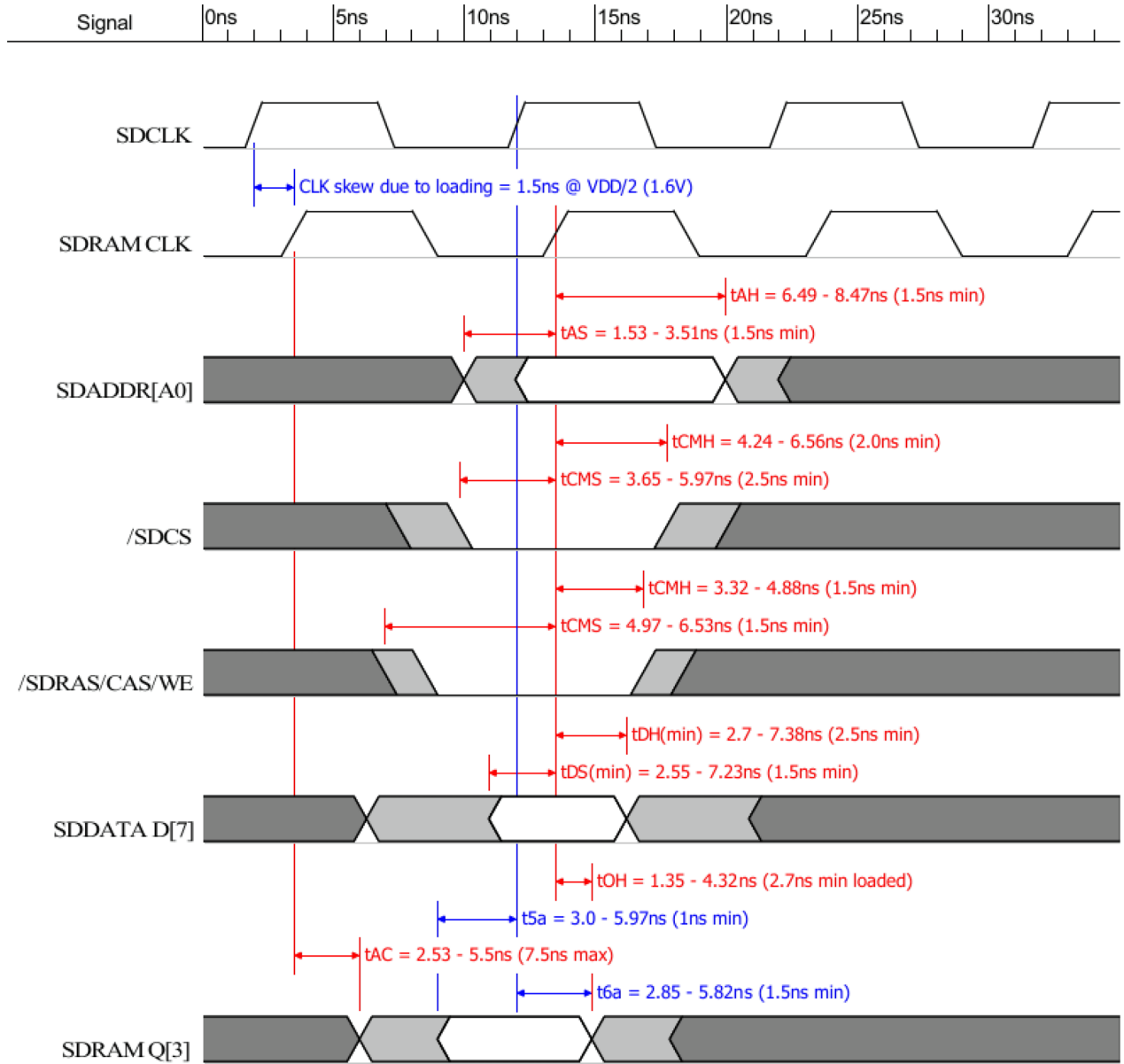

Figure 37: 100MHz Matilda evaluation board timing analysis Rs = 10 ohms and worst case expected timing variance due to voltage, temperature and irradiation with RadClock −2tu skew (−1.25ns).

8.0 Conclusion

A direct connection between CAES' UT700 LEON 3FT SPARC™ V8 Microprocessor and CAES' 2.5Gb and 3.0Gb SDRAM modules is functionally possible. A datasheet timing analysis at 100MHz reveals that most of the timing requirements overlap with none in violation. Timing margin is built into the testing as all parameters are tested to meet specifications at worst case temperatures and voltages. Running at lesser frequencies, increases timing margin for all the SDRAM setup time requirements, but does not affect the overlap of the SDRAM hold time requirements. Instituting a clock buffer between the two devices can create hold margin by ideally distributing the margin equally between setup and hold requirements. However, datasheet timing analysis assumes ideal signal characteristics (0ns rise and fall times). Beyond the specification timing analysis, it may be necessary to consider an analysis of actual signals due to signal characteristics such as rise and fall times.

The SDRAM's internal complexity necessary to meet DLA's QML Q level mechanical stress requirements in a single x48 bus width hermetic package results in a tradeoff between circuit board area savings and signal integrity. HyperLynx simulations using CAES' S-Parameter IBIS model results in large non-monotonic reflections at the SDRAM package clock input pin. Smaller non-monotonic reflections exist at some of the active die clock input pads. While CAES' currently available S-Parameter IBIS model is useful for selecting the best series resistor for your board layout, actual signal measurements at maximum frequency of 100MHz show no non-monotonic clock signals at the inputs of the functional SDRAM dice. This results in full functionality at 100MHz. Actual timing measurements of the application show margin at both 75MHz and 100MHz. Worst case timing analysis was performed using characterization for both devices across full temperature and voltage range. This represents an over exaggeration as it considers both worst case temperature in conjunction with worst case voltage which would not occur typically in system operations. Applying this data results in no timing violations at 75MHz and one violation at 100MHz for the SDRAM data input hold time tDH. CAES' RadClock could be used to correct this timing. After applying the worst case analysis, tOH at both 75MHz and 100MHz appears to be out of specification. This is attributed to the difference in measurement techniques between physical and ATE (automated test equipment). The SDRAM hold time requirement does not affect the operation of the SDRAM, but only affects the operation of the LEON. When the 2.75ns delay between the SDRAM and LEON clocks is taken into account, the LEON hold time is actually well within its input requirements.

CAES' SDRAM is specified and tested at 100MHz across full temperature and operating voltage range. The Matilda evaluation board functions at 100MHz with a complete write and read of patterns to the SDRAM at room temperature. While 100MHz may be possible, it is not recommended for all applications especially if the application requires some timing margin for system specifications. The RadClock is useful for adjusting signal timing with respect to circuit clocks occurrences. The SDRAM S-Parameter IBIS model results in an exaggeration of signal reflections from actual operating signal measurements. Using the model to examine signal properties and timing for the best series resistance for a given application is recommended. CAES continues to work towards offering a more accurate signaling model solution.

Finally, CAES application engineering believes that while the interior configuration of our 2.5Gb and 3.0Gb SDRAM processor memory solution presents challenges, it represents one of the best processor memory options qualified to a QML Q for the aerospace market. It is CAES' hope that this application note and data presented herein provides confidence that the SDRAM is capable of operating reliably in similar application up to 83MHz across most system temperature ranges.

SDRAM to UT700 LEON 3FT Timing & Signal Integrity Analysis UT8SDMQ64M40/48 2.5 & 3.0Gb SDRAM

9.0 Revision History

Date	Rev. #	Author	Change Description
02/26/2019	1.0.0	Mike Leslie	Initial Release