Features/Capabiltities	IntelliProp	Arasan	Siglead	Phison	Cadence	Xilinx	Boyuan	Marvell	Hyperstone	Comments
Webpage		https://www.arasan.com/products/nand-flash/onfi-4-1/	http://siglead.com/eng/product/ip/nand.php	https://www.phison.com/en/solutions/enterprise	https://ip.cadence.com/ipportfolio/ip-portfolio-overview/memory-ip/nand-flash/nand-flash-controller	https://www.xilinx.com/products/intellectual-property/1-fod2wk.html	http://www.bjbytech.com/index_en.html	https://www.marvell.com/products/storage/ssd/technologies.html	https://www.hyperstone.com/en/Silicon-IP-Core-NAND-Flash-Controller-1376.html	
ONFI Level	3.2 and 4.0	ONFI 3.2, 4.0 and 4.1			ONFI 4.x (excluding EZ-NAND), ONFI 3.x, and Toggle 2	3.2 and 4.0	ONFI 2/3/4			Xilinx does not mention TLC
Transaction Speed	266MT/s NV-DDR2 mode 5	NV-DDR2: 400MHz NV-DDR3: 600MHz			1200MT/s					
Density/LUNs supported	128 total NAND targets	1Tb limit				128 total NAND targets				
ECC Support	BCH	For SLC Flash, Hamming Code is being used for 1 bit error correction and 2 bit error detection. BCH Code, capable of up to 32-Bit error correction, is used for MLC and TLC Flash devices	BCH		BCH	BCH	BCH and LDPC			
Page size		Page Size – 2KB, 4KB, 8KB, 16KB	2 to 16K Bytes		256B to 16kB		2KB, 4KB, 8KB and 16KB			
Data integrity support (Wear Leveling, Bad Block Management, Garbage Collection, etc)			Bad Block Management, Wear Leveling (Dynamic/ Static), Garbage Collection, etc., can also be provided							
Source Format (Verilog/VHDL)	Verilog	Verilog	Verilog		Verilog	Verilog	Verilog			
Open / Encrypted Source	Encrypted									
Target Platform (Xilinx/Intel/ASIC)	Xilinx/Intel	No specific FPGAs called out	Xilinx, Altera, Lattice		No specific FPGAs called out	No specific FPGAs called out	No specific FPGAs called out			
Supported interfaces	NV-DDR, DDR2, Toggle 2.0	NV-DDR, DDR2, DDR3				NV-DDR, DDR2, Toggle 2.0				
		Multi LUN/DIE Operations; On-die termination; Interleaving operations; Programmable timing; Address cycles – 4, 5; ECC enable, disable; RAM size – 1KB, 2KB and 4KB; Supports parallel connection of two 8-bit flash devices;	NAND block size : 64 to 512 pages Test bench and test patterns are also provided	Appears to be an hardware controller; Don't know if IP is an offering	Support for multi-LUN modes; give the impression that TLC parts are supported only in SLC mode			Appears to be an hardware controller; Don't know if IP is an offering	No specific info listed	