UT7R995/C RadClock Jitter Performance

Table 1: Cross Reference of Applicable Products

PRODUCT NAME	MANUFACTURER PART NUMBER	SMD #	DEVICE TYPE	INTERNAL PIC NUMBER
RadClock Multi-phase PLL Clock Buffer	UT7R995 UT7R995C	5962-05214	01-04	WD27 WD35

1.0 Overview

Clock jitter is a critical performance parameter in most electronic systems today. As next generation system clocks run faster, the direct impact of jitter also increases proportionately. For example, excess jitter on the system clock can have the following results: 1) adversely impacts the bit error rate (BER) in serial data systems, 2) degrades accuracy of, and therefore reduces speed for clocks in computer central processing units (CPUs) and digital signal processors (DSPs), and 3) limits the signal-to-noise ratio (SNR), reducing the effective number of bits (ENOB) of resolution of analog-to-digital converters (ADCs). The UT7R995/C RadClock Multi-phase PLL Clock Buffer provides a multi-phase, multiple output, low jitter clock with selectable, user-defined output frequencies from a single input reference clock. The UT7R995/C includes an internal phase-locked loop (PLL). The internal PLL provides "zero delay" operation when using an external feedback path, and can reduce jitter transfer from the input reference clock due to the low-pass filter (LPF) operation of the PLL loop bandwidth (BW).

This Application Note (AN) provides a brief overview of clock jitter, including definitions and general measurement methods. The primary purpose of this AN is to present additional measured jitter data for the UT7R995/C RadClock and is supplemental to the data sheet. The measured jitter data contained in this AN is for reference only and not guaranteed, since the RadClock has not been fully characterized over all conditions specified in the data sheet during testing for this AN. These data include time domain cycle-to-cycle (C2C) jitter (J_{C2C}) and period jitter (J_{PER}) from oscilloscope measurements, and phase, or random jitter (J_R) derived from frequency domain phase noise measurements.

2.0 Technical Background

The UT7R995/C RadClock 2.5V/3.3V 200 MHz High-Speed Multi-Phase PLL Clock Buffer is a low-voltage low-power, eight-output, 6-200 MHz clock driver with output clock phase programmability. The core power supply is 3.3V. The outputs can be operated on either 2.5V or 3.3V power supplies, where output banks 1-4 can be operated using either 2.5V or 3.3V independently of one another.

3.0 Clock Jitter: General Description and Information

Timing jitter is defined as the unwanted phase modulation of a digital or analog signal and is considered one of the most important requirements for specifying, or measuring a device's signal integrity and quality. Jitter is an unwanted variation in signal period, frequency, phase, duty cycle or other timing characteristic and can be of interest from cycle to cycle, over many consecutive cycles, or even longer-term. This section of the AN describes some of the basic terminology and measurement techniques used in quantifying and characterizing jitter in general and for clock jitter specifically.

3.1 Elements of Clock Jitter

Clock signals are periodic. Clock jitter is primarily determined by random noise processes in the clock source and not by deterministic jitter (J_D), or data-dependent jitter (J_{DD}) contributors as can be the case for high-speed data signals, for example. Since clock jitter is a random process, it is best described by Gaussian (normal) statistics with units of seconds (s), root mean square (rms).

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Clock random jitter (J_R) is primarily dependent on the clock signal rise and fall times (tr,tf) for square wave signals and its analog, slew rate (SR), for sine wave signals, as well as device input noise voltage (v_n, rms) in both cases. The simple relationships between J_R, SR, and v_n for a sine wave clock are shown below in Equations 3.1a,b and Figures 3.1a,b.

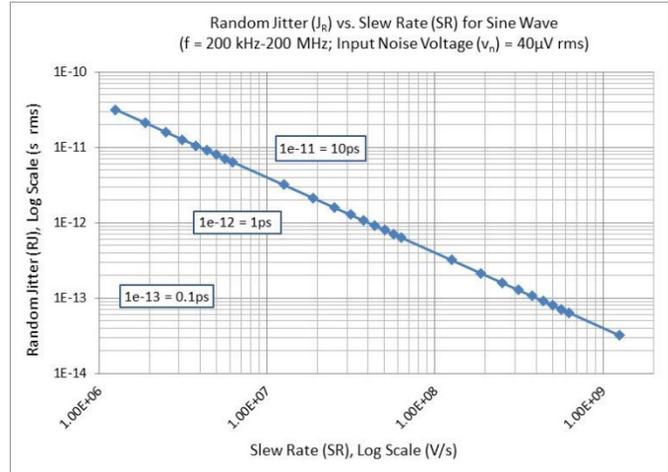**Slew Rate (SR) = 2πfA = ωA; A=Vpk=Amplitude (V), f=frequency (Hz)** (3.1a)

Figure 3.1a: Random Jitter vs. Slew Rate for a Sine Wave Signal (Simulated)

J_R = v_n(rms)/SR (3.1b)
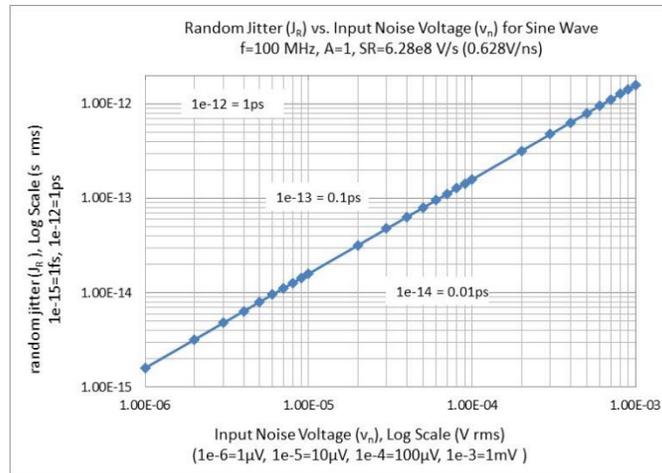
Figure 3.1b: Random Jitter vs. Input Noise Voltage for a Sine Wave Signal (Simulated)

In general, increasing slew rate (SR) or clock frequency, and decreasing v_n or receiver (Rx) rms input noise voltage for a sine wave input results in lower J_R. Figure 3.1c shows the time uncertainty (Δτ), or random jitter (J_R) for two different SR, but fixed amplitude sine wave clock signals. Consider an arbitrary active Rx device (e.g. clock buffer) in the clock signal path with input voltage noise v_n, where v_n is the same rms value for both SR cases in Figure 3.1c. The lower frequency clock (left-hand figure), with lower slew rate (SR_1), will spend more time in the linear region where the noise of the input circuit , resulting in greater time uncertainty, as represented by $Δτ_1$, versus the higher frequency clock (right- hand figure), with higher slew rate (SR_2) and smaller time uncertainty $Δτ_2$.
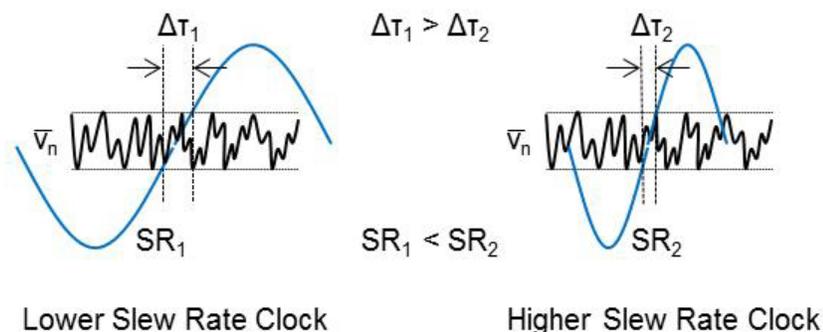
Figure 3.1c: Slew Rate Dependence of Random Jitter

A square wave clock may be used to achieve faster input tr, tf, however, there are additional considerations for a square wave clock. A square wave clock must also contain additional frequency content over the fundamental clock frequency, as shown by Fourier Analysis, while a sine wave clock is a much closer approximation to a single frequency or tone. A square wave clock, for example, may have higher jitter versus a sine wave clock due to additional frequency content, harmonics, spurs, etc., which can nullify any jitter reduction due to higher edge rate/slew rate. Phase noise measurements and associated jitter calculations using a predetermined integration bandwidth for either clock source shows the actual phase jitter and so can be used as a selection tool for choosing between different clock sources and signal formats.

Clock jitter is random jitter (J_R) and its distribution is unbounded. This means that the peak-to-peak (p-p) value is not well defined. Because J_R is unbounded, determining p-p value is best accomplished by defining the p-p value at a given bit error rate (BER). The rms J_R clock jitter value can be converted to a peak-to-peak (p-p) value by multiplying by the Gaussian statistics crest factor corresponding to the desired BER. This method, and in the example calculation, below, assumes that there is no deterministic jitter (J_D) component, which is a good assumption for clock signals.

Example calculation:

Inputs:

BER = 1e-12; Typical value for many high-speed data communication systems = 1 error per 1 Trillion bits transmitted.

J_R = Random Jitter = 1 ps (rms)

Data Transition Density (DTD) for a clock signal =1

Crest Factor = ɑ = 14.261

J_D = Deterministic Jitter = 0 ps (p-p)

Calculation:

J_R p-p = ɑ * J_R rms   (3.1c)

jitter (p-p) = 1 ps (rms) * 14.261 = 14.261 ps (p-p)

Crest factors for a range of BER and data or clock signal formats is given in Table 3.1a, below.

Table 3.1a: J_R rms to J_R p-p conversion: Crest Factor (α) vs. BER

BER	Crest Factor = α*	
	Data Transition Density (DTD) = 0.5 (Typical Data Signals)	Data Transition Density (DTD) = 1 (Clock Signals)
1e-01	2.563	3.290
1e-02	4.653	5.152
1e-03	6.180	6.581
1e-04	7.438	7.781
1e-05	8.530	8.834
1e-06	9.507	9.783
1e-07	10.399	10.653
1e-08	11.224	11.461
1e-09	11.996	12.219
1e-10	12.723	12.934
1e-11	13.412	13.613
1e-12	14.069	14.261
1e-13	14.698	14.882
1e-14	15.301	15.479
1e-15	15.883	16.054
1e-16	16.444	16.610

* From Gaussian statistics:

$Q(x) = 0.5 * erfc(x/\sqrt{2})$; x = BER, erfc(x) is the complementary error function (3.1d)

$BER(Q_{BER}) = 0.5*DTD*erfc(Q_{BER}/\sqrt{2})$; (3.1e)

$Q_{BER} = \sqrt{2} * erfc^{-1}(2*BER/DTD)$ (3.1f)

$α = 2*Q_{BER}$ (3.1g)

3.2 Jitter: Time Domain vs. Frequency Domain

Clock jitter is typically defined as three main types. These are 1) cycle-to-cycle jitter (J_{C2C}), 2) period jitter (J_{PER}), and 3) phase jitter (R_{PH}), which is also called random jitter (J_R). All three types of jitter can be measured in the time domain, while R_{PH} (J_R) is measured most accurately in the frequency domain from phase noise data.

Test and measurement equipment for jitter characterization consists of time domain oscilloscopes or frequency domain signal source analyzers (SSAs), spectrum analyzers (SAs), or phase noise analyzers (PNAs). The frequency domain equipment has the lowest noise floor compared to oscilloscopes and so phase noise techniques are the preferred method for clock jitter measurements since they are the most accurate. The rms phase jitter can be derived from phase noise measurements by integrating phase noise over a specified bandwidth (BW). It is common to use the SONET OC-48 jitter BW of 12kHz-20MHz, as a reference, for example. An SA with phase noise measurement software can also be used for measuring phase noise and for calculating J_R.

These three jitter types are detailed and defined below in Equations 3.2a-c and Figures 3.2a-f, below.

- Cycle-to-Cycle Jitter (J_{C2C}) is the maximum time difference between two adjacent clock periods over N clock cycles, where N = 10^3.

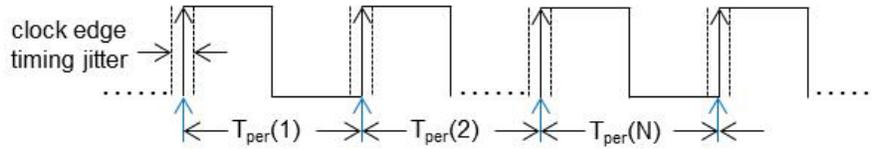$$J_{C2C} = \max\{|T_{per}(n) - T_{per}(n+1)|\} ; 1 \le n \le N, \text{ ps p-p} \quad (3.2a)$$

Figure 3.2a: Cycle-to-Cycle jitter definition

- Period Jitter (J_{PER}) is the time difference between the ideal clock period $T_{per}(0)$ and the measured clock period T_{per} (n) over N clock cycles, where N = 10^3, or 10^4.

$$J_{PER} = |T_{per}(0) - T_{per}(n)| ; 1 \le n \le N, \text{ ps p-p.} \quad (3.2b)$$
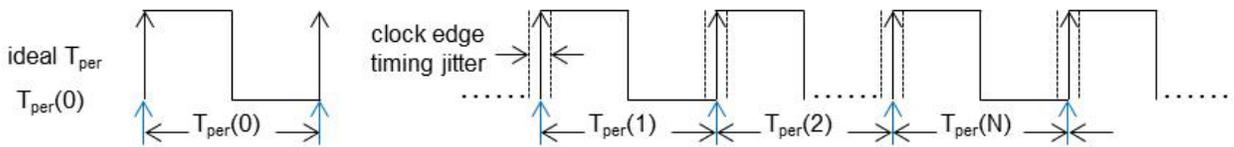
Figure 3.2b: Period jitter definition

Phase jitter (R_{PH}) is most accurately measured in the frequency domain as derived from phase noise measurements. The following equation is used for calculating phase jitter (J_{PH}), or random jitter (J_R), and is typically performed by software included as part of the phase noise measurement equipment.

$$J_R = (1/2\pi f)*\sqrt{(2\int L(f)df}; L(f) \quad (3.2c)$$

L(f) is the single sideband (SSB) phase noise spectrum (dBc/Hz). The integration BW is specified by the user, as described above.

Figures 3.2c-f , below, depict phase noise calculation and plotting from frequency spectrum measurements and also shows the integration bandwidth on the phase noise plot that is used to calculate phase or random jitter. Only random jitter (J_R) components are shown.
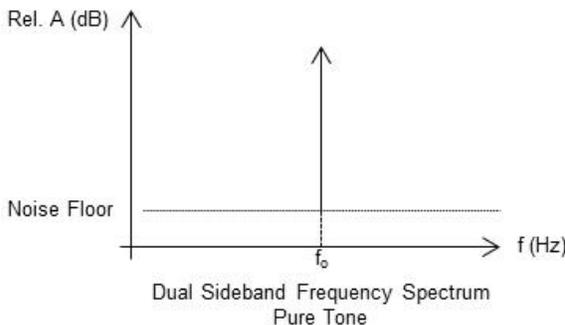

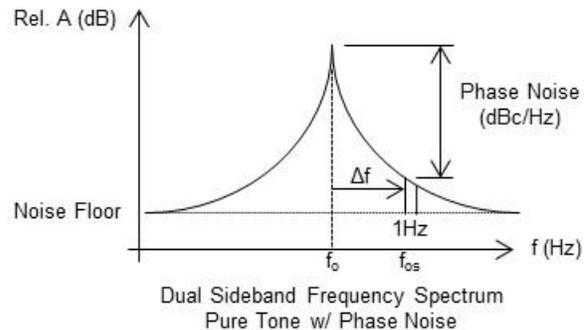**Figure 3.2c: Frequency Spectrum of Single Tone without Phase Noise**

Figure 3.2d: Frequency Spectrum of Single Tone with Phase Noise

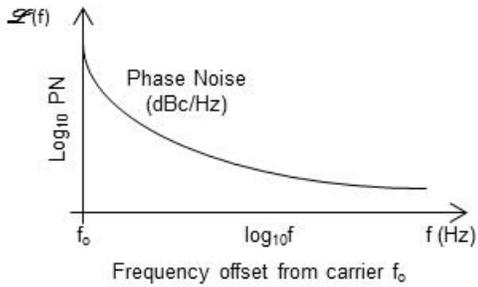# UT7R995/C RadClock Jitter Performance

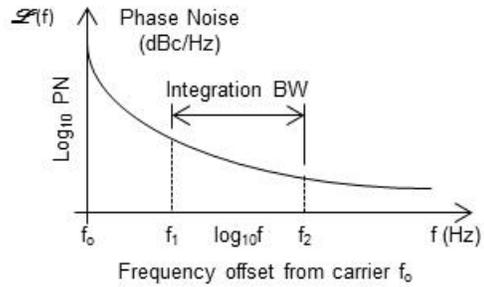**Figure 3.2e: Phase Noise vs. Frequency without Integration BW shown**

Figure 3.2f: Phase Noise vs. Frequency with Integration BW for J_R calculations

The SONET OC-48 integration band, or mask of 12kHz-20MHz is widely used as a standard integration BW when calculating phase jitter from phase noise for typical system clock signals. This mask was chosen for UT7R995 RadClock Phase Jitter measurements. Other bands, or masks can be implemented, depending on the selected data protocol, or other user requirements, such as phase noise (dBc/Hz) at a limited set of frequencies (Hz), for example.

3.3 UT7R995/C RadClock Measured Jitter Data

Measured jitter data for : Cycle-to-Cycle Jitter (J_{C2C}), Period Jitter (J_{PER}), and Phase, or Random Jitter (J_R) are presented in this section as summary plots of the respective jitter vs. RadClock output frequency, divider settings and temperature. Details of the test conditions and RadClock settings are provided in Section 3.3.0.

3.3.1 Test Equipment Setup and Measurement Conditions

Test equipment setup is presented in this section for both Time-Domain and Frequency-Domain measurements. The custom low noise, low jitter, dedicated 3.3V LVCMOS clock source is used for all measurements. The complete integrated test equipment setup configuration is shown below as a block diagram in Figure 3.3.0.a.

Time-Domain measurements: Cycle-to-Cycle Jitter (J_{C2C}) and Period Jitter (J_{PER}) are defined and measured in the time- domain, and so a digital sampling oscilloscope (DSO) is used for this purpose. A LeCroy oscilloscope is used to observe and measure the device under test (DUT) output waveforms, and calculate J_{C2C}.and J_{PER} . The LeCroy (WRXi-) JTA2-OM- E Rev. A Jitter & Timing Analysis software option is the primary application used for time-domain jitter measurement and analysis. The number of clock cycles for Time-Domain measurements was set per JEDEC standard JESD65B, Table 2, p.2; *Definition of Skew Specifications for Standard Logic Devices*.

Table 3.3.1.a: Number of Clock Cycles for Time-Domain Jitter Measurements

Jitter Type	Number of Clock Cycles
Cycle-to-Cycle Jitter (J_{C2C})	1,000
Period Jitter (J_{PER})	10,000

Frequency-Domain measurements: Phase, or Random Jitter (J_R) is most accurately measured in the frequency-domain. A Spectrum Analyzer with Phase Noise (PN) software is used for this purpose. An Agilent N9030A PXA Spectrum Analyzer combined with N9068A PN Application software is used to measure PN, and calculate J_R by integrating PN over a specified bandwidth (BW). The integration BW selected is the SONET OC-48 mask of 12kHz-20MHz. The lower frequency bound for Phase/Random Jitter measurements was limited to 50 MHz due to noise floor limitations of the test equipment.

The remaining equipment shown is used for VDD biasing, temperature control, and for automation of the measurements, including data collection. Both Time- and Frequency-Domain measurements are made during each test program step, where the RadClock configuration settings are fixed. Configuration settings are /N, /R divider ratios and input frequencies. The program then moves to the next step with different configuration settings. The VDD power supplies are set to nominal 3.3V and temperature is held constant for each complete set of RadClock configuration settings. Jitter measurements are made at three temperatures: -55°C, +25°C, and +125°C. The data presented in this AN reflects the maximum jitter value measured for each jitter type (i.e. J_{C2C}, J_{PER}, J_R), across three different DUTs. All measurements were performed in an Engineering lab via bench measurements and not in a production test environment.
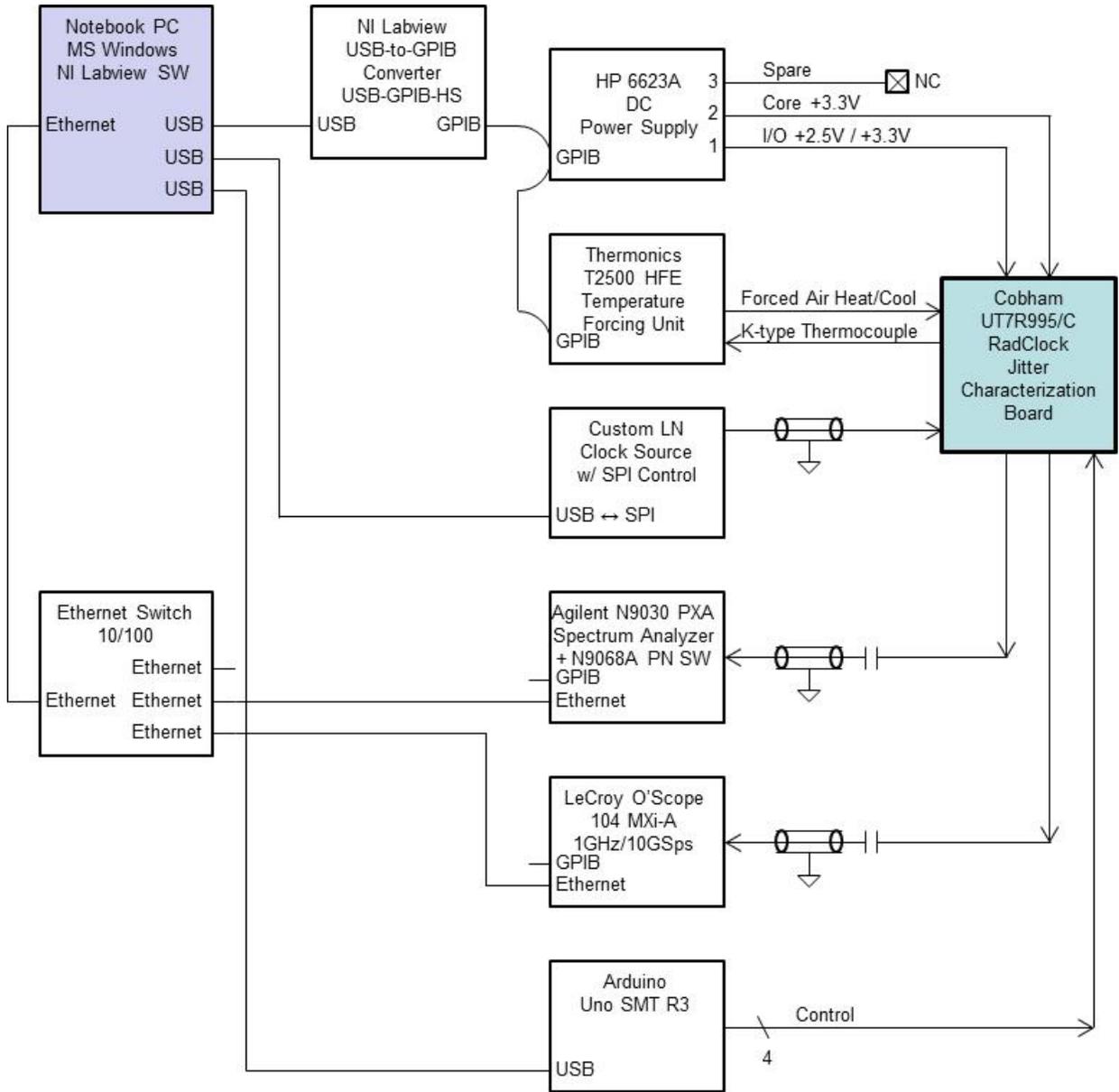
Figure 3.3.1.a: Test Equipment Setup Block Diagram

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3.3.2 Measured Data - Cycle-to-Cycle Jitter (JC2C)
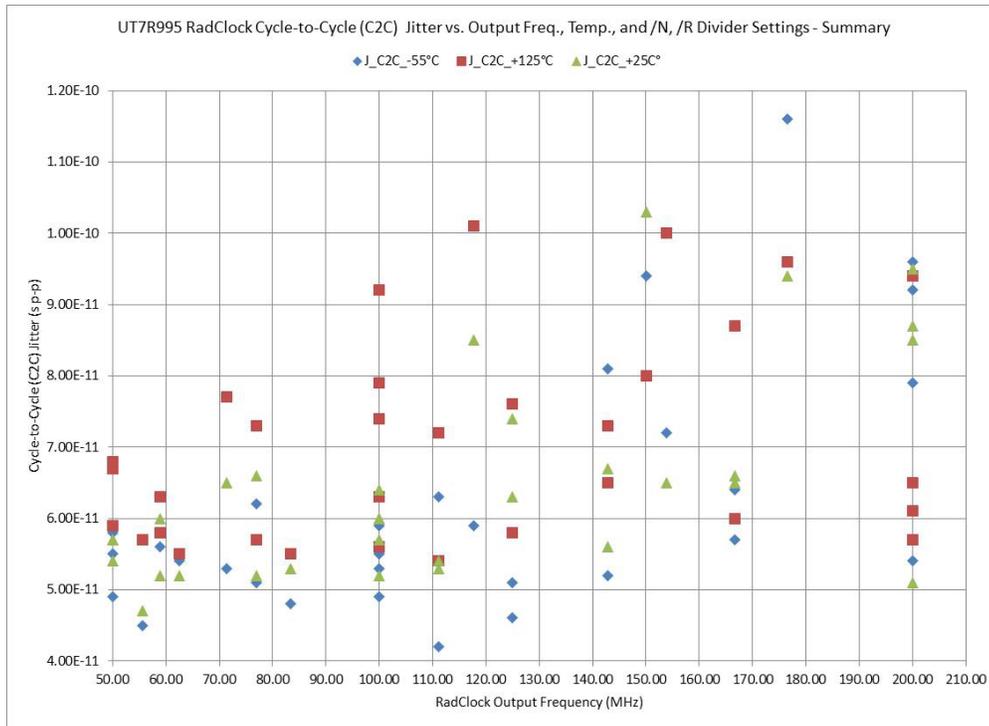
Figure 3.3.2.a: Cycle-to-Cycle (C2C) Jitter (JC2C) vs. Output Frequency
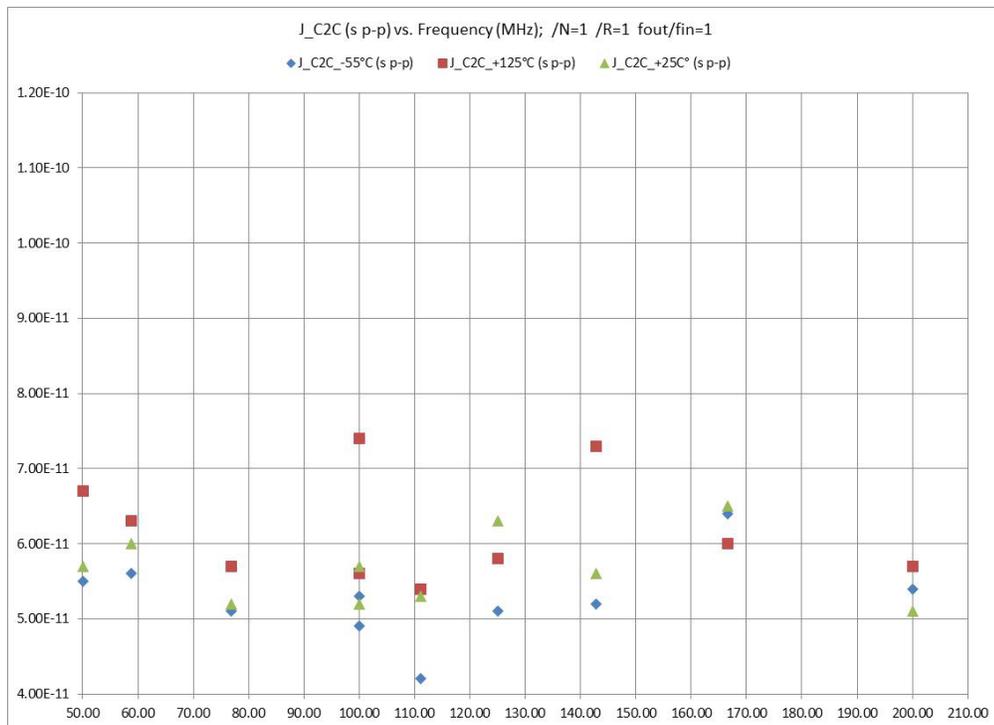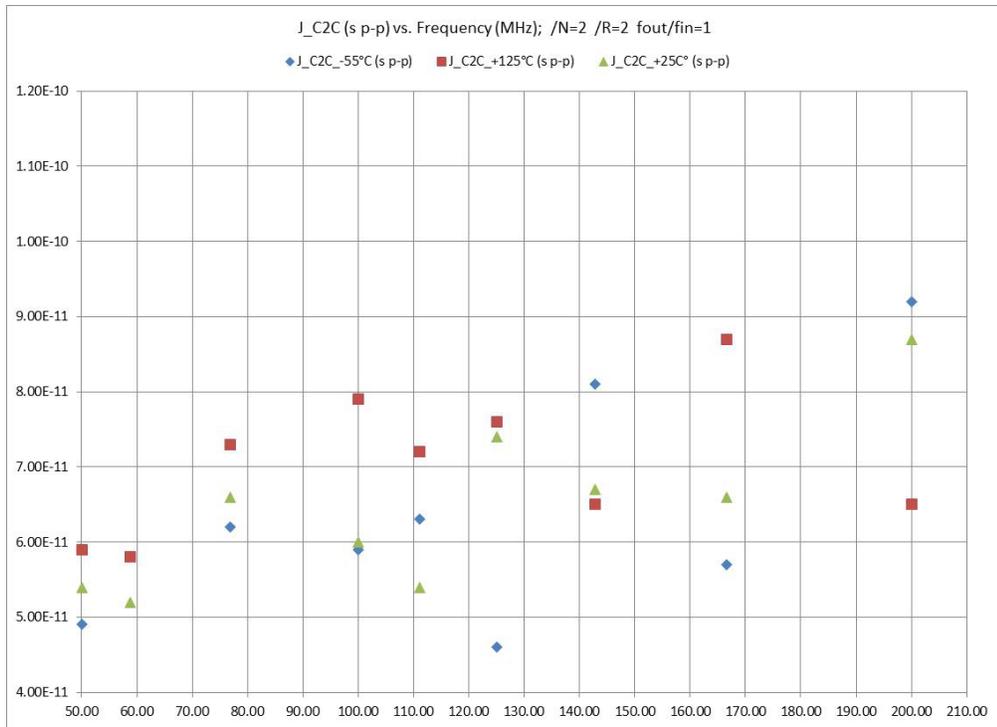and PLL Divider Settings: /N, /R – Summary

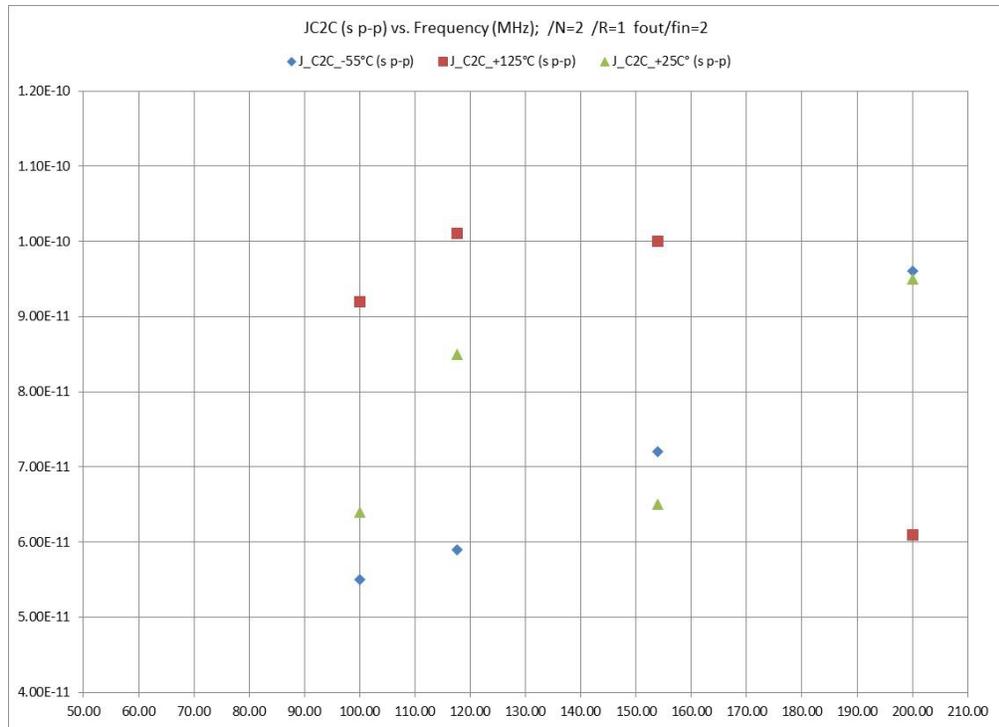Figure 3.3.2.b: Cycle-to-Cycle (C2C) Jitter (J_{C2C}) vs. Output Frequency
and PLL Divider Settings: /N=1, /R=1

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**Figure 3.3.2.c: Cycle-to-Cycle (C2C) Jitter (JC2C) vs. Output Frequency
and PLL Divider Settings: /N=2, /R=2**
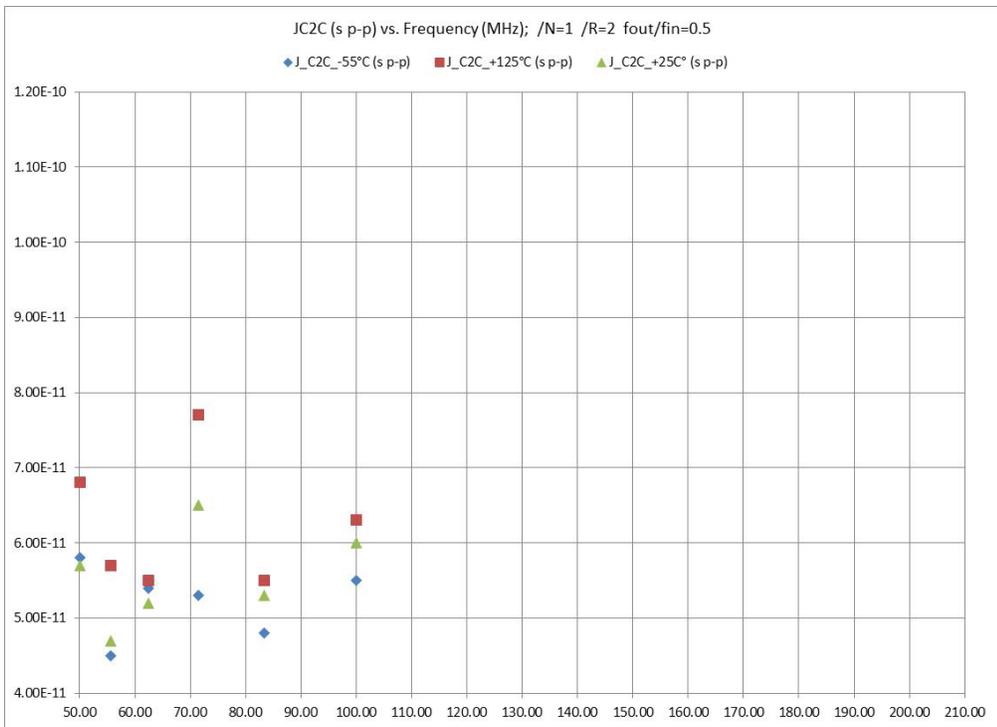
**Figure 3.3.2.d: Cycle-to-Cycle (C2C) Jitter (J$_{C2C}$) vs. Output Frequency
and PLL Divider Settings: /N=1, /R=2**

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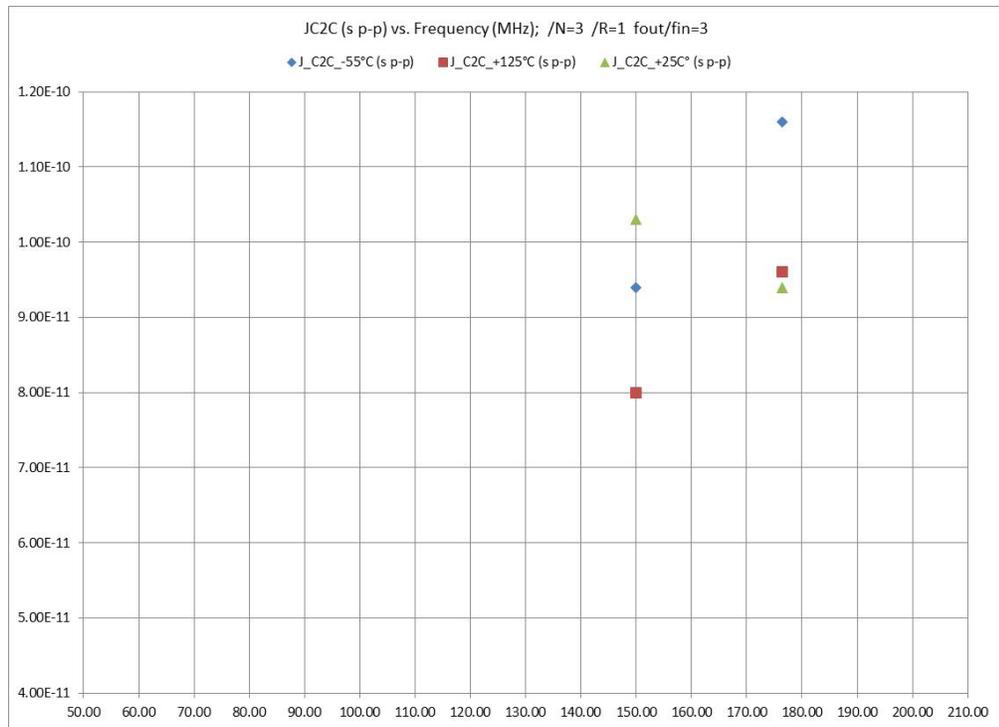**Figure 3.3.2.e: Cycle-to-Cycle (C2C) Jitter (J$_{C2C}$) vs. Output Frequency and PLL Divider Settings: /N=2, /R=1**

Figure 3.3.2.f: Cycle-to-Cycle (C2C) Jitter (J$_{C2C}$) vs. Output Frequency and PLL Divider Settings: /N=3, /R=1

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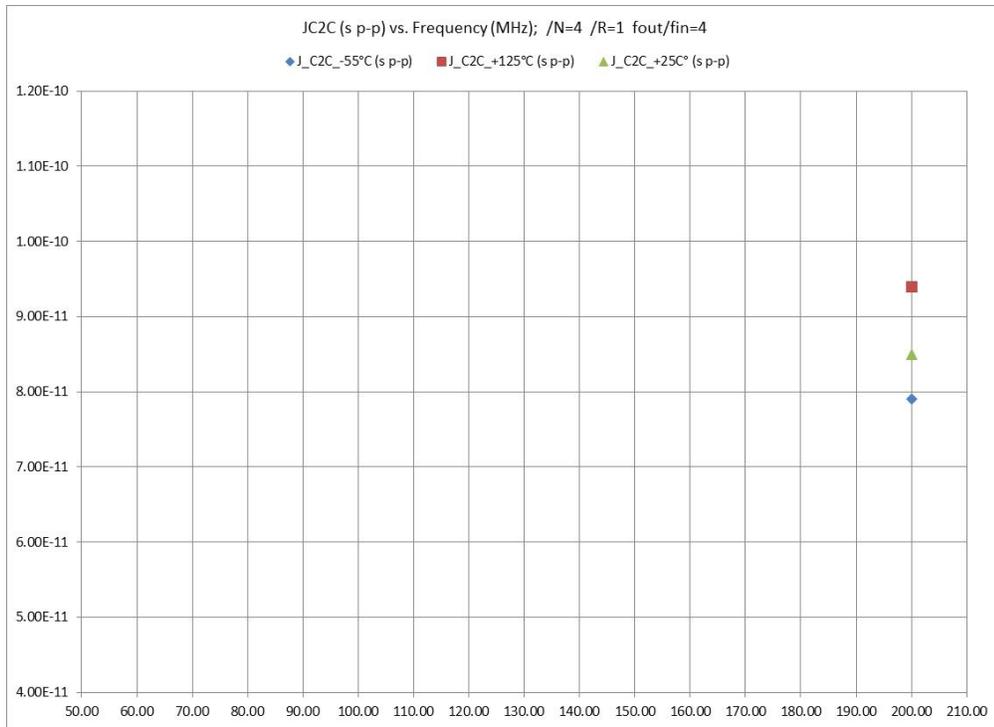
Figure 3.3.2.g: Cycle-to-Cycle (C2C) Jitter (J$_{C2C}$) vs. Output Frequencyand and PLL Divider Settings: /N=4, /R=1
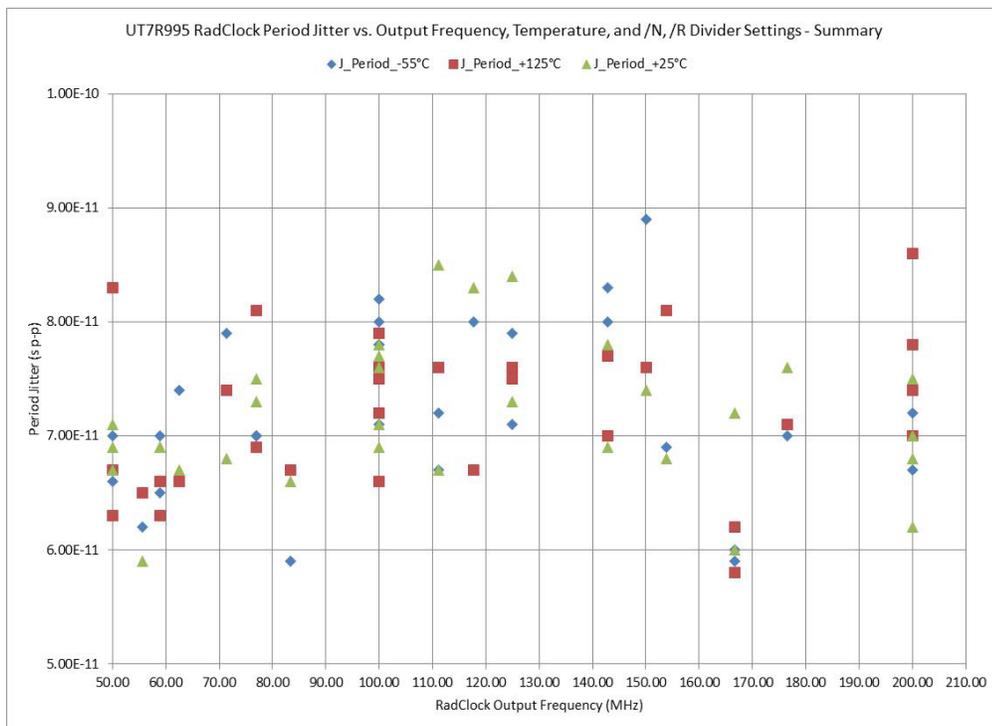
3.3.3 Measured Data - Period Jitter (J$_{PER}$)

Figure 3.3.3.a: Period Jitter (J$_{PER}$) vs. Output Frequency and PLL Divider Settings: /N, /R - Summary

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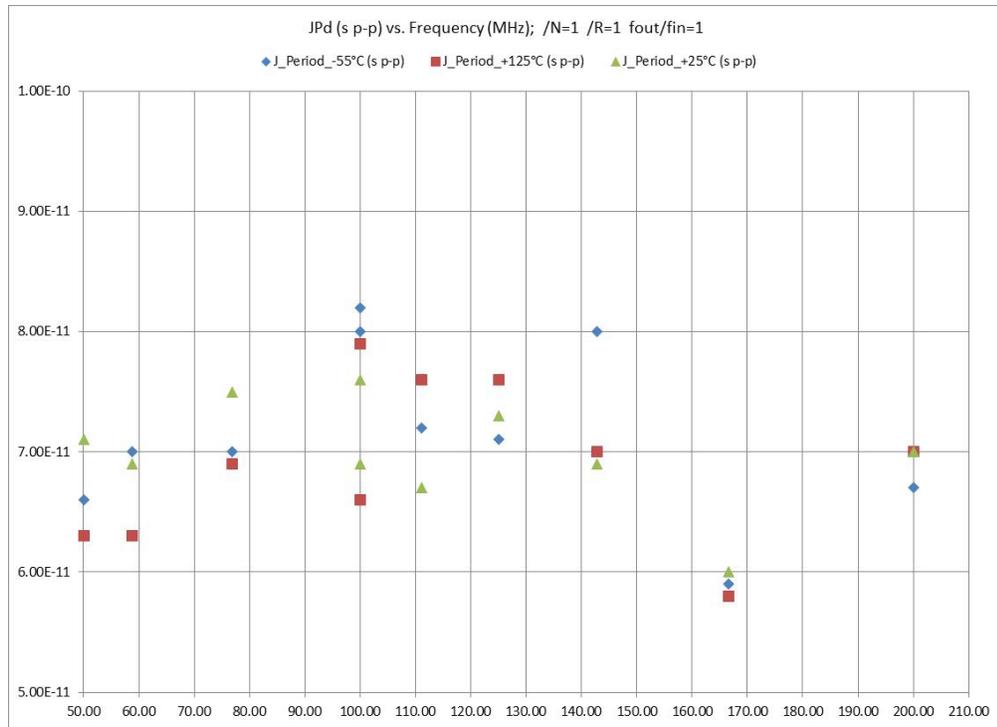
**Figure 3.3.3.b: Period Jitter (J$_{PER}$) vs. Output Frequency
and PLL Divider Settings: /N=1, /R=1**

**Figure 3.3.3.c: Period Jitter (J$_{PER}$) vs. Output Frequency
and PLL Divider Settings: /N=2, /R=2**

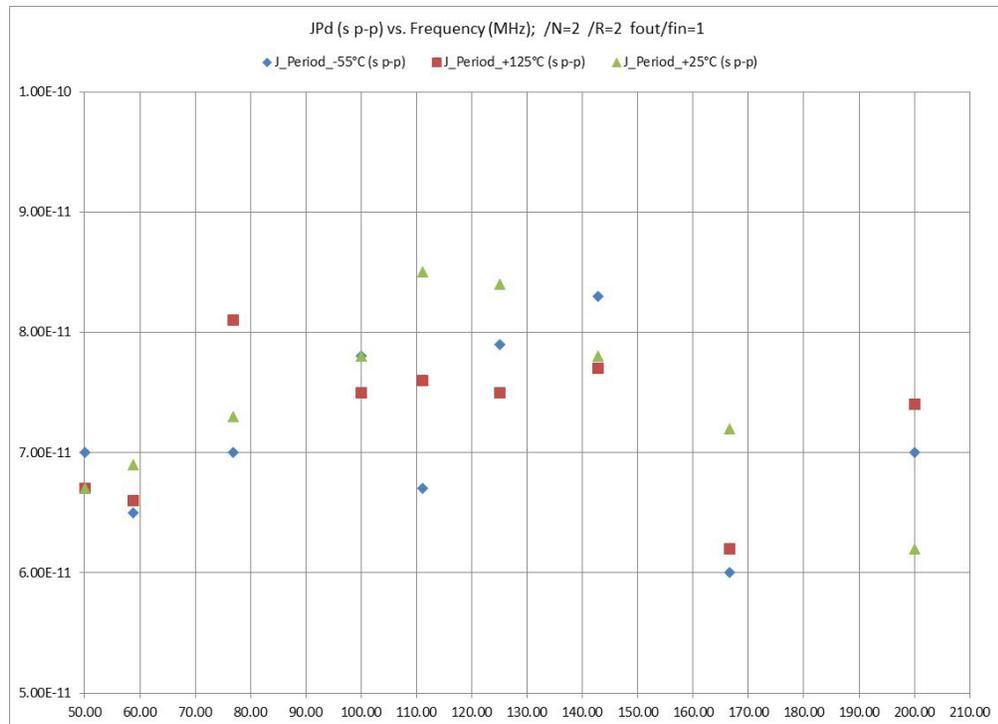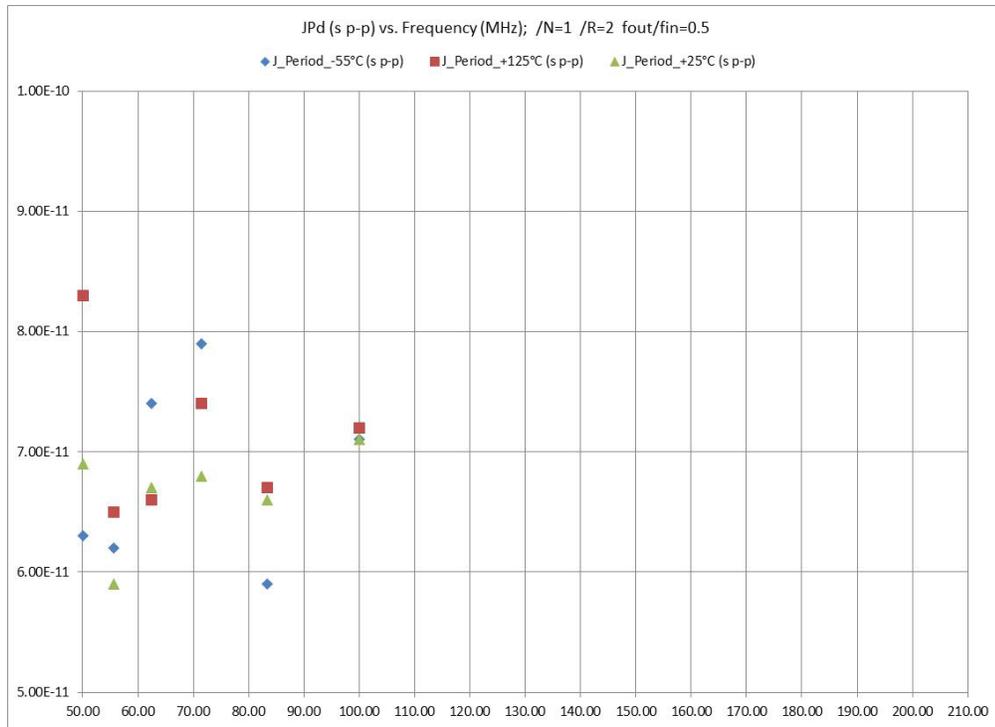**Figure 3.3.3.d: Period Jitter (J$_{PER}$) vs. Output Frequency and PLL Divider Settings: /N=1, /R=2**

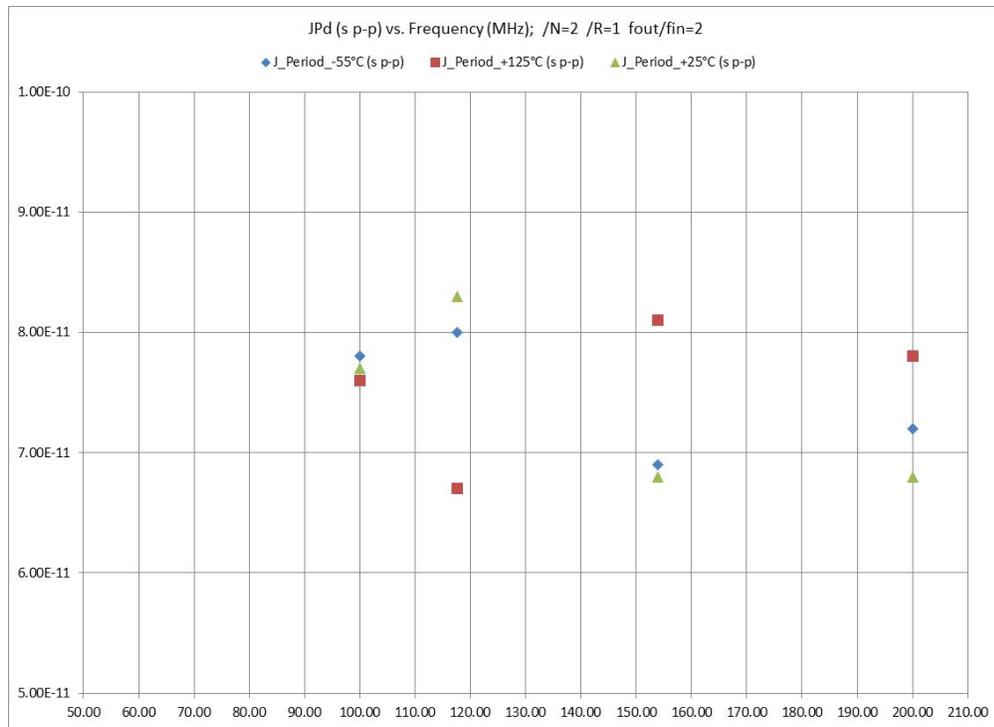**Figure 3.3.3.e: Period Jitter (J$_{PER}$) vs. Output Frequency and PLL Divider Settings: /N=2, /R=1**
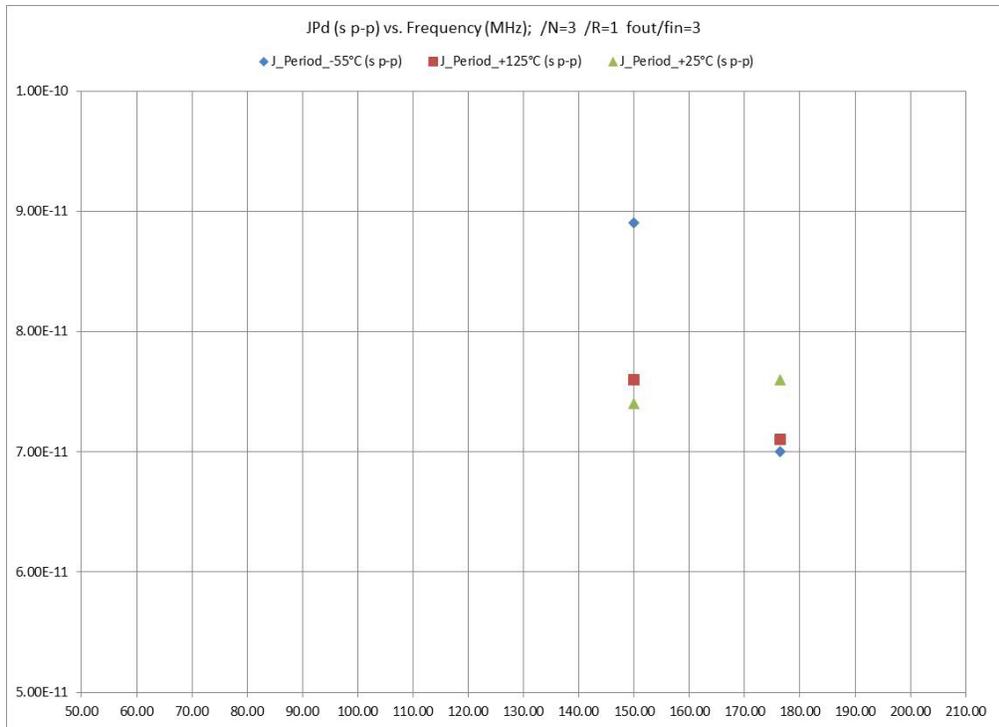
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Figure 3.3.3.f: Period Jitter (J$_{PER}$) vs. Output Frequency and PLL Divider Settings: /N=3, /R=1

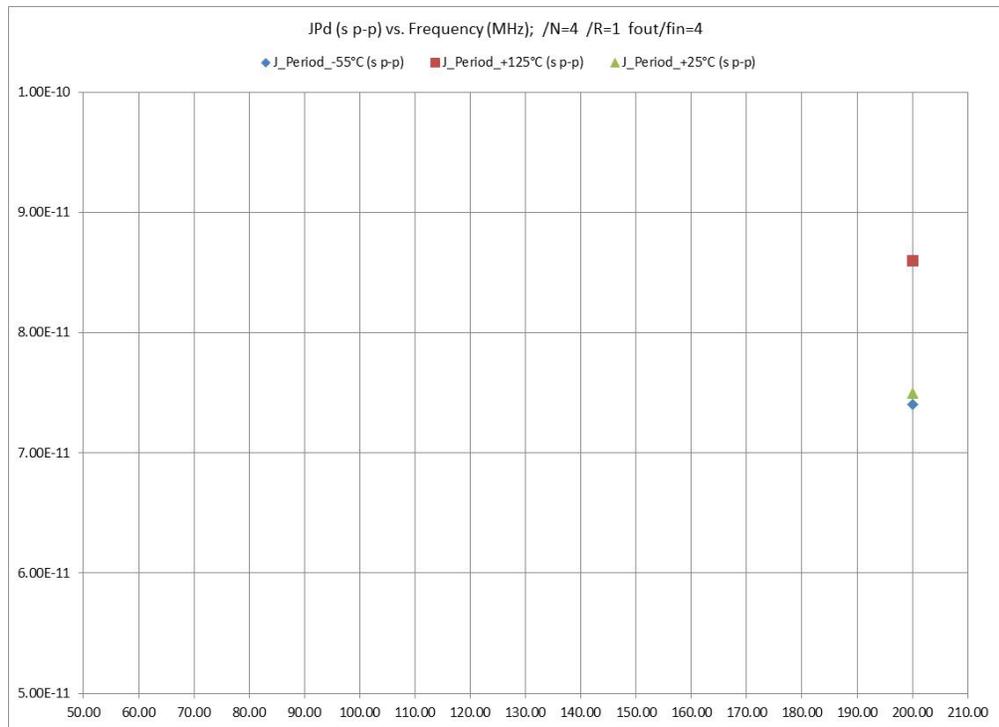**Figure 3.3.3.g: Period Jitter (J$_{PER}$) vs. Output Frequency and PLL Divider Settings: /N=4, /R=1**

3.3.4 Measured Data - Phase or Random Jitter (J_R)

Figure 3.3.4.a: Phase or Random Jitter (J_R) vs. Output Frequency and PLL Divider Settings: /N, /R - Summary
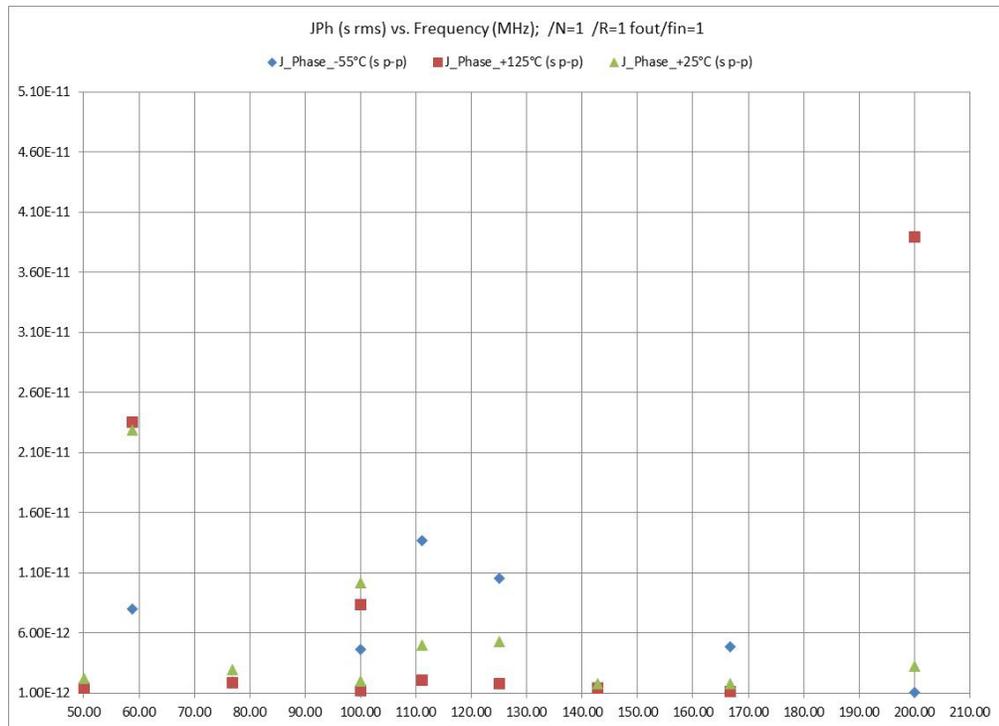
Figure 3.3.4.b: Phase or Random Jitter (J_R) vs. Output Frequency and PLL Divider Settings: /N=1, /R=1

Figure 3.3.4.c: Phase or Random Jitter (J_R) vs. Output Frequency and PLL Divider Settings: /N=2, /R=2
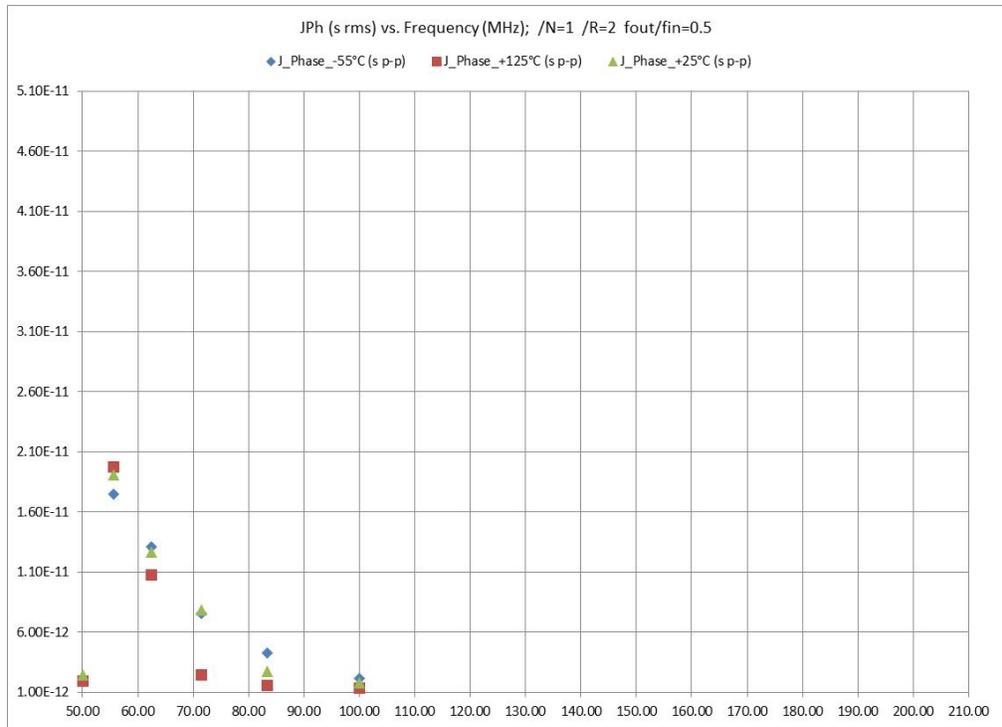
Figure 3.3.4.d: Phase or Random Jitter (J_R) vs. Output Frequency and PLL Divider Settings: /N=1, /R=2

Figure 3.3.4.e: Phase or Random Jitter (J_R) vs. Output Frequency and PLL Divider Settings: /N=2, /R=1
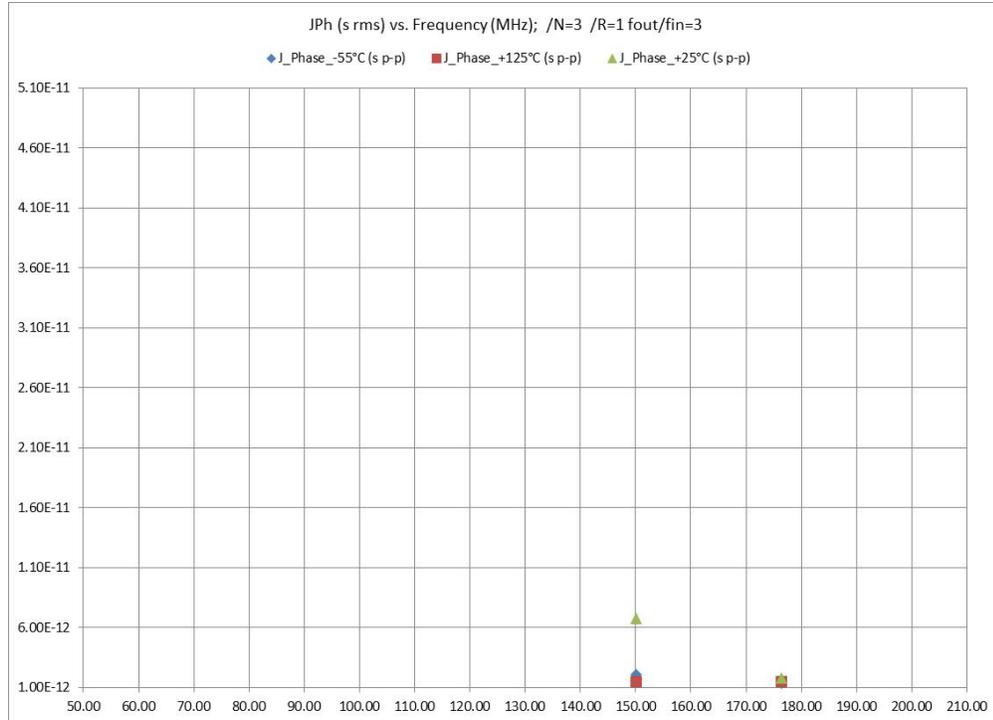
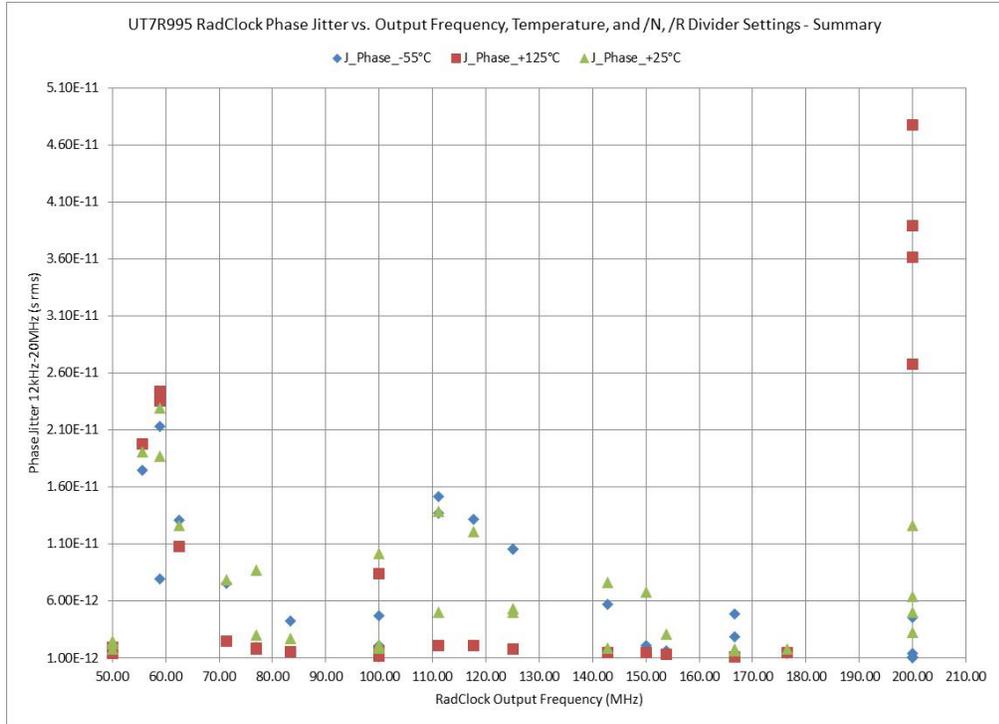**Figure 3.3.4.f: Phase or Random Jitter (JR) vs. Output Frequency and PLL Divider Settings: /N=3, /R=1**

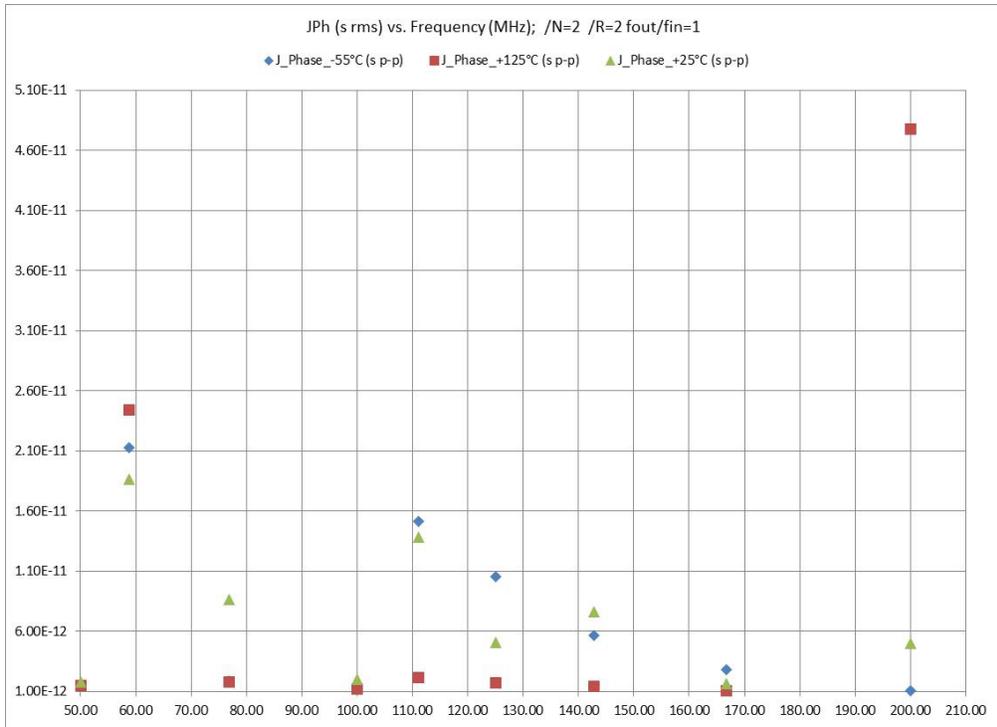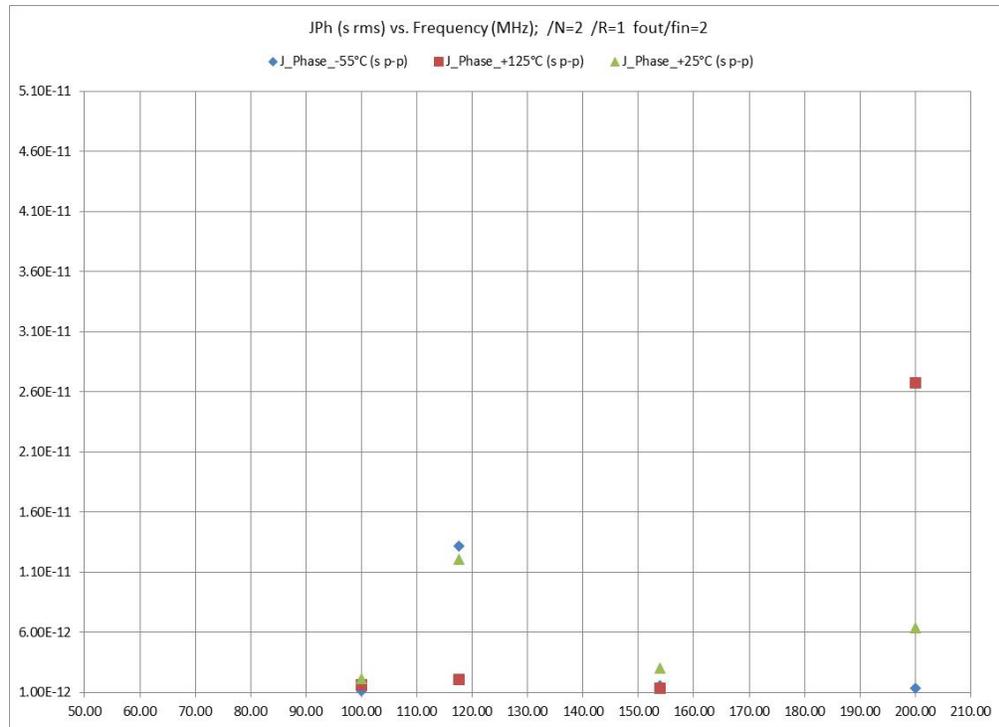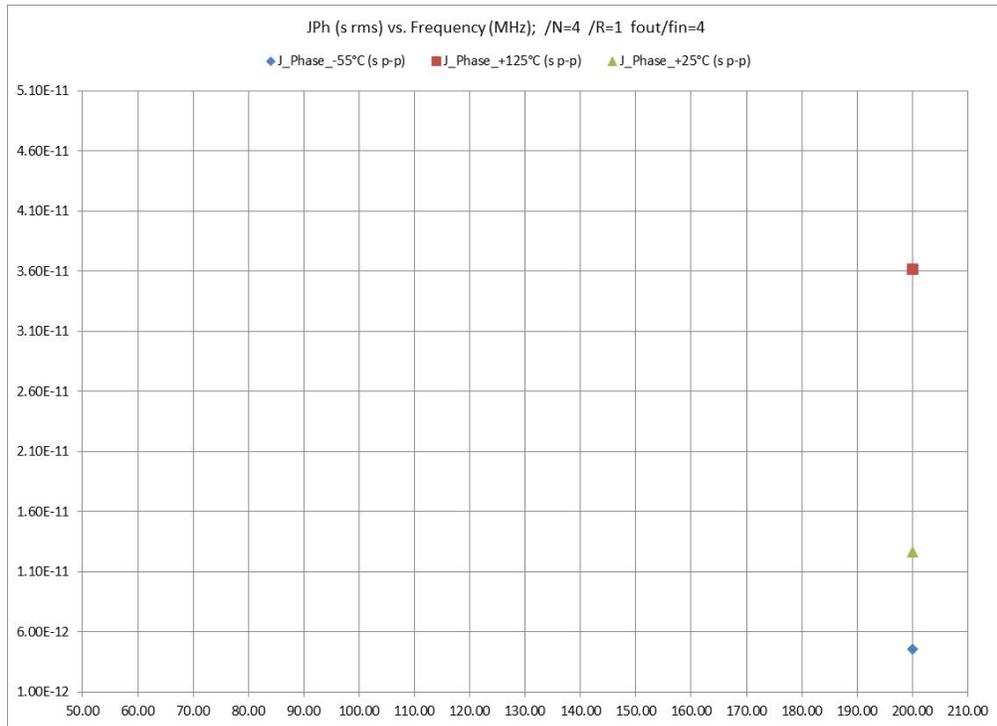**Figure 3.3.4.g: Phase or Random Jitter (J$_R$) vs. Output Frequency and PLL Divider Settings: /N=4, /R=1**

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3.3.5 Measured Data – Summary Table

Table 3.3.5.a: RadClock Measured Jitter Data Summary

DS1	DS0	FS	PD*/DIV	fin (MHz)	fout (MHz)	Divide Ratio	J_C2C_-55°C (s p-p)	J_C2C_+125°C (s p-p)	J_C2C_+25C° (s p-p)	J_Period_-55°C (s p-p)	J_Period_+125°C (s p-p)	J_Period_+25°C (s p-p)	J_Phase_-55°C (s rms)	J_Phase_+125°C (s rms)	J_Phase_+25°C (s rms)
M	M	L	H	50.01	50.01	1.0	5.50E-11	6.70E-11	5.70E-11	6.60E-11	6.30E-11	7.10E-11	1.46E-12	1.42E-12	2.21E-12
M	M	M	H	58.83	58.83	1.0	5.60E-11	6.30E-11	6.00E-11	7.00E-11	6.30E-11	6.90E-11	7.95E-12	2.35E-11	2.29E-11
M	M	M	H	76.94	76.94	1.0	5.10E-11	5.70E-11	5.20E-11	7.00E-11	6.90E-11	7.50E-11	1.91E-12	1.85E-12	2.98E-12
M	M	M	H	100.02	100.02	1.0	4.90E-11	5.60E-11	5.70E-11	8.00E-11	7.90E-11	7.60E-11	1.20E-12	1.19E-12	1.98E-12
M	M	H	H	100.02	100.00	1.0	5.30E-11	7.40E-11	5.20E-11	8.20E-11	6.60E-11	6.90E-11	4.67E-12	8.35E-12	1.02E-11
M	M	H	H	111.13	111.13	1.0	4.20E-11	5.40E-11	5.30E-11	7.20E-11	7.60E-11	6.70E-11	1.37E-11	2.07E-12	4.97E-12
M	M	H	H	125.02	125.02	1.0	5.10E-11	5.80E-11	6.30E-11	7.10E-11	7.60E-11	7.30E-11	1.05E-11	1.81E-12	5.31E-12
M	M	H	H	142.87	142.89	1.0	5.20E-11	7.30E-11	5.60E-11	8.00E-11	7.00E-11	6.90E-11	1.66E-12	1.43E-12	1.82E-12
M	M	H	H	166.69	166.68	1.0	6.40E-11	6.00E-11	6.50E-11	5.90E-11	5.80E-11	6.00E-11	4.83E-12	1.11E-12	1.80E-12
M	M	H	H	200.03	200.04	1.0	5.40E-11	5.70E-11	5.10E-11	6.70E-11	7.00E-11	7.00E-11	1.04E-12	3.89E-11	3.25E-12
L	L	M	H	50.01	100.01	2.0	5.50E-11	9.20E-11	6.40E-11	7.80E-11	7.60E-11	7.70E-11	1.15E-12	1.61E-12	2.13E-12
L	L	H	H	58.83	117.66	2.0	5.90E-11	1.01E-10	8.50E-11	8.00E-11	6.70E-11	8.30E-11	1.32E-11	2.05E-12	1.21E-11
L	L	H	H	76.94	153.88	2.0	7.20E-11	1.00E-10	6.50E-11	6.90E-11	8.10E-11	6.80E-11	1.58E-12	1.34E-12	3.05E-12
L	L	H	H	100.01	200.04	2.0	9.60E-11	6.10E-11	9.50E-11	7.20E-11	7.80E-11	6.80E-11	1.38E-12	2.67E-11	6.40E-12
L	M	H	H	50.01	150.02	3.0	9.40E-11	8.00E-11	1.03E-10	8.90E-11	7.60E-11	7.40E-11	2.05E-12	1.49E-12	6.75E-12
L	M	H	H	58.83	176.49	3.0	1.16E-10	9.60E-11	9.40E-11	7.00E-11	7.10E-11	7.60E-11	1.37E-12	1.49E-12	1.76E-12
L	H	H	H	50.01	200.03	4.0	7.90E-11	9.40E-11	8.50E-11	7.40E-11	8.60E-11	7.50E-11	4.56E-12	3.61E-12	1.26E-11
M	M	L	M	58.83	29.42	0.5	5.40E-11	5.80E-11	6.30E-11	6.00E-11	6.40E-11	7.00E-11	1.25E-11	1.40E-11	1.59E-11
M	M	L	M	76.93	38.47	0.5	5.00E-11	5.80E-11	6.10E-11	6.30E-11	6.70E-11	7.00E-11	4.77E-12	2.60E-12	7.53E-12
M	M	L	M	100.01	50.01	0.5	5.80E-11	6.80E-11	5.70E-11	6.30E-11	8.30E-11	6.90E-11	2.04E-12	1.96E-12	2.44E-12
M	M	M	M	111.13	55.56	0.5	4.50E-11	5.70E-11	4.70E-11	6.20E-11	6.50E-11	5.90E-11	1.75E-11	1.97E-11	1.91E-11
M	M	M	M	125.02	62.51	0.5	5.40E-11	5.50E-11	5.20E-11	7.40E-11	6.60E-11	6.70E-11	1.31E-11	1.08E-11	1.26E-11
M	M	M	M	142.88	71.44	0.5	5.30E-11	7.70E-11	6.50E-11	7.90E-11	7.40E-11	6.80E-11	7.55E-12	2.43E-12	7.85E-12
M	M	M	M	166.69	83.35	0.5	4.80E-11	5.50E-11	5.30E-11	5.90E-11	6.70E-11	6.60E-11	4.27E-12	1.56E-12	2.71E-12
M	M	M	M	200.03	100.02	0.5	5.50E-11	6.30E-11	6.00E-11	7.10E-11	7.20E-11	7.10E-11	2.11E-12	1.35E-12	1.82E-12
L	L	L	M	50.01	50.01	1.0	4.90E-11	5.90E-11	5.40E-11	7.00E-11	6.70E-11	6.70E-11	1.48E-12	1.46E-12	1.78E-12
L	L	M	M	58.83	58.83	1.0	5.80E-11	5.80E-11	5.20E-11	6.50E-11	6.60E-11	6.90E-11	2.13E-11	2.44E-11	1.87E-11
L	L	M	M	76.93	76.93	1.0	6.20E-11	7.30E-11	6.60E-11	7.00E-11	8.10E-11	7.30E-11	1.87E-12	1.77E-12	8.66E-12
L	L	M	M	100.01	100.01	1.0	5.90E-11	7.90E-11	6.60E-11	7.80E-11	7.50E-11	7.80E-11	1.23E-12	1.22E-12	2.02E-12
L	L	H	M	111.13	111.13	1.0	6.30E-11	7.20E-11	5.40E-11	6.70E-11	7.60E-11	8.50E-11	1.51E-11	2.11E-12	1.38E-11
L	L	H	M	125.01	125.01	1.0	4.60E-11	7.60E-11	7.40E-11	7.90E-11	7.50E-11	8.40E-11	1.05E-11	1.74E-12	5.04E-12
L	L	H	M	142.89	142.87	1.0	8.10E-11	6.50E-11	6.70E-11	8.30E-11	7.70E-11	7.80E-11	5.68E-12	1.45E-12	7.62E-12
L	L	H	M	166.68	166.68	1.0	5.70E-11	8.70E-11	6.60E-11	6.00E-11	6.20E-11	7.20E-11	2.82E-12	1.09E-12	1.63E-12
L	L	H	M	200.02	200.04	1.0	9.20E-11	6.50E-11	8.70E-11	7.00E-11	7.40E-11	6.20E-11	1.06E-12	4.77E-11	5.01E-12

4.0 Summary and Conclusion

This Application Note (AN) provides an overview of clock jitter principles, including definitions and general measurement methods. The main purpose of this AN is to present measured jitter data for the UT7R995/C RadClock for customers.
These data include time domain Cycle-to-Cycle jitter (J_{C2C}) and Period Jitter (J_{PER}) from oscilloscope measurements, and Phase or Random jitter (J_R) derived from frequency domain phase noise (PN) measurements.

The UT7R995/C RadClock 2.5V/3.3V 200 MHz High-Speed Multi-Phase PLL Clock Buffer simplifies system design by providing low jitter outputs with adjustable phase and frequency to meet a variety of clock requirements. The time and frequency domain jitter data presented in this AN gives the user additional product information for the UT7R995/C RadClock that is complementary to the data sheet and facilitates customer clock designs.

1/21/2016

REVISION HISTORY

Date	Rev. #	Change Description
01/21/2016	1.0.0	New

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