# Recommended Bypass Capacitance Values for the $V_{DD}$ Pins of the UT7R995/C RadClock™

## 1.0 Overview

The UT7R995 and UT7R995C RadClock are clock buffers with PLL capable of independently driving four banks of outputs to 200 MHz with programmable skews relative to the feedback input. The devices consist of independent power supplies for the core and for each of the four output banks. VDD powers the core, which consists of the PLL, the clock circuitry, and the control logic. There are also independent power supply pins for each output buffer designated as $V_{DD}Qn$ ($n$:1-4). The purpose of this application note is to characterize typical current requirements for each power supply and to provide recommended bypass capacitors.

The core and the four output drivers are independent and electrically isolated. Also, the structure of the four output drivers is the same. Therefore, it is sufficient to characterize IDD and one output driver supply $I_{DD}Qn$, where $n$ is either 1, 2, 3 or 4. Channel 3 is selected as the output.

## 2.0 Lab Setup

In order to characterize the bypass requirements for each $V_{DD}$ pin, it is first necessary to characterize $I_{DD}$ and $I_{DD}Q3$ under controlled conditions. These conditions are captured in Table 1.

**Table 1: RadClock Test Configuration**

| Parameter | Value |
|---|---|
| Input Frequency | 25 MHz |
| PLL Frequency | 50 MHz, 100 MHz, 150 MHz |
| Load | 25pF |
| Output Drive Level | 24mA |
| $V_{DD}$ | 3.3V |
| $V_{DD}Q3$ | 3.3V |
| Temperature | 25ºC |

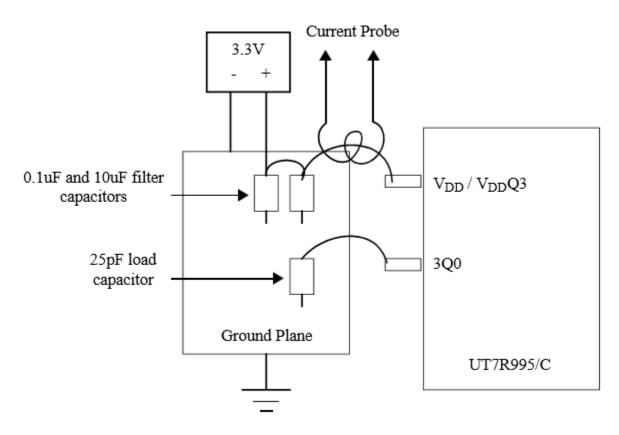# Recommended Bypass Capacitance Values for the $V_{DD}$ Pins of the UT7R995/C RadClock™

The laboratory setup is shown in Figure 1. One side of the 25pF load capacitor is tied to $V_{DD}Q3$, with the other side soldered to the copper ground plane as shown. To measure $I_{DD}$ or $I_{DD}Q3$, several capacitors are tied close to the input pins to ensure there is adequate charge needed to supply the ac component of the current. An ac-coupled current probe is used to monitor the ac component of $I_{DD}$ or $I_{DD}Q3$.

**Figure 1. Laboratory Setup for Current Characterization.**



In the case where $I_{DD}$ is being measured, $V_{DD}Q3$ is connected normally through the power plane in the PCB. Like- wise, when $I_{DD}Q3$ is being measured, $V_{DD}$ is connected to 3.3V through the PCB. For the $I_{DD}$ measurement, all $V_{DD}$ pins are tied together.

## 3.0 Lab Results

The input frequency to the UT7R995/C is 25 MHz. The output frequency is set to 50 MHz, 100 MHz, and 150 MHz using the internal PLL divider. Worst-case current for $I_{DD}Q3$ occurs at an output frequency of 50 MHz. Figure 2 shows the supply current in the top trace where the scale is 5mV/mA. The bottom trace is the output voltage 3Q0, shown for reference. As a first-order approximation, $I_{DD}Q3$ will be modeled as a 100 MHz sine wave. The doubling of frequency in the current waveform relative to the output voltage is due to reflections caused by the capacitive load, as no attempt is made to match the source impedance to the load. The peak-to-peak current is 100mA.
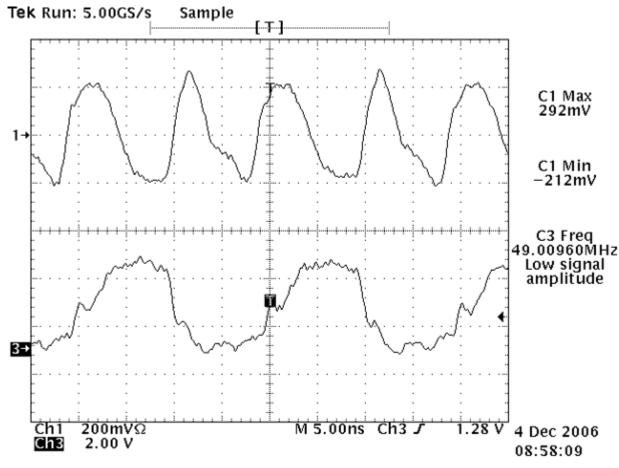


**Figure 2. $I_{DD}Q3$ and Output Voltage for Channel 3Q0.**

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For the core power supply, worst-case $I_{DD}$ occurs at an output frequency of 150 MHz. Figure 3 shows $I_{DD}$ in the top trace where the scale factor is 1mV/mA. The bottom trace is the output voltage 3Q0, shown for reference. The peak- to-peak current is 53mA, and is approximated as a sine wave at 150 MHz.
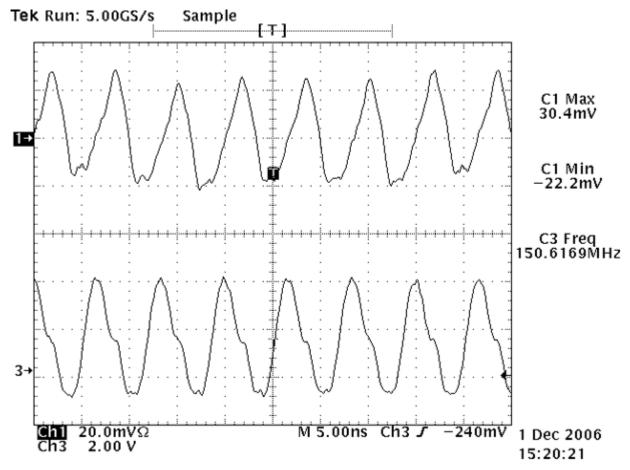


**Figure 3. $I_{DD}$ and Output Voltage for Channel 3Q0.**

## 4.0 Simulation Results

The voltage seen at the supply pin is derived by simulating a circuit using the models for the current waveforms shown in Section 3.0. The voltage source is an ideal 3.3V dc source separated from the UT7R995/C power pins by 15cm traces represented by a 150nH inductor and 25m$\wedge$ resistor on both sides of the power supply. This represents a worst-case scenario where there is no ground plane and where the voltage regulator is located some distance from the UT7R995/C. A capacitor is placed directly on the power pin whose ESR is determined by assuming a 2.5% dissipation factor, typical for ceramic multi-layer chip capacitors. The circuit is simulated and the ripple voltage on the power pin is determined. Tables 2 and 3 show the ripple voltage with several different capacitor values.

**Table 2: Peak-to-Peak Ripple Voltage for $V_{DD}Q3$**

| Capacitance | ESR | Ripple Voltage (Vp-p) |
|---|---|---|
| 0.001uF | 40m$\wedge$ | 140mV |
| 0.01uF | 4m$\wedge$ | 10mV |
| 0.1uF | 0.4m$\wedge$ | 1.6mV |

**Table 3: Peak-to-Peak Ripple Voltage for $V_{DD}$**

| Capacitance | ESR | Ripple Voltage (Vp-p) |
|---|---|---|
| 0.001uF | 26m$\wedge$ | 55mV |
| 0.01uF | 2.6m$\wedge$ | 5.5mV |
| 0.1uF | 0.26m$\wedge$ | 0.6mV |

## 5.0 Conclusion

In order to minimize ripple voltage, a 0.1uF capacitor should be placed on each $V_{DD}$ and $V_{DD}Qn$ input, as close to the pin as possible. $V_{DD}$ pins that are close together may share a bypass capacitor, but $V_{DD}$ should be isolated from the $V_{DD}Qn$ inputs. Use of the recommended bypass capacitors will reduce only the ripple voltage due to the ac com- ponent of the supply current. The designer should use additional filtering as required to reduce the coupling of transients within the system or due to neighboring components.

APPLICATION NOTE

1/1/2007