Calculating Power Dissipation Capacitance for the UT54ALVC2525 Clock Buffer

APPLICATION NOTE

1. Overview

This document calculates the dynamic power dissipation capacitance for the UT54ALVC2525 Clock Driver. To focus specifically on the capacitive power dissipation of the UT54ALVC2525, this analysis removed output loading to eliminate the capacitive load power dissipation and forced fast input edge rates to reduce internal shoot through currents to a minimal value. With these constraints, essentially all of the measured AIDD current results from the internal power dissipation capacitance (C_{pd}) of the device. Knowing this, the designer can now accurately determine the total power dissipation of the UT54ALVC2525 Clock Driver by summing internal power dissipation capacitance (C_{pd}) developed in this application note with the actual capacitive load dissipation of their specific application.

The UT54ALVC2525 is a low-voltage CMOS, minimum skew, one-to-eight clock driver. The UT54ALVC2525 distributes a single clock to eight, high-drive outputs with low skew across all outputs during both the t_{PLH} and t_{PHL} transitions, making it ideal for signal generation and clock distribution. Since the UT54ALVC2525 is a critical component for clock and signal distribution, calculating its' power dissipation is an important aspect of system power supply and thermal management design. Total power consumption has several components. This document calculates dynamic power-dissipation capacitance (C_{pd}) for the UT54ALVC2525 and shows how it contributes to the total power consumption of this device.

The two components of total power consumption for CMOS devices such as the UT54ALVC2525 are static power consumption (P_S) and dynamic power consumption (P_D) . The relationship between P_S and P_D is expressed in Equation 1:

Equation 1

$$P_{Total} = P_S + P_D$$

Equation 2

$$P_D = P_T + P_L = (C_{pdD} * V^2 * f_I) + (C_L * V_{OUT\text{-}PP}^2 * f_O * N_{SW})$$

Where:

P_D = dynamic power consumption
P_T = transient power consumption
P_L = capacitive-load power consumption
C_{pd} = internal dynamic power dissipation capacitance
V_{DD} = supply voltage
f_I = input frequency
C_L = output load capacitance
$V_{OUT\text{-}PP}$ = output voltage swing (peak-peak)
f_O = output frequency
N_{SW} = number of outputs switching

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The transient power consumption (P_T) results from currents flowing within the device when internal transistors switch states during operation. This includes both the actual switching currents required to charge the internal nodes and the shoot-through or crowbar currents that flow through a CMOS device when both p-channel and n-channel transistors briefly conduct during switching. The frequency at which the device switches, as well as the rise and fall times of the switching signals, has a direct effect on the transient power dissipation. For fast rise and fall times, the shoot-through cur- rents are small compared to the switching currents required to charge the internal nodes. For this analysis, we use a1ns rise/fall time for the input reference clock to minimize these shoot-through currents. Thus, the switching of the internal capacitance of the device, known as the dynamic power dissipation capacitance (C_{pd}), determines the UT54ALVC2525 transient power dissipation.

The capacitive load portion (P_L) of the dynamic power consumption (P_D) results from actively charging and discharging output capacitive loads. This depends on the external loading and the switching frequency of the output drivers. To calculate capacitive load power dissipation, the user must determine the number of outputs switching, their frequency of operation and the actual peak-peak switching voltage at each load. Since the purpose of this analysis is to determine the internal, dynamic power dissipation (C_{pd}) for the UT54ALVC2525, we use a characterization board with output pins lifted so the load capacitance on each output (C_L) is negligible. This removes the capacitive load portion of the dynamic power dissipation, leaving only the transient power dissipation defined by the dynamic power dissipation capacitance in Equation 2. The short pins also ensure no reflections or "ringing" on the output signals that would increase the measured currents.

The remaining discussion uses this reduced equation for power dissipation to calculate C_{pd} for the UT54ALVC2525. Equation 3 shows the dynamic power dissipation solved to calculate C_{pd}.

Equation 3

$P_D = P_T + P_L = P_T = (C_{pd} * V_{DD}^2 * f_I)$: for fast input rise/fall and $C_L \approx 0pF$

$P_D = (V_{DD})*(I_{DD}) = (C_{pd} * V_{DD}^2 * f_I)$

$C_{pd} = (V_{DD} * I_{DD}) / (V_{DD}^2 * f_I)$

$C_{pd} = I_{DD} / (V_{DD} * f_I)$

2. Technical Data

To determine C_{pd} in the laboratory, measure the I_{DD} supplied to the device across its frequency range of operation, then calculate an average I_{DD} / f_I slope. The data in Table 2 lists this active current (AIDD), measured versus frequency for the UT54ALVC2525. AIDD values are from maximum measurements taken during characterization of a single UT54ALVC2525 device configured under the following conditions. Each set of data points calculates an AIDD/frequency slope. The data and corresponding AIDD/frequency slopes appear in Figure 1. Table 1 summarizes an average value for C_{pd} at each of the three temperatures. Please note the listed conditions for the lab characterization.

Device: UT54ALVC2525

Temperature: T_C = 25°C, +125°C, -55°C,
Voltage: V_{DD} =3.3 V
Frequency: f =1MHz, 25MHz, 50MHz, 75MHz, 100MHz, 125MHz, 150MHz, 175MHz, 200MHz

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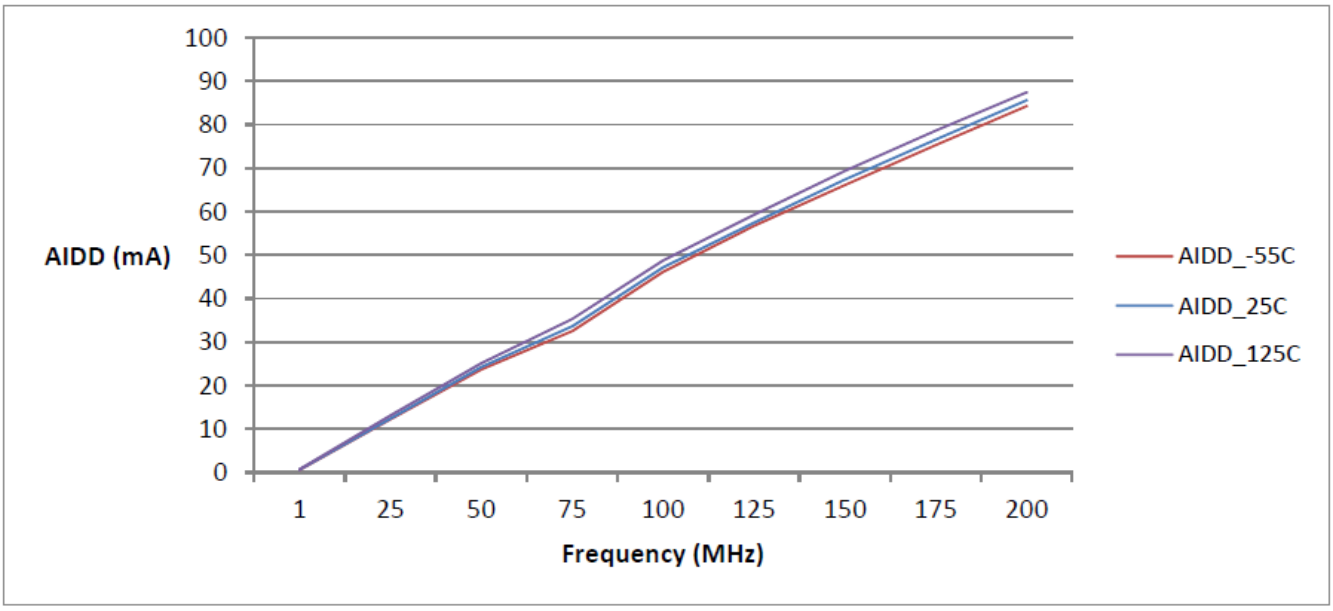
Table 1: UT54ALVC2525 C_{pd} Characterization Data

	Frequency (MHz)	AIDD (mA) -55°C	Slope (mA/MHz)	AIDD (mA) 25°C	Slope (mA/MHz)	AIDD (mA) 125°C	Slope (mA/MHz)
UT54ALVC2525 Clock Buffer Vdd= 3.3V Inputrise/falltime<1ns $C_{L(eff)}$=0pF	0	0.054		0.047		0.044	
	1	0.592		0.624		0.710	
	25	12.19	0.483	12.37	0.489	13.11	0.517
	50	23.68	0.460	24.24	0.475	25.12	0.480
	75	32.46	0.351	33.57	0.373	35.28	0.406
	100	46.13	0.547	47.17	0.544	48.73	0.538
	125	56.66	0.421	57.41	0.410	59.26	0.421
	150	66.05	0.376	67.33	0.397	69.33	0.403
	175	75.25	0.368	76.55	0.369	78.61	0.371
	200	84.25	0.360	85.57	0.361	87.40	0.352
Slope Average (mA/MHz)			0.421		0.427		0.436
C_{pd} (pF)			127.487		129.448		132.131

Figure 1.1 UT54ALVC2525 Characterization Plots: AIDD vs. Frequency



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