UT81NDQ512G8T
NAND System Information

Table 1: Cross Reference of Applicable Products

PRODUCT NAME	MANUFACTURER PART NUMBER	SMD #	DEVICE TYPE
4Tb NAND Flash	UT81NDQ512G8T	N/A	N/A

1 OVERVIEW

This App Note covers the NAND system hierarchy and highlights what is available from CAES and what is needed from the user.
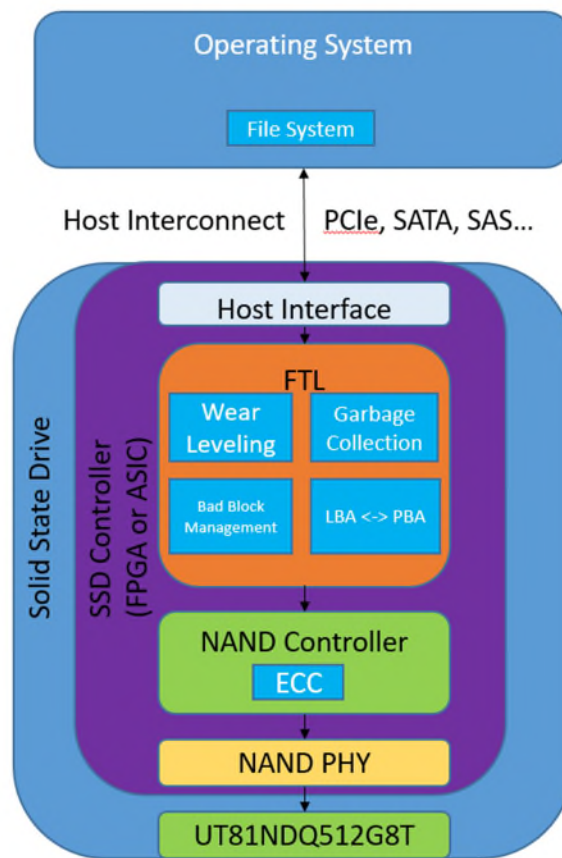
2 NAND SYSTEM OVERVIEW

Figure 1: SSD example

Flash Translation Layer (FTL)

This block handles several critical NAND Flash management services. It requires supporting DRAM buffer memory and non-volatile memory to hold metadata for the logical to physical address mapping. Typically this requires 1MB of non-volatile memory for every 1GB of NAND Flash memory. Non-volatile memory allows for recovery of operations during a power outage situation without losing address mapping, bad block, and block wear information.

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NAND Controller

This block handles commands to the NAND such as erase, program, read, and status. The controller also generates and decodes the ECC. The ECC codes are stored on the physical NAND.

PHY

This block provides the interface between the controller and the physical NAND and should support the interface modes of the NAND. Most PHY's support ONFi standards. It is recommended to check which version of ONFi the PHY supports. This will ensure that the maximum speeds of the NAND is supported as well as advanced features such as multi-plane and interleaving commands.

NAND Flash

This is the physical memory to which the PHY interfaces and the controller talks to. It is recommended to use an ONFi compliant part. There are several interfaces that the ONFi spec defines such as Asynchronous and NV-DDRx. Designs should take into account the speed requirements of the system and select the interface to will support those needs. Some interfaces have voltage restrictions on the I/O. Please check your part datasheet for those types of restrictions.

3   CAES OFFERINGS

NAND Controller

CAES offers a NAND controller with ECC correction for SLC mode. A fully ONFi 4.0 compliant controller will be available in a future release, and will include support for TLC mode and LDPC correction. The controller has a flag output to notify the user when a SEFI occurs. The controller can be found here:
https://www.gaisler.com/index.php/products/ipcores/nand-flash-memory-controller-with-dma

PHY

A reference NAND PHY will also be available for customers. The PHY will not have performance guarantees but can be used as a starting point for users to customize to their operating and hardware requirements.

NAND Flash

CAES offers a NAND memory standard product. It is a radiation tolerant 4Tb memory that supports both triple level cell (TLC) and single level cell (SLC) modes. NV-DDR2, NV-DDR3, and Asynchronous interfaces are available with a maximum data rate of 667 MT/sec. A summary of radiation performance is available upon request. Additional information for the UT81NDQ512G8T can be found here:
https://frontgrade.com/product/ut81ndq512g8t

Application Note

5   REVISION HISTORY

Date	Revision	Change Description
01/2023	1.0	Initial Release

The following United States (U.S.) Department of Commerce statement shall be applicable if these commodities, technology, or software are exported from the U.S.: These commodities, technology, or software were exported from the United States in accordance with the Export Administration Regulations. Diversion contrary to U.S. law is prohibited.

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