Application Note

Using NAND Basics

Table 1: Cross Reference of Applicable Products

PRODUCT NAME	MANUFACTURER PART NUMBER	Die Source
4Tb TLC NAND Flash	UT81NDQ512G8T	Micron B17A industrial

1 Overview

This document covers the basics of NAND features and consideration in using NAND. Covered in this app note are Cell Modes, Part Interface, Error Correction, Endurance & Data Retention, Mirroring, and Controllers.

2 SLC and TLC ENDURNACE and Density

UT81NDQ512G8T is a Triple Level Cell (TLC) device with 3 bits per cell. NAND can be setup to run either in the intrinsic bits per cell or in SLC, 1 bit per cell. To calculate the SLC density, divide the array by intrinsic number of bits per cell. For UT81NDQ512G8T, it uses a TLC cell and to calculate the SLC array size, divide by 3. Running in SLC mode increases device program/erase (PE) cycles. Typical PE cycles are specified as 3000 in TLC mode and 40,000 in SLC mode. This gives the user flexibility to adjust the part performance to address system's more critical requirements, P/E cycles vs. density. It should be noted that after performing 10% of the P/E cycles, the cell mode cannot be changed.

3 Data Retention

The UT81NDQ512G8T is tested per JESD47 for data retention. NAND uses floating gate or charge trapping technology to store information. Higher temperatures will affect the data retention of the NAND cell. Retention time decreases exponentially with increasing temperature. The increase in temperature causes more electrons to leak off of a floating gate and leads to data loss.

4 Interface

The UT81NDQ512G8T supports three different interfaces: asynchronous, NV-DDR2, and NV-DDR3. The maximum performance of each interface is 50 Mega transfers per second (MT/s), 533 MT/s, and 667 MT/s, respectively. For speeds above 200MT/s, differential signaling is required. On die termination is supported by the part to impedance match the signal paths.

The asynchronous and NV-DDR2 interfaces use an I/O voltage of 1.8V. The NV-DDR3 interface uses a voltage of 1.2V. The default interface at initial power up is asynchronous for 1.8V I/O supply and NV-DDR3 for 1.2V I/O supply. The part can switch from the asynchronous to NV-DDR2 interface using the SET FEATURES command.

5 Error Correction

NAND Flash requires ECC to ensure data integrity. ECC has been used for many years in RAM modules as well as in many other types of storage. ECC can be used in any device that may be susceptible to data errors. The NAND Flash memory includes a 2,208 byte spare area for extra storage on each page (16,384 bytes). This spare area can be used to store the ECC code as well as other software information, such as wear-leveling or logical-to-physical block-mapping information. ECC can be performed in hardware or software; however, hardware implementation provides a performance advantage.

During a programming operation, the ECC unit calculates the ECC code based on the data stored in the sector. The ECC code for the data area is then written to the corresponding spare area. When the data is read out, the ECC code is also read out, and the reverse operation is applied to check that the data is correct. It is possible for the ECC algorithm to correct data errors. The number of data errors that can be

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corrected depends on the correction strength of the algorithm used. The inclusion of ECC in hardware or software provides a robust solution at the system level.

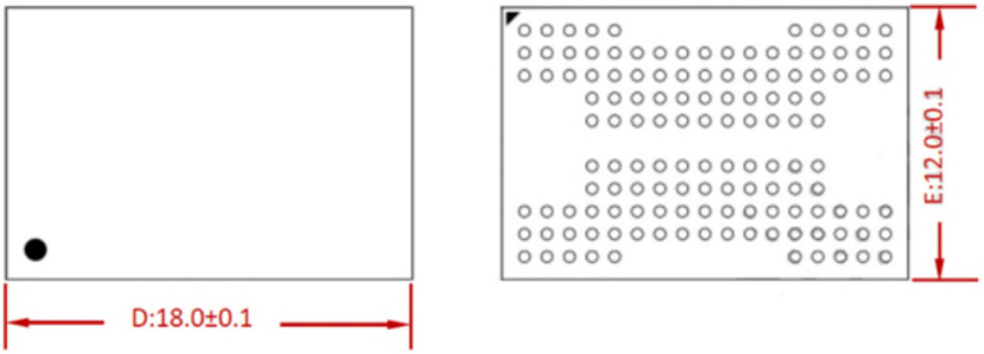
This NAND device requires 60-bit ECC per 1162 bytes of data for SLC mode and a Low Density Parity Check (LDPC) algorithm to correct 1e-2 RBER or better error correction scheme is required for TLC mode.

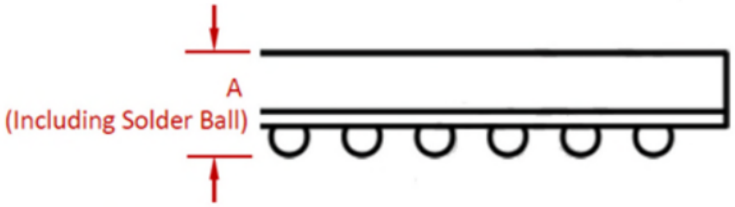
5.1 Bad Block Information

Each block within the part will have a marking at the first spare location of the first page (Byte 16,384) guaranteed, and all locations if possible. If the block is good, the bad block location will read out FFh. If the block is bad, there will be manufacturer specific mark, 00h in the case of the UT81NDQ512G8T. In the first block, there will be a summary of the bad blocks in the array.

6 Packaging

The UT81NDQ512G8T is an ONFi compliant 132 ball plastic BGA.





Symbol (Dimension)	Min	Norm	Max
A (Total Thickness)	1.25	1.35	1.45
D (Lenth)	17.90	18.00	18.10
E (Width)	11.90	12.00	12.10
Ball Pitch	1.0 mm Typical		
Ball Diameter	0.45 mm Typical		

Notes:
1) All Dimensions in mm
2) Solder ball material: Sn-Pb
3) Package Mass: 0.534 grams

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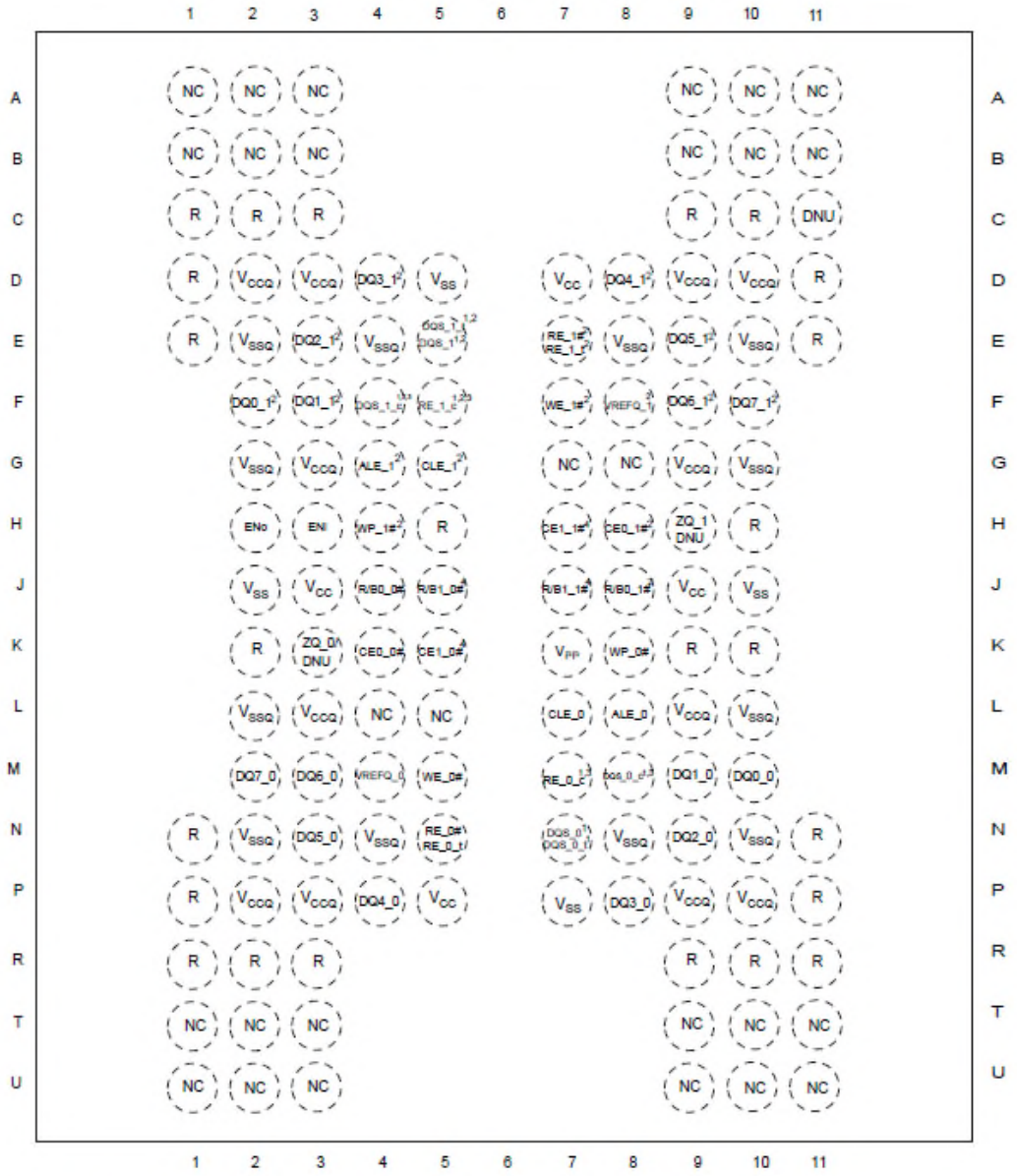

Notes:
1. N/A: This signal is tri-stated when the asynchronous interface is active.
2. These signals are available on dual, quad, and octal die stacked die packages. They are NC for other configurations.
3. These signals are available when differential signaling is enabled.

7 ELECTRONIC MIRRORING

Electronically mirrored DQ[7:0] pinout is available in order to assist in optimizing printed circuit board (PCB) layout by assisting two-sided (clamshell) designs; reducing the complexity and the number of signal routing layers between the top and bottom side of the PCB. This ability for electronic mirrored DQ[7:0] pinout also assists in reducing the vertical profile of a two-sided system. Only the DQ[7:0] signals have the ability to be changed by electronic mirrored functionality, all other NAND signals remain consistent.

See Figures 1 and 2 as examples of how packages in the default non-mirrored DQ[7:0] pinout and the mirrored DQ[7:0] pinout could be used in a two-sided PCB system.

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Figure 1: Example PCB Layout of a Two-Sided System Without Electronic Mirroring of DQ[7:0]

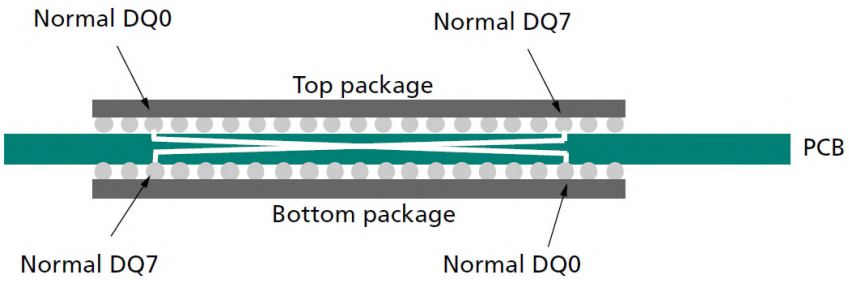
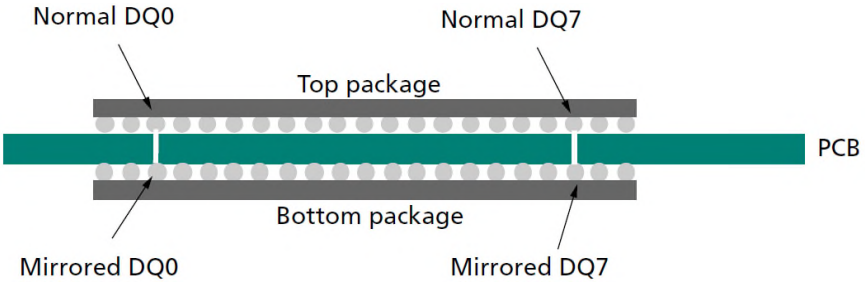


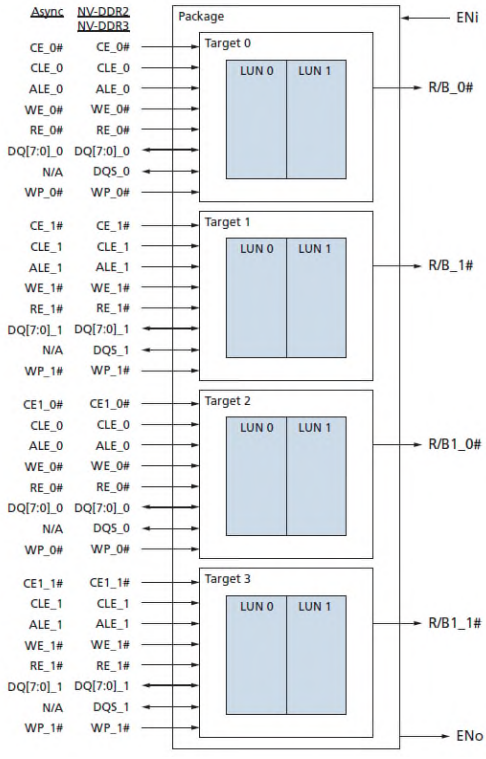
Figure 2: Example PCB Layout of a Two-Sided System With Electronic Mirroring of DQ[7:0]



The mirror and non-mirrored packages are physically the same with same internal bond connections, but based on how first issued command after device initialization is decoded, the LUNs internally are electrically configured to be non-mirrored or mirrored. See Micron B17A Industrial Datasheet for additional details.

8 Device Organization

The UT81NDQ512G8T is organized as 4 targets with 2 LUNs per target. A LUN is a NAND die.



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Each LUN has 4 planes. Each plane has 504 blocks. Each block has 2304 pages. Each page is made up of 16,384 + 2208 bytes. Multiplying all of these together results in 690.85GB of storage within the device.

9 Addressing

The UT81NDQ512G8T uses NAND Flash electrical and command interfaces. Data, commands, and addresses are multiplexed onto the same pins and received by I/O control circuits. The commands received at the I/O control circuits are latched by a command register and are transferred to control logic circuits for generating internal signals to control device operations. The addresses are latched by an address register and sent to a row decoder to select a row address or to a column decoder to select a column address.

10 Reading (NOR vs NAND vs SRAM)

Traditional NOR and SRAM have separate address and data pins. To read from those parts, an address is applied to the address pins and control signals toggled to get data. For NAND, the address has to be latched into the part using a column, row, and block address. To keep the pin count low, the DQ pins are used for both input and output. It takes multiple command cycles to get data out of the part. Data is READ/WRITTEN from/to the device as a contiguous data stream the size of an entire page through the device's onboard cache register.

11 Controller

The NAND controller is required to manage bad blocks, wear leveling, garbage collection, and data randomization. In order to minimize the effects of the limited program/erase endurance of Flash cells, and maximize the lifetime of the Flash, the controller uses wear levelling to ensure that all blocks are used evenly. This means that the controller must select the least used page from a pool of unused blocks when writing data. Again, there are several methods that can be used with different trade-offs for effectiveness and processing performance.[1]

The controller also needs to manage bad blocks over the life of the part. It must read and store bad block information at initial use. Additionally, it must be able to identify when a block becomes bad and adds it to the bad block table.

The controller will also need to perform data randomization. One of the primary objectives of performing data randomization is to prevent structured data patterns from getting programmed into the NAND array. The reliability of the NAND is not guaranteed if a structured data pattern is programmed into the NAND array. Important to note that multiple pages that are skipped or not fully programmed in terms of full page length may also constitute a structured data pattern. To avoid a structured data pattern the user must program randomized data to the entire page length even if beyond the user data.

Refer to https://caes.com/product/ut81ndq512g8t for the NAND page and controller cross reference information.

1/ https://www.electronicspecifier.com/industries/industrial/controller-importance-in-nand-flash-storage-systems

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Cobham Semiconductor Solutions – Application Note Revision History

Date	Revision	Change Description
09/01/2020	1.0.0	Initial Release
11/24/2020	1.0.1	Fixed formatting errors and added missing figure numbers in section 7
12/2022	1.1	Updated package dimensions figure; Updated app note to latest template; Updated hyperlink to NAND product page