PRODUCT NAME	MANUFACTURER PART NUMBER	DEVICE TYPE
Lattice Certus-NX-RT FPGA	UT24C407	RL01

**Table 1: Cross Reference of Applicable Products** 

#### 1.0 Overview

This document details the process of debugging a **Certus-NX-RT** FPGA project using the **Lattice ModelSim**. For the purposes of this document, create a project named **counter\_sim\_debug** and configure **ModelSim** to include all the source modules required for a successful build. Using this template, projects are created using (a) the preferred application source directory structures and (b) the directory structure for the **Lattice Radiant**-supplied files. **Figure 1** shows the counter simulation.



Figure 1: An Example ModelSim Wave

### 2.0 Creating a Project

1. Copy **Mentor Graphics** example files from **Lattice Radiant** installation directory: <installation dir>\modeltech\examples\tutorials\verilog\basicSimulation

To:

<project dir>\Lattice\applications



Launch Lattice ModelSim 
 Click Jumpstart to create a project, see Figure 2.

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Figure 2: ModelSim-Lattice Project Creation

4. Specify the project name as **counter\_sim\_debug**, navigate to the **Project Location** of your choice and click **OK**, see **Figure 3**.

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Figure 3: Naming the Project

5. Click **Add Existing File** and add **counter.v** and **tcounter.v** from <project dir>\Lattice\basicSimulation, see **Figure 4**.

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Figure 4: Adding Files to the Project

6. Form the top menu, select **Compile > Compile All** to compile **tcounter.v** and **counter.v**, see **Figure 5**.

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Figure 5: Compiling the Project

7. Form the top menu, select **Simulate > Start Simulation...** and select **test\_counter.v** in the work library and click **OK**, see **Figure 6**.

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Figure 6: Starting a Simulation

### 3.0 Running the Simulation

### 3.1 Simulating Signals

8. From the **Objects** window, choose the top-level signals and drag them over to the **Wave** window. **Run** for 100 nanoseconds and the **Wave** window will display the timing diagram of the signals. Click **Zoom Full** to see the full picture, see **Figure 7**.



#### Figure 7: Zooming on the ModelSim Waveform

#### 4.0 Debugging HDL Code

- 9. In the Transcript window, enter: edit counter.v
- 10. The **counter.v** file opens next to or over the **Wave** window, see **Figure 8**.



Figure 8: Debugging HDL Code

11. **ModelSim** allows to debug the **HDL** code with break points and stepping through the code. Double click on line 40 or right-click on it and select **Set Breakpoint**; the debugger sets a breakpoint at line 40, see **Figure 9**.



Figure 9: Setting a Breakpoint



Figure 10: Stepping Around a Breakpoint

#### 5.0 **REVISION HISTORY**

Date	Rev. #	Author	Change Description			
3/18/2022	1.0.0	JA	Initial Release.			
4/21/23	1.0.1	JB	Document reformatted to match Frontgrade template.			

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