Creating Certus-NX-RT Project in Radiant Software

PRODUCT NAME	MANUFACTURER PART NUMBER	DEVICE TYPE
Lattice Certus-NX-RT FPGA	UT24C407	RL01

Table 1: Cross Reference of Applicable Products

1.0 Overview

This document details the process of creating a **Certus-NX-RT** FPGA project using the **Lattice Radiant** software tools and the Lattice Certus-NX Versa Evaluation board LFD2NX-VERSA-EVN.

For the purposes of this document, create a project named **led_brightness** and configure the **Radiant** tools to include all the source modules required for a successful build.

Using this template, projects are created using:

(a) the preferred application source directory structures and
(b) the directory structure for the **Radiant**-supplied files.

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Figure 1 shows the block diagram of the design, it includes:

- the DIP switch inputs DIP_SW[4:1] which control the duty cycle to the PWM output, which in turn controls the brightness to LED[0]
- the LED[7:0] outputs controlled by 7 bits of the design's internal 32-bit counter "count" and are used to show the heartbeat of the system. The counter's bits [30:24] drive the LED[7:0]
- the S_SEG[7:0] outputs are also controlled by 4 bits of the internal 32-bit counter "count" and are used to drive the board's 7-segment LED device. Specifically, the counter's 4 bits [30:27] are decoded in such a way as to drive the 7-segment LED display's control signals S_SEG[7:0] as a hexadecimal counter with the decimal point LED also being turned on whenever the count value equals F hex.

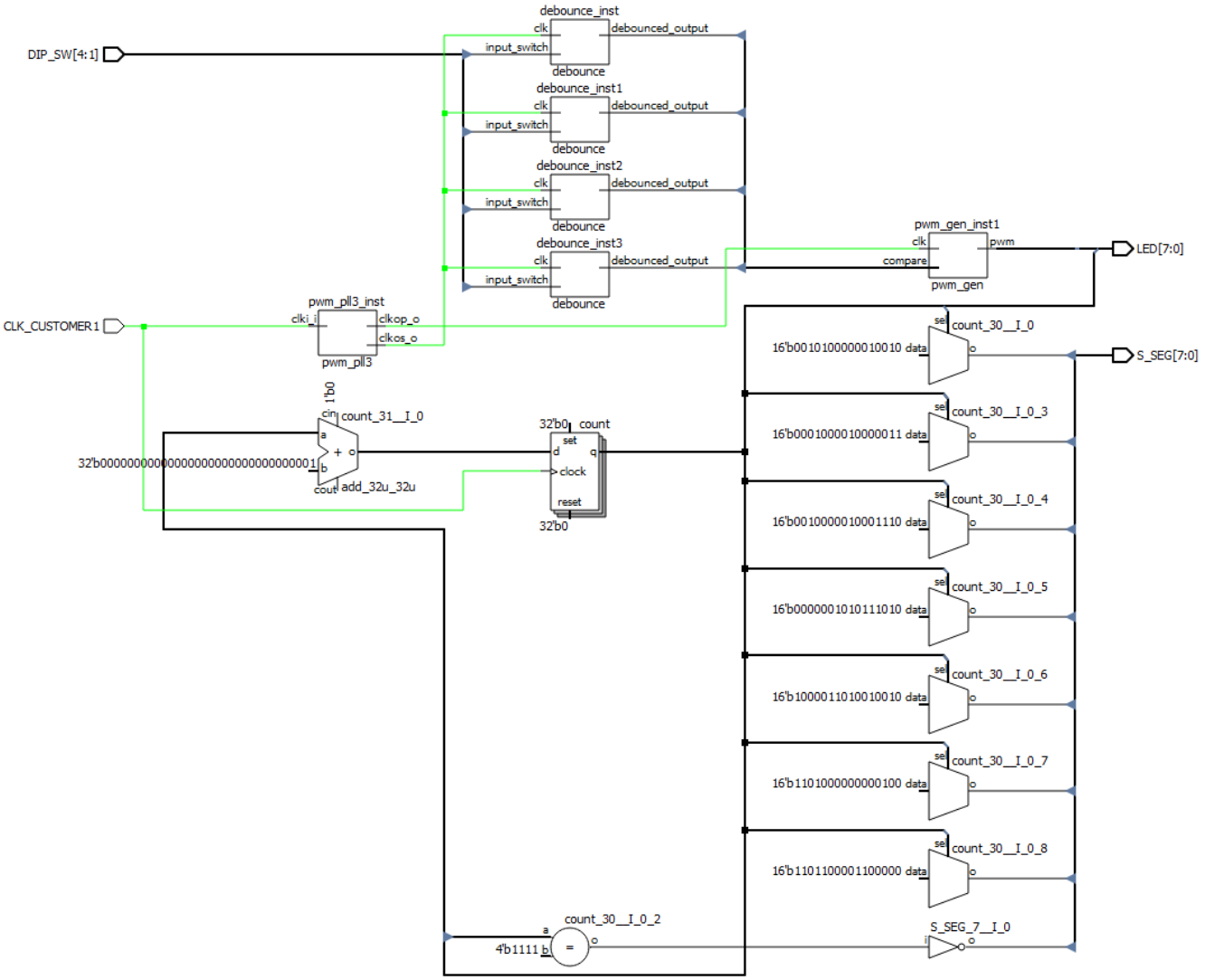

Figure 1: An Example Netlist View

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3.0 Creating a Design Project with Radiant Software

1. Download CreatingRadiantProject.zip from caes.com.
2. Launch Radiant Software
3. From the **File** menu, select **New > Project...**.
4. Specify the project name as **led_brightness**, navigate to the **location** of your choice and click **Next**, see **Figure 2**.

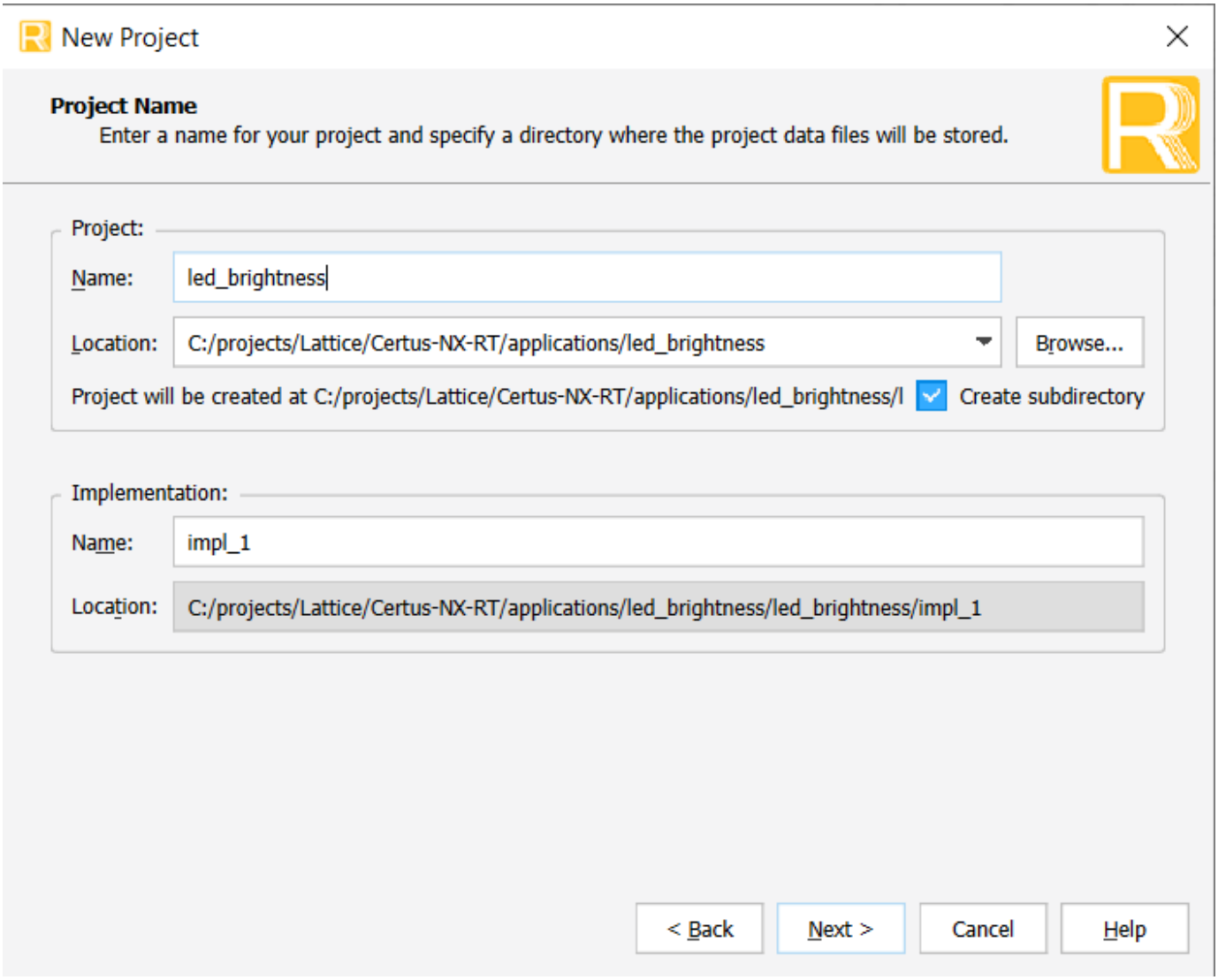

Figure 2: Creating a Radiant Design Project

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5. Select **Add Source...** and click **Open**, see **Figure 3** and **Figure 4**, click **Next**.

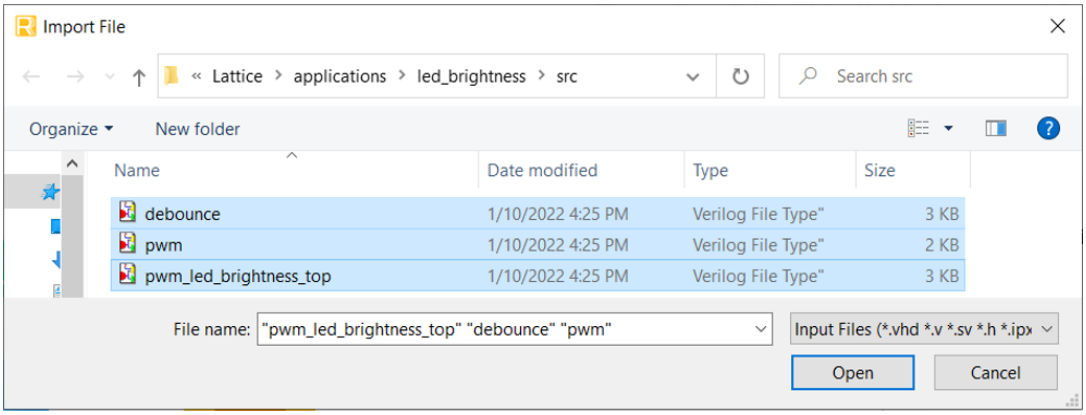

Figure 3: Selecting Sources

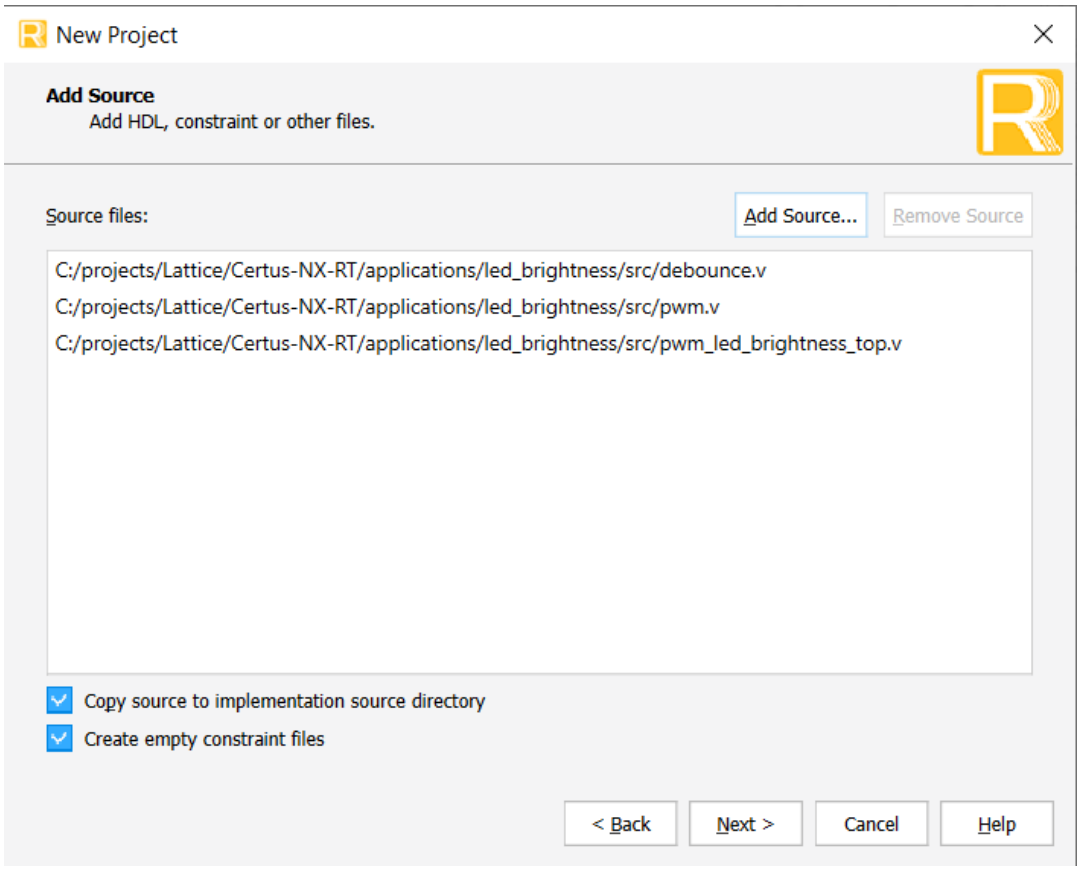

Figure 4: Adding Sources

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6. Select the appropriate device, click **Next** and choose **Lattice LSE**; click **Next** and **Finish**, see **Figure 5**.

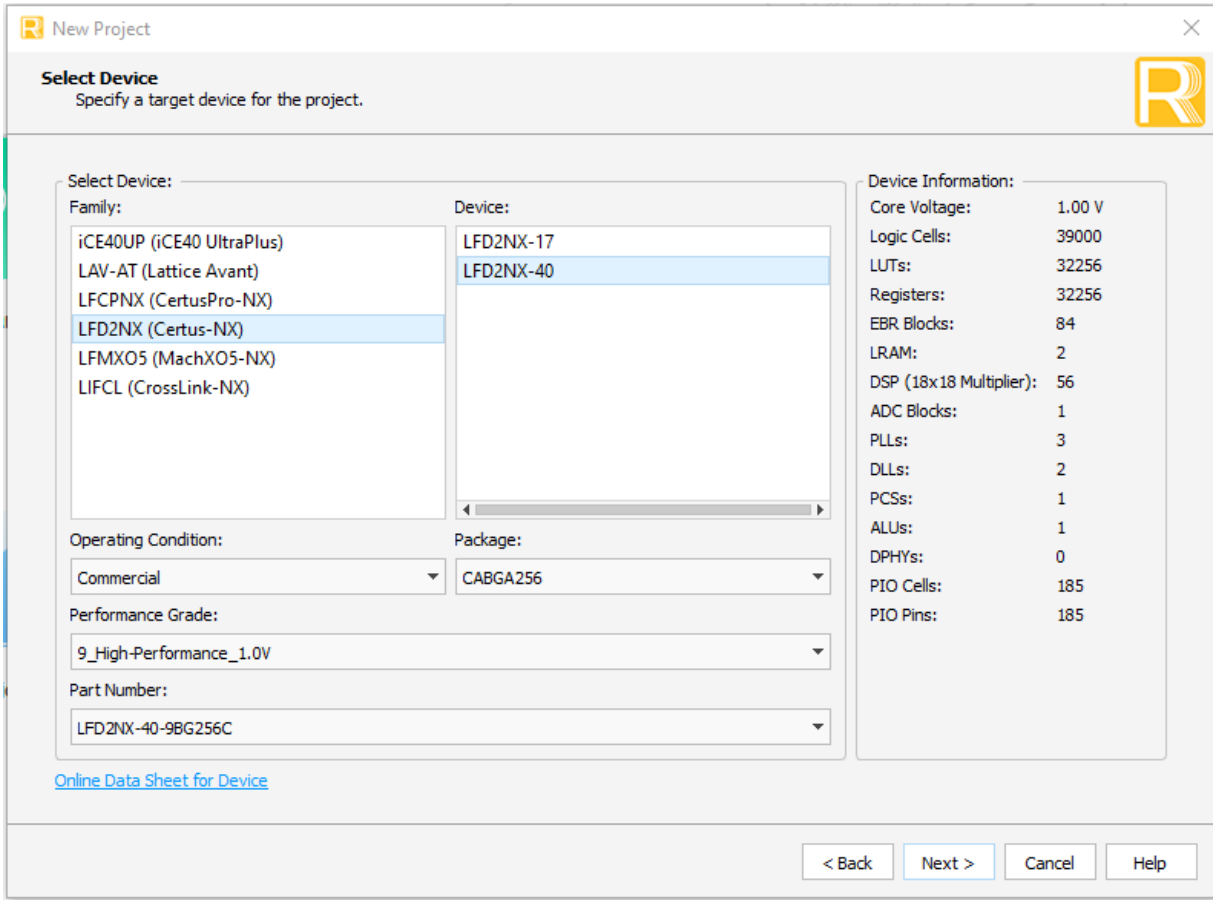

Figure 5: Selecting the FPGA Device

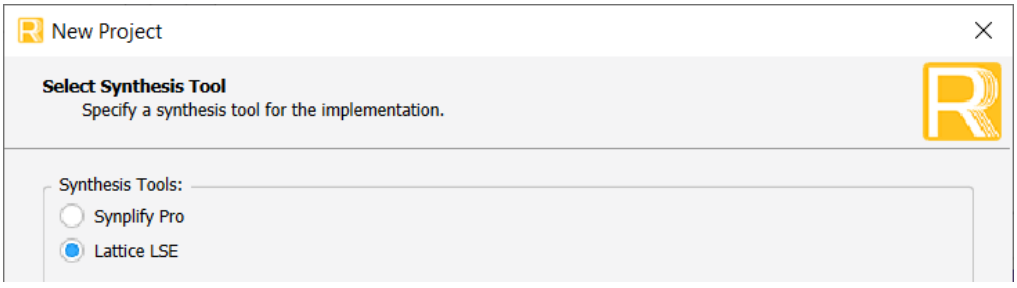

Figure 6: Selecting the Synthesis Tool

7. The initial project with the provided files should look like **Figure 7**.

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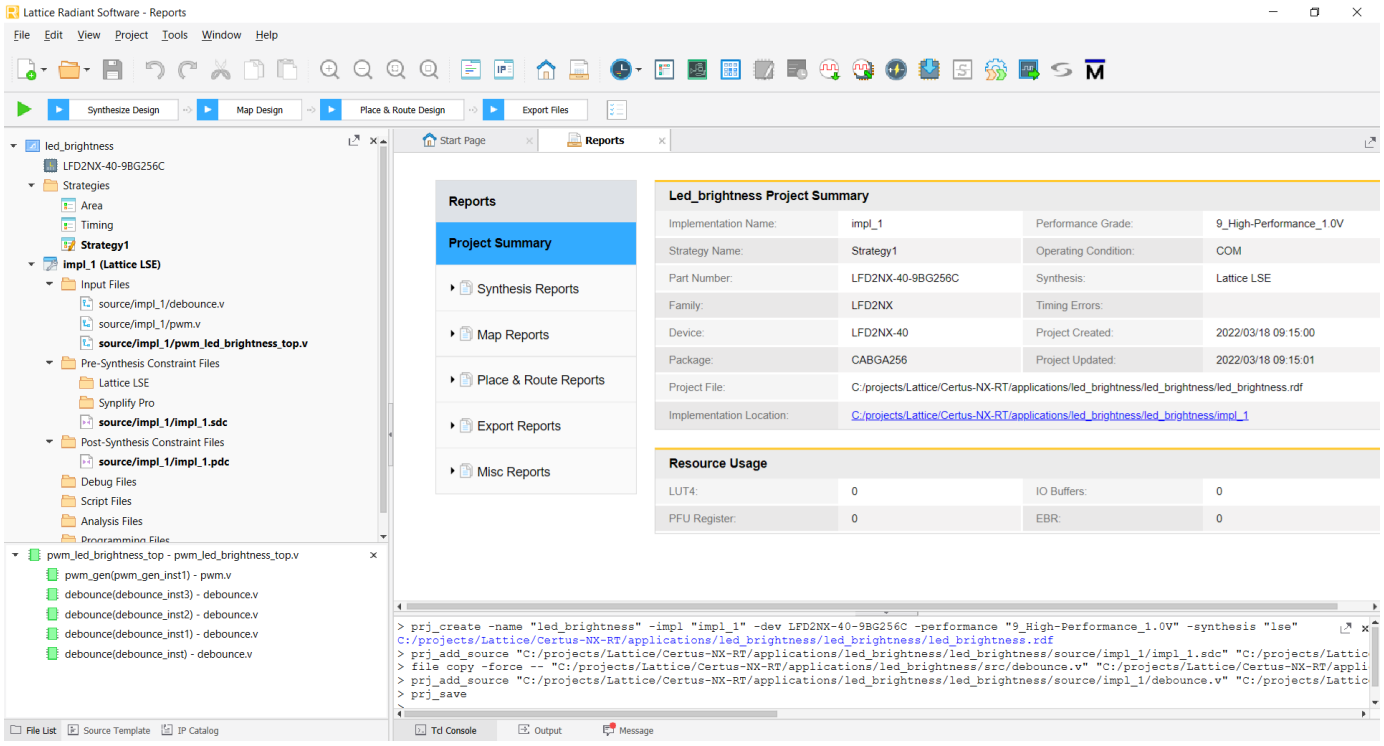

Figure 7: An Example of an Initial Project

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8. From the **IP Catalog Architecture Modules**, add a **PLL** module with the options shown below and name it **pwm_pll3**, see **Figure 8** and **Figure 9**.

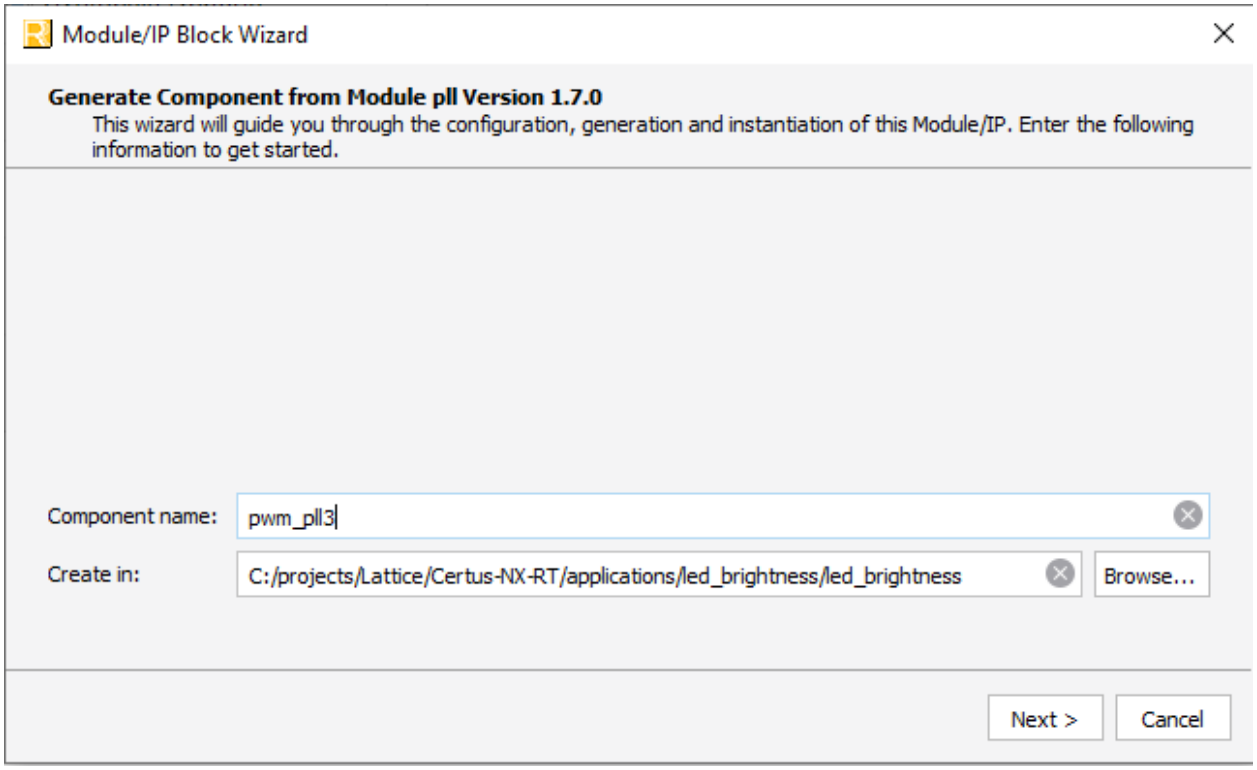

Figure 8: Opening the IP Catalog

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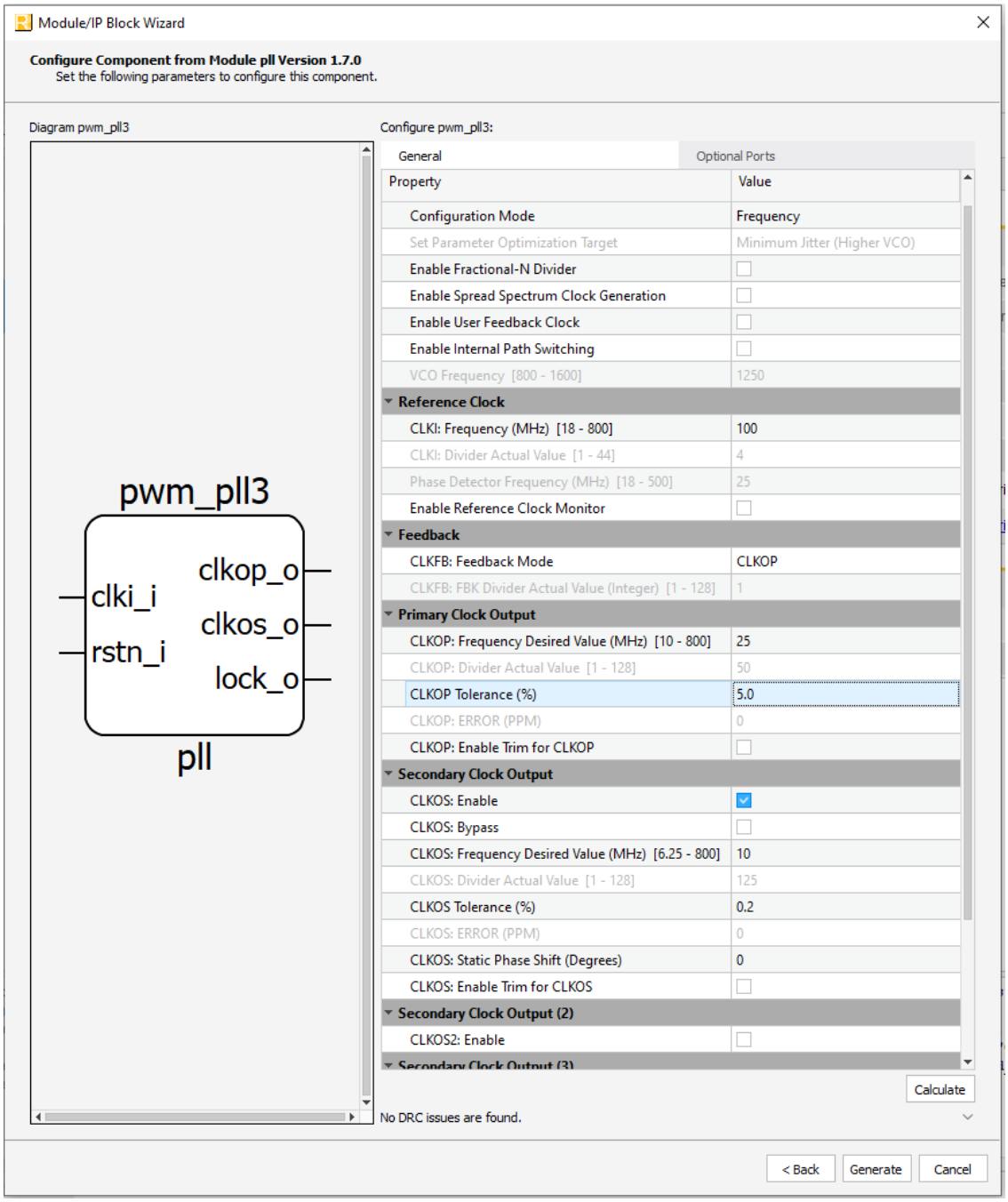

Figure 9: Adding a PLL from the IP Catalog

9. Once the **PLL** options are entered, click the Generate button to start the creation of the module.
10. ON the next screen, click the **Finish** button to complete the creation of the module.

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11. Once the **PLL** is created, it is added to the project files, see **Figure 10**.

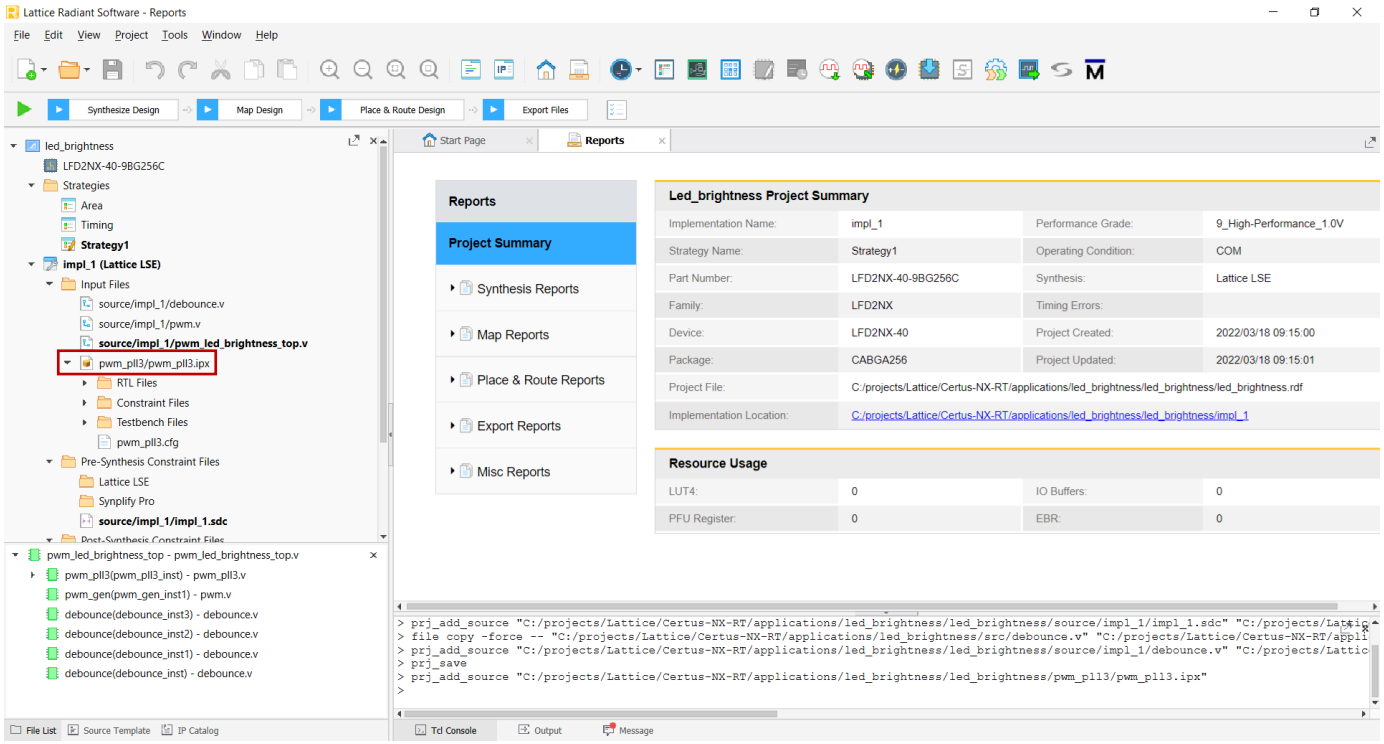

Figure 10: Looking at the Recently Added PLL IP

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4.0 Compile Design using Radiant Software

4.1 Set Top Level File

12. From the **Project** menu, select **Active Implementation** > **Set Top-Level Unit...** and set **pwm_led_brightness_top.v** as the top level file, see **Figure 11**.

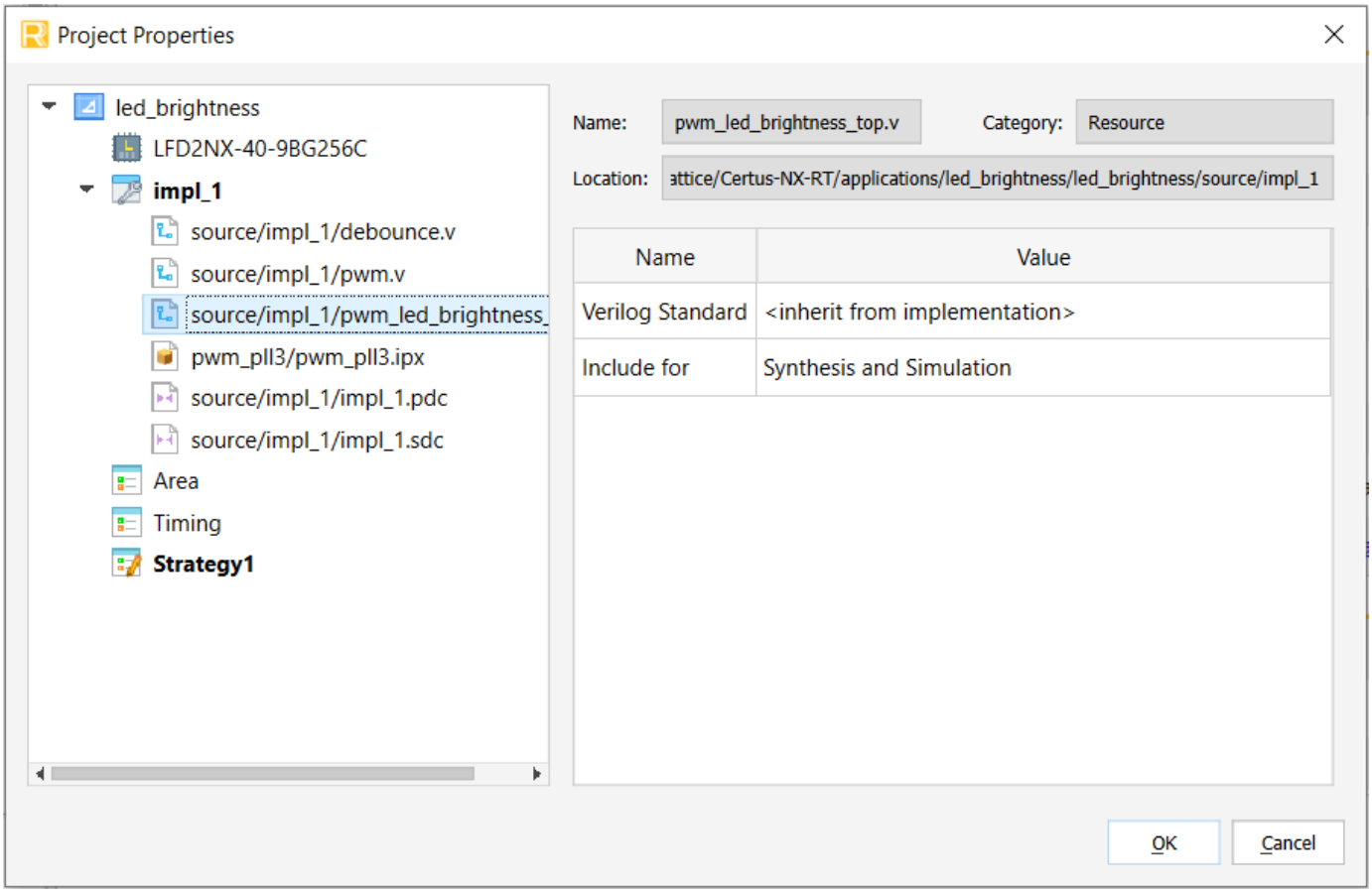

Figure 11: Setting a Top Level File

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4.2 Synthesize Design

13. Synthesize the design by clicking on the **Synthesize Design** arrow, see **Figure 12**.

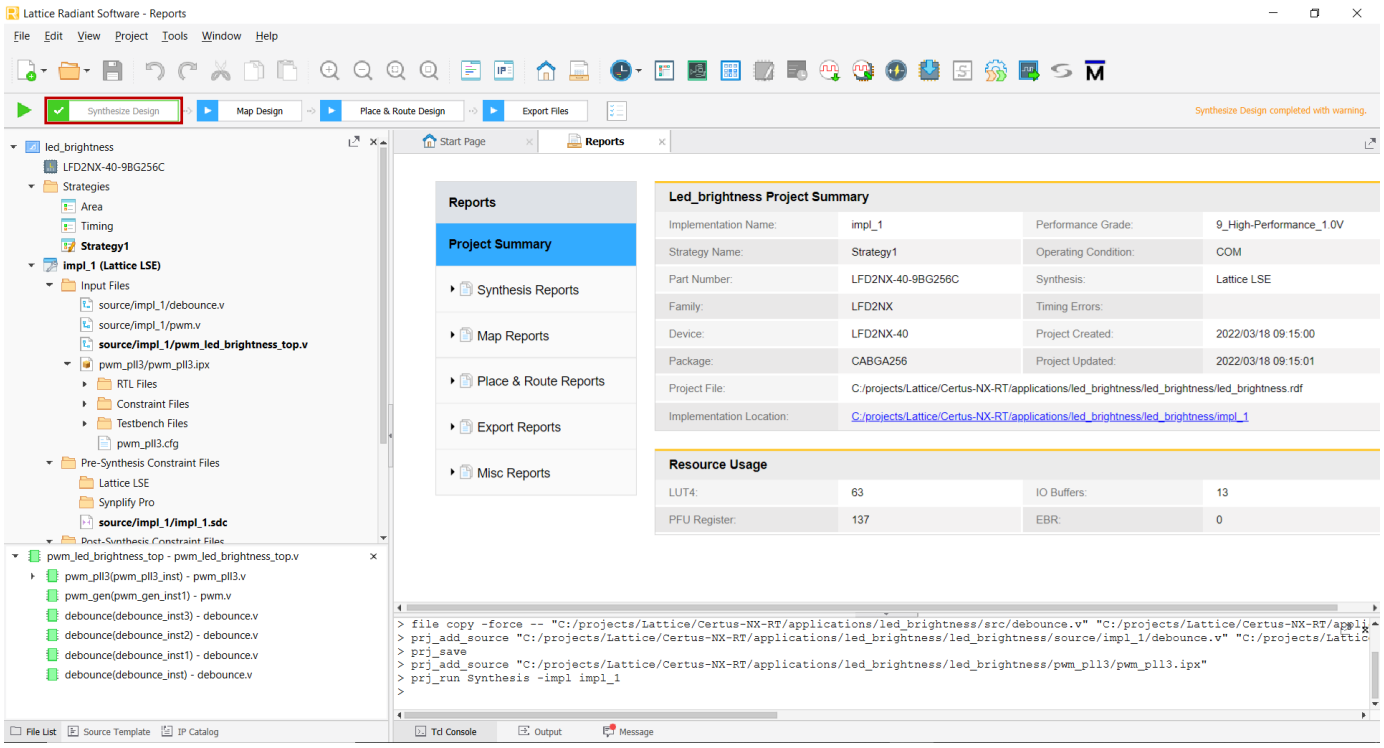

Figure 12: Synthesizing the Design

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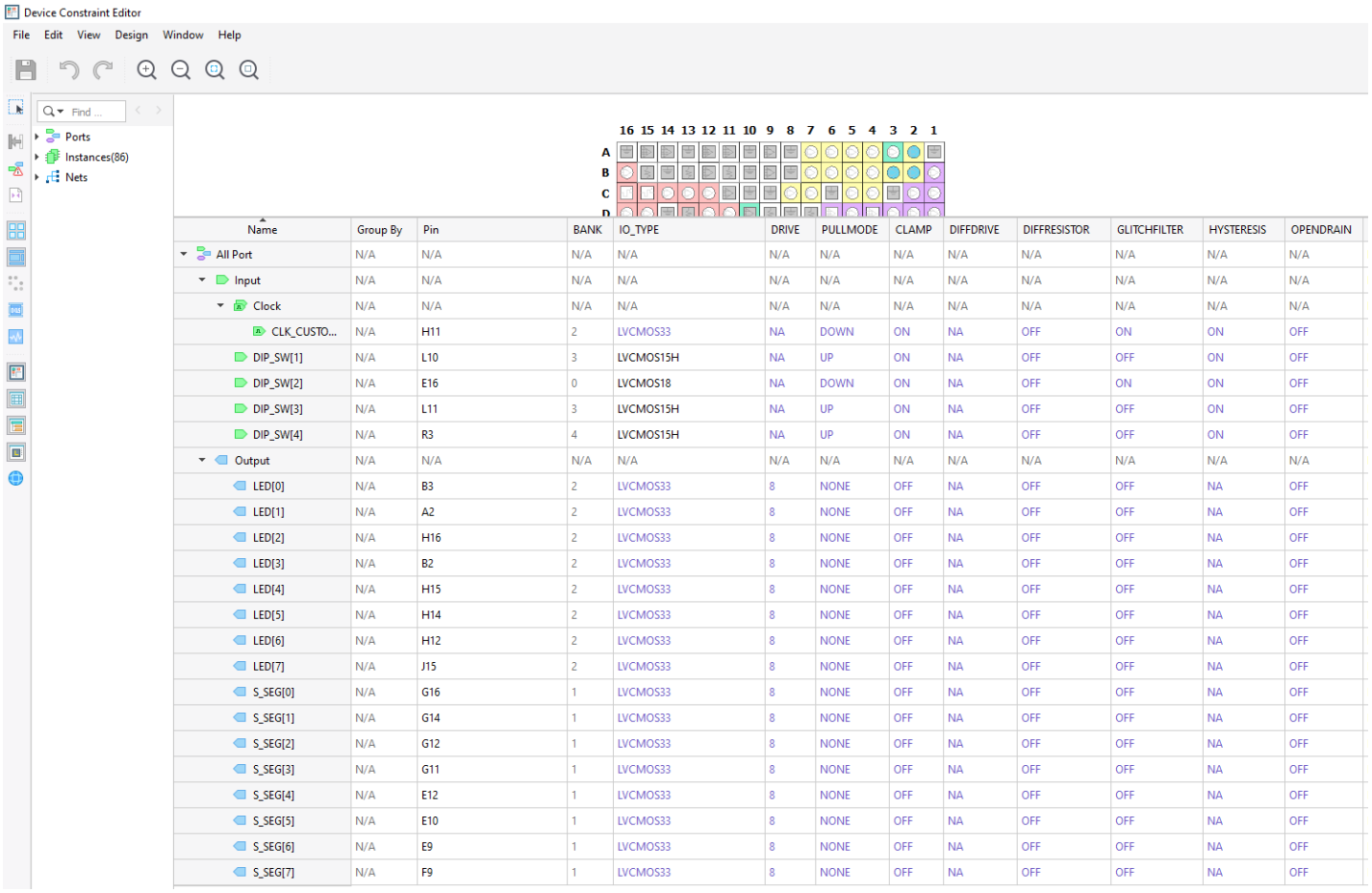
4.3 Pin Assignment (Device Constraint Editor)

14. Once the design has been synthesized, use the **Device Constraints Editor** option of the **Tools** drop down menu to assign the pin numbers to their respective signals, see **Figure 13**.



Name	Group By	Pin	BANK	IO_TYPE	DRIVE	PULLMODE	CLAMP	DIFFDRIVE	DIFFRESISTOR	GLITCHFILTER	HYSTERESIS	OPENDRAIN
All Port	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Input	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Clock	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
CLK_CUSTO...	N/A	H11	2	LVCMOS33	NA	DOWN	ON	NA	OFF	ON	ON	OFF
DIP_SW[1]	N/A	L10	3	LVCMOS15H	NA	UP	ON	NA	OFF	OFF	ON	OFF
DIP_SW[2]	N/A	E16	0	LVCMOS18	NA	DOWN	ON	NA	OFF	ON	ON	OFF
DIP_SW[3]	N/A	L11	3	LVCMOS15H	NA	UP	ON	NA	OFF	OFF	ON	OFF
DIP_SW[4]	N/A	R3	4	LVCMOS15H	NA	UP	ON	NA	OFF	OFF	ON	OFF
Output	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
LED[0]	N/A	B3	2	LVCMOS33	8	NONE	OFF	NA	OFF	OFF	NA	OFF
LED[1]	N/A	A2	2	LVCMOS33	8	NONE	OFF	NA	OFF	OFF	NA	OFF
LED[2]	N/A	H16	2	LVCMOS33	8	NONE	OFF	NA	OFF	OFF	NA	OFF
LED[3]	N/A	B2	2	LVCMOS33	8	NONE	OFF	NA	OFF	OFF	NA	OFF
LED[4]	N/A	H15	2	LVCMOS33	8	NONE	OFF	NA	OFF	OFF	NA	OFF
LED[5]	N/A	H14	2	LVCMOS33	8	NONE	OFF	NA	OFF	OFF	NA	OFF
LED[6]	N/A	H12	2	LVCMOS33	8	NONE	OFF	NA	OFF	OFF	NA	OFF
LED[7]	N/A	J15	2	LVCMOS33	8	NONE	OFF	NA	OFF	OFF	NA	OFF
S_SEG[0]	N/A	G16	1	LVCMOS33	8	NONE	OFF	NA	OFF	OFF	NA	OFF
S_SEG[1]	N/A	G14	1	LVCMOS33	8	NONE	OFF	NA	OFF	OFF	NA	OFF
S_SEG[2]	N/A	G12	1	LVCMOS33	8	NONE	OFF	NA	OFF	OFF	NA	OFF
S_SEG[3]	N/A	G11	1	LVCMOS33	8	NONE	OFF	NA	OFF	OFF	NA	OFF
S_SEG[4]	N/A	E12	1	LVCMOS33	8	NONE	OFF	NA	OFF	OFF	NA	OFF
S_SEG[5]	N/A	E10	1	LVCMOS33	8	NONE	OFF	NA	OFF	OFF	NA	OFF
S_SEG[6]	N/A	E9	1	LVCMOS33	8	NONE	OFF	NA	OFF	OFF	NA	OFF
S_SEG[7]	N/A	F9	1	LVCMOS33	8	NONE	OFF	NA	OFF	OFF	NA	OFF

Figure 13: Performing Pin Assignment

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4.4 Compile Design

15. Compile the design by clicking on the **Run All** arrow, see **Figure 14**.

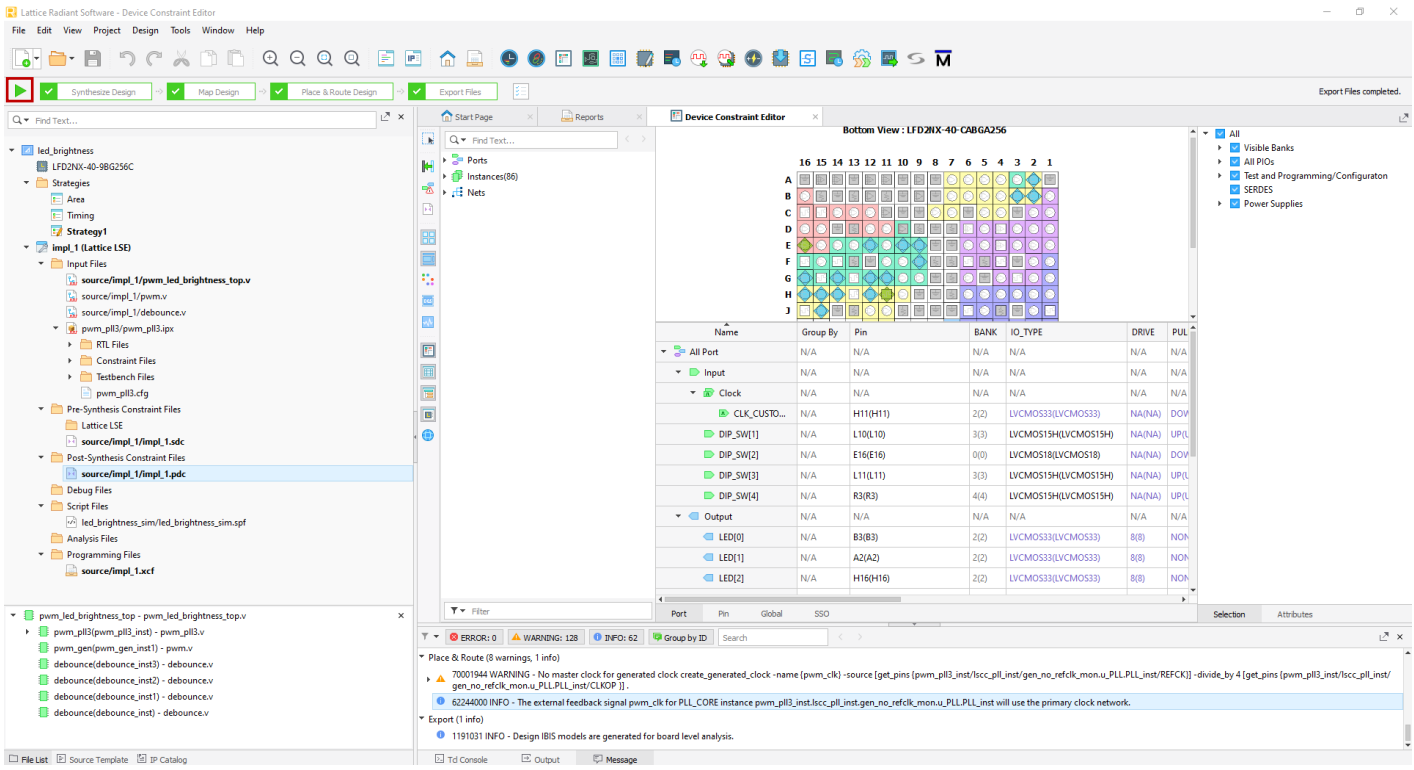

Figure 14: Compiling the Design

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4.4 Simulate Design

16. From the **Tools** menu, select **Simulation Wizard** and click **Next**, see **Figure 15**.

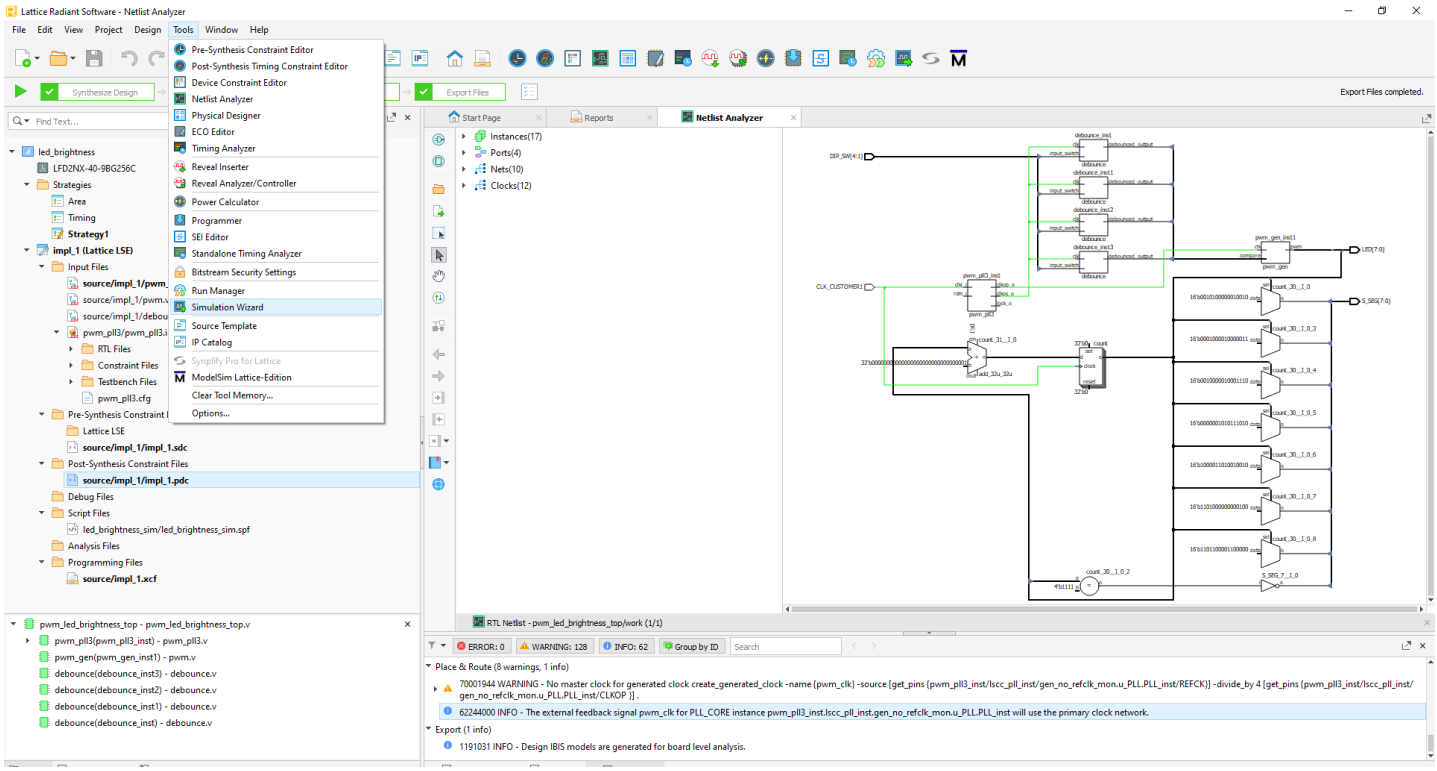

Figure 15: Simulating the Design

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17. Name the project **led_brightness_sim** and click **Next**, see **Figure 16**. If asked whether you want to create it, click **Yes**. Click Next to **Add and Reorder Source** and **Parse HDL files for simulation**. Click **Finish** to start the simulation.

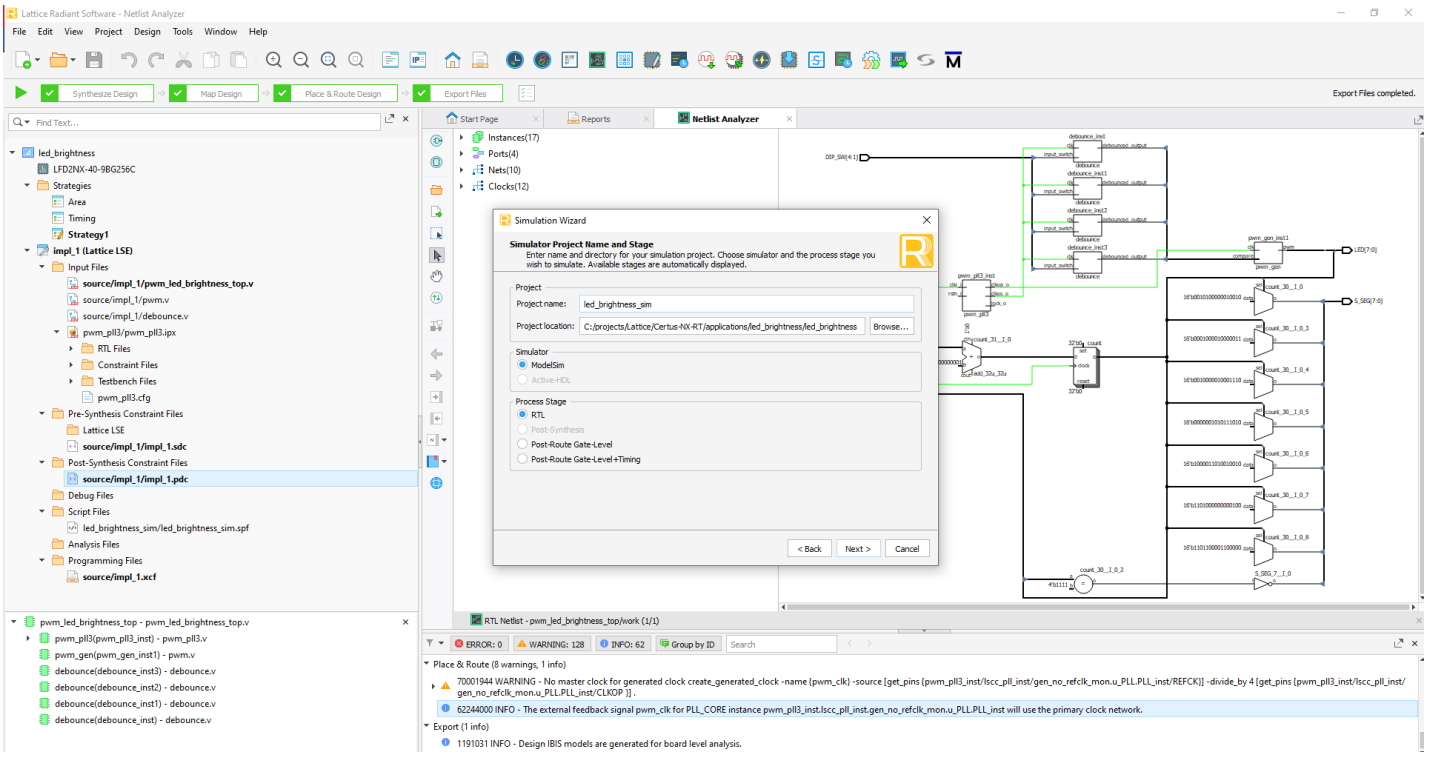

Figure 16: Naming the Simulation

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18. When finished, **ModelSim** will open and run the simulation, see **Figure 17**.

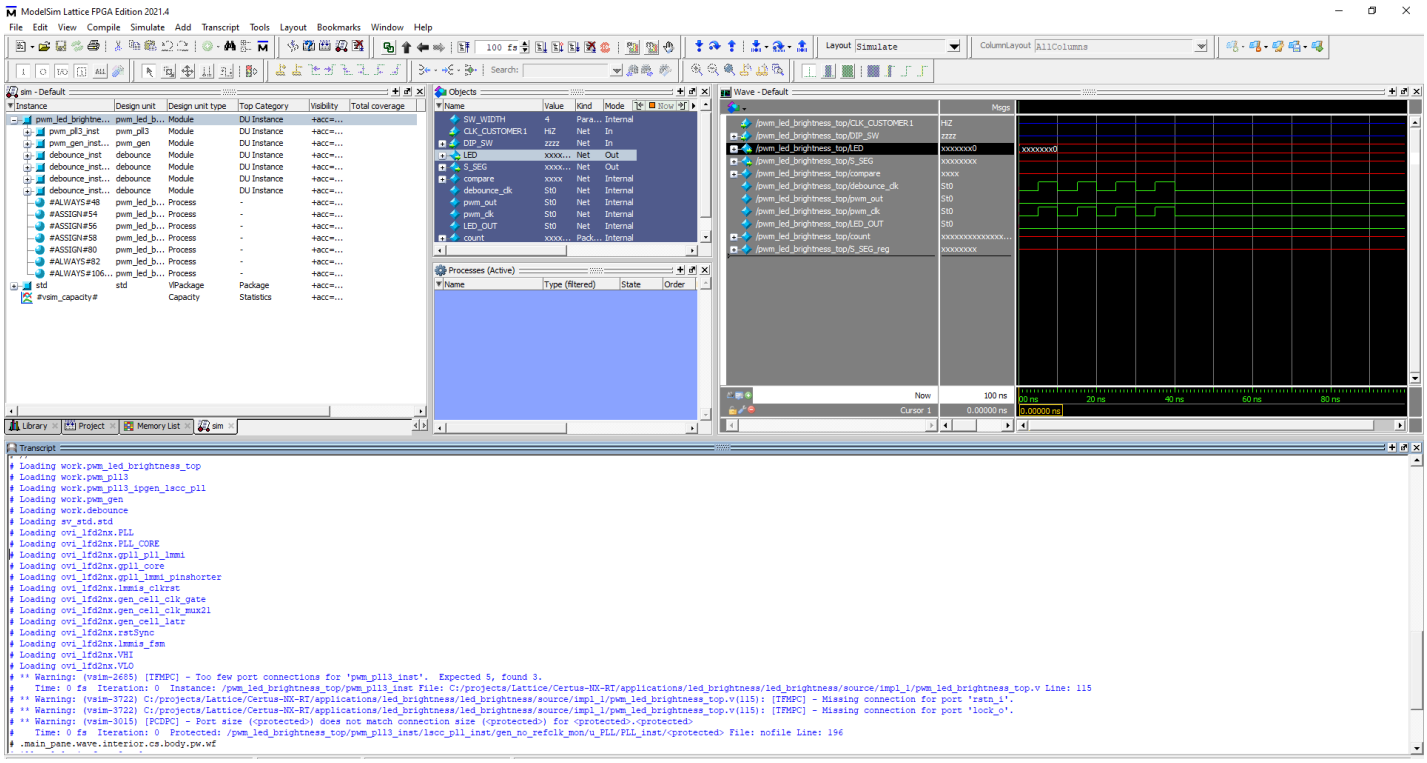

Figure 17: The ModelSim Simulation Wave View

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5.0 Program the Device with Radiant Programmer

19. Make sure that in the Lattice Certus-NX Versa Evaluation board LFD2NX-VERSA-EVN:
20. there is a USB cable connecting the computer to J2
21. there is a 12V power supply connected to J35
22. From the **Tools** menu, select **Programmer** and a new window opens, see **Figure 18**.

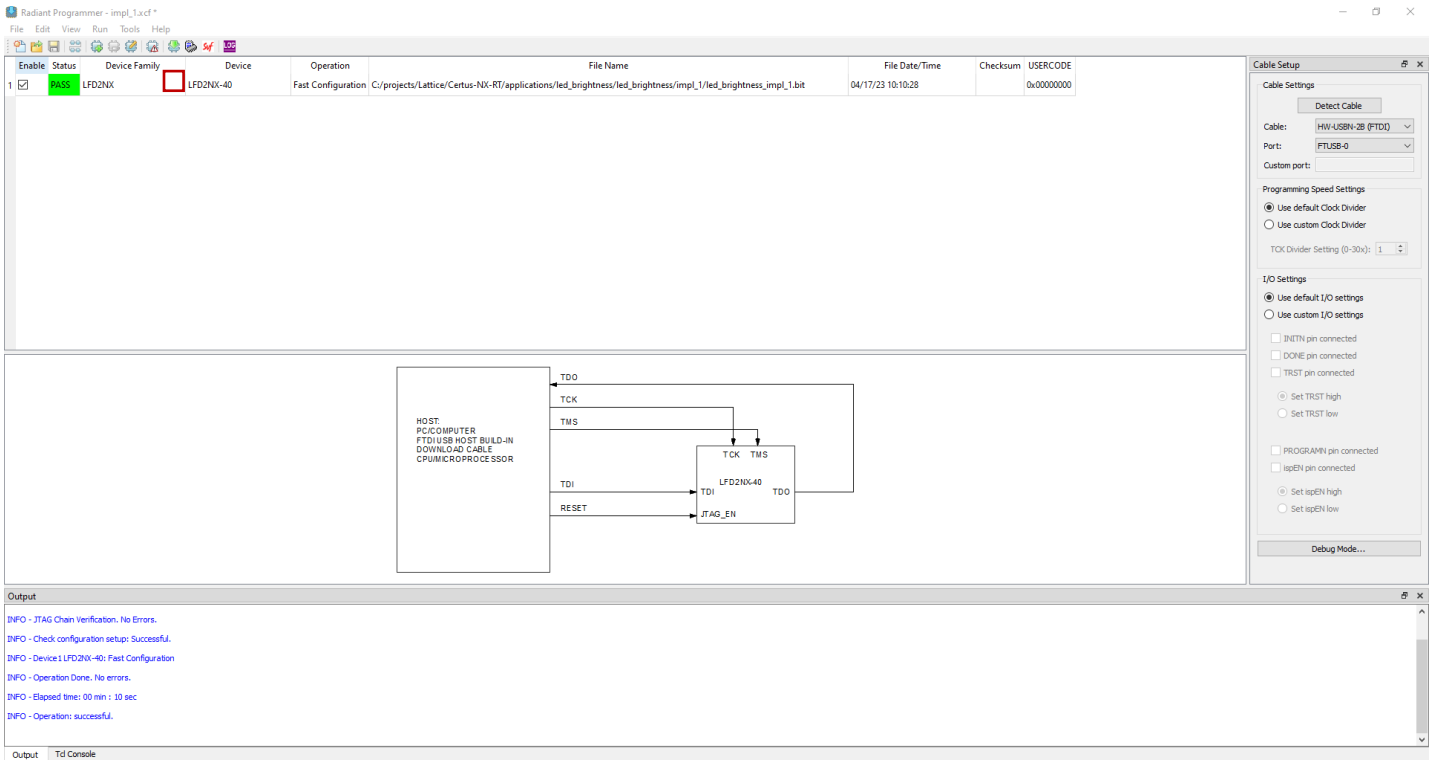

Figure 18: Programming the FPGA

23. Once the cable is detected and settings are set, program the device by clicking the Program Device icon  , **Figure 18**.
24. Verify that:
    - the LED's [7:0] show the heartbeat of the system
    - the sever-segment LED displays a hexadecimal counter with the decimal point LED also being turned on whenever the count value equals F hex.

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REVISION HISTORY

Date	Rev. #	Author	Change Description
3/18/2022	1.0.0	JA	Initial Release.
4/17/2023	1.0.1	JB	Completed porting App Note to Certus-NX-RT using Lattice Certus-NX Versa Evaluation board LFD2NX-VERSA-EVN

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