PRODUCT NAME	MANUFACTURER PART NUMBER	DEVICE TYPE
Lattice Certus-NX-RT FPGA	UT24C407	RL01

Table 1: Cross Reference of Applicable Products

1.0 Overview

This document details the process of creating a **Certus-NX-RT** FPGA project using the **Lattice Radiant** software tools and the Lattice Certus-NX Versa Evaluation board LFD2NX-VERSA-EVN.

For the purposes of this document, create a project named **led_brightness** and configure the **Radiant** tools to include all the source modules required for a successful build.

Using this template, projects are created using:

- (a) the preferred application source directory structures and
- (b) the directory structure for the **Radiant**-supplied files.

Figure 1 shows the block diagram of the design, it includes:

- the DIP switch inputs DIP_SW[4:1] which control the duty cycle to the PWM output, which in turn controls the brightness to LED[0]
- the LED[7:0] outputs controlled by 7 bits of the design's internal 32-bit counter "count" and are used to show the heartbeat of the system. The counter's bits [30:24] drive the LED[7:0]
- the S_SEG[7:0] outputs are also controlled by 4 bits of the internal 32-bit counter "count" and are used to drive the board's 7-segment LED device. Specifically, the counter's 4 bits [30:27] are decoded in such a way as to drive the 7-segment LED display's control signals S_SEG[7:0] as a hexadecimal counter with the decimal point LED also being turned on whenever the count value equals F hex.



Figure 1: An Example Netlist View

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2.

Creating Certus-NX-RT Project in Radiant Software

3.0 Creating a Design Project with Radiant Software

- 1. Download CreatingRadiantProject.zip from caes.com.
 - Launch Radiant Software
- 3. From the **File** menu, select **New > Project...**.
- 4. Specify the project name as **led_brightness**, navigate to the **location** of your choice and click **Next**, see **Figure 2**.

民 New Proje	ect	×
Project Nan Enter a	ne name for your project and specify a directory where the project data files will be stored.	R
Project: -		
<u>N</u> ame:	led_brightness	
Location:	C:/projects/Lattice/Certus-NX-RT/applications/led_brightness	
Project will	l be created at C:/projects/Lattice/Certus-NX-RT/applications/led_brightness/l 🔽 Create subdirect	ory
Implement	tation:	
Na <u>m</u> e:	impi_1	_
Location:	C:/projects/Lattice/Certus-NX-RT/applications/led_brightness/led_brightness/impl_1	
	< <u>B</u> ack <u>N</u> ext > Cancel <u>H</u>	elp

Figure 2: Creating a Radiant Design Project

5. Select Add Source... and click Open, see Figure 3 and Figure 4, click Next.

民 Import I	File			×
$\leftarrow \rightarrow$	A Lattice > applications > led_brig	ghtness > src	✓ Ŭ ,○ se	earch src
Organize	New folder			
~	Name	Date modified	Туре	Size
	📓 debounce	1/10/2022 4:25 PM	Verilog File Type"	3 KB
	📓 pwm	1/10/2022 4:25 PM	Verilog File Type"	2 KB
	pwm_led_brightness_top	1/10/2022 4:25 PM	Verilog File Type"	3 KB
	File name: "pwm_led_brightness_top" "	debounce" "pwm"	V Input Fi	iles (*.vhd *.v *.sv *.h *.ipx ~

Figure 3: Selecting Sources

Add Source Add HDL, constraint or c	ther files.			
Source files:			<u>A</u> dd Source	Remove Sourc
C:/projects/Lattice/Certus-	-NX-RT/applications/le	d_brightness/src/de	bounce.v	
C:/projects/Lattice/Certus-	-NX-RT/applications/le	d_brightness/src/pv	vm.v	
C:/projects/Lattice/Certus-	-NX-RT/applications/le	d_brightness/src/pv	wm_led_brightness_to	op.v
✓ Copy source to implement	ntation source directory			
 ✓ Copy source to implement ✓ Create empty constraint 	itation source directory files			

Figure 4: Adding Sources

6. Select the appropriate device, click Next and choose Lattice LSE; click Next and Finish, see Figure 5.

Select Device:		Device Information:	
Family:	Device:	Core Voltage:	1.00 V
iCE40UP (iCE40 UltraPlus)	LFD2NX-17	Logic Cells:	39000
LAV-AT (Lattice Avant)	LFD2NX-40	LUTS:	32256
LFCPNX (CertusPro-NX)		Registers:	32256
LFD2NX (Certus-NX)		EBR Blocks:	84
LFMXO5 (MachXO5-NX)		LRAM:	2
LIFCL (CrossLink-NX)		DSP (18x18 Multiplie	er): 56
		ADC Blocks:	1
		PLLs:	3
		DLLS:	2
	4	PCSS:	1
Operating Condition:	Package:	ALUS:	1
Commercial	▼ CABGA256	PIO Cells:	185
Performance Grade:		PIO Pins:	185
9_High-Performance_1.0V		•	
Part Number:			
LFD2NX-40-9BG256C		-	

Figure 5: Selecting the FPGA Device

R New Project	×
Select Synthesis Tool Specify a synthesis tool for the implementation.	R
Synthesis Tools: Synplify Pro Lattice LSE	

Figure 6: Selecting the Synthesis Tool

7. The initial project with the provided files should look like **Figure 7**.

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Inpr_ (tattee LSt)	Cunthasia Daparta	Part Number:	LFD2NX-40-9BG256C	Synthesis:	Lattice LSE	
source/impl_1/debounce.v	Synthesis Reports	Family:	LFD2NX	Timing Errors:		
source/impl_1/pwm.v	Map Reports	Device:	LFD2NX-40	Project Created:	2022/03/18 09:15:00	
Source/mp_r/pwm_reg_brightness_top.v		Package:	CABGA256	Project Updated:	2022/03/18 09:15:01	
Lattice LSE	Place & Route Reports	Project File:	C:/projects/Lattice/Certus-NX-	RT/applications/led_brightness/led_b	rightness/led_brightness.rdf	
Synplify Pro	_	Implementation Location: C:/projects/Lattice/Certus-NX-RT/applications/led_brightness/led_brightness/impl_1				
source/impl_1/impl_1.sdc	 Export Reports 					
s source/impl_1/impl_1.pdc	Misc Reports	Resource Usage				
Debug Files		LUT4:	0	IO Buffers:	0	
Analysis Files		PFU Register:	0	EBR:	0	
Programming Files						
pwm_led_brightness_top - pwm_led_brightness_top.v ×						
pwm_gen(pwm_gen_inst1) - pwm.v						
debounce(debounce_inst3) - debounce.v	•				•	
debounce(debounce_inst2) - debounce.v	> prj_create -name "led_brightness	" -impl "impl_1" -dev LFD2	NX-40-9BG256C -performance	9_High-Performance_1.0	/" -synthesis "lse" 🖉 🛪	
debounce(debounce_inst) - debounce v	C:/projects/Lattice/Certus-NX-RT/a	pplications/led_brightness ice/Certus-NX-RT/applicati	<pre>/led_brightness/led_bright ons/led_brightness/led_bright</pre>	ness.rdf abtness/source/impl 1/imr	1.sdc" "C:/projects/Lattic	
	<pre>> file copy -force "C:/projects > prj_add_source "C:/projects/Latt > prj_save</pre>	/Lattice/Certus-NX-RT/appl ice/Certus-NX-RT/applicati	ications/led_brightness/sn .ons/led_brightness/led_bri	c/debounce.v" "C:/project ghtness/source/impl_1/deb	cs/Lattice/Certus-NX-RT/appli bounce.v" "C:/projects/Lattic	
File List Source Template IP Catalog	Td Console 🕑 Output 투 Mes	sage			•	

Figure 7: An Example of an Initial Project

8. From the **IP Catalog Architecture Modules**, add a **PLL** module with the options shown below and name it **pwm_pll3**, see **Figure 8** and **Figure 9**.

R Module/IP Block	Wizard	×				
Generate Component from Module pll Version 1.7.0 This wizard will guide you through the configuration, generation and instantiation of this Module/IP. Enter the following information to get started.						
Component name:	pwm_pll3	\otimes				
Create in:	C:/projects/Lattice/Certus-NX-RT/applications/led_brightness/led_brightness	·				
	Next > Ca	ncel				

Figure 8: Opening the IP Catalog

gram pwm_pll3	Configure pwm_pll3:	
	General Optic	onal Ports
	Property	Value
	Configuration Mode	Frequency
	Set Parameter Optimization Target	Minimum Jitter (Higher VCO)
	Enable Fractional-N Divider	
	Enable Spread Spectrum Clock Generation	
	Enable User Feedback Clock	
	Enable Internal Path Switching	
	VCO Frequency [800 - 1600]	1250
	▼ Reference Clock	
	CLKI: Frequency (MHz) [18 - 800]	100
	CLKI: Divider Actual Value [1 - 44]	4
nwm nll3	Phase Detector Frequency (MHz) [18 - 500]	25
hwiii_hii2	Enable Reference Clock Monitor	
	▼ Feedback	
	CLKFB: Feedback Mode	CLKOP
	CLKFB: FBK Divider Actual Value (Integer) [1 - 128]	1
	 Primary Clock Output 	
_rstn_i	CLKOP: Frequency Desired Value (MHz) [10 - 800]	25
	CLKOP: Divider Actual Value [1 - 128]	50
	CLKOP Tolerance (%)	5.0
	CLKOP: ERROR (PPM)	0
pll	CLKOP: Enable Trim for CLKOP	
P.1	 Secondary Clock Output 	
	CLKOS: Enable	
	CLKOS: Bypass	
	CLKOS: Frequency Desired Value (MHz) [6.25 - 800]	10
	CLKOS: Divider Actual Value [1 - 128]	125
	CLKOS Tolerance (%)	0.2
	CLKOS: ERROR (PPM)	0
	CLKOS: Static Phase Shift (Degrees)	U
	CLKUS: Enable Irim for CLKUS	
	CLKOS2: Enable	
	CLNUS2: Enable	
	Secondary (lock ()utnut (3)	

Figure 9: Adding a PLL from the IP Catalog

Once the **PLL** options are entered, click the Generate button to start the creation of the module.
 ON the next screen, click the **Finish** button to complete the creation of the module.

11. Once the **PLL** is created, it is added to the project files, see **Figure 10**.

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📝 Strategy1	Project Summary	Strategy Name:	Strategy1	Operating Condition:	COM	
▼ 🛃 impl_1 (Lattice LSE)		Part Number:	LFD2NX-40-9BG256C	Synthesis:	Lattice LSE	
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source/impl 1/pwm led brightness top.v	Map Reports	Device:	LFD2NX-40	Project Created:	2022/03/18 09:15:00	
 pwm_pll3/pwm_pll3.ipx 		Package:	CABGA256	Project Updated:	2022/03/18 09:15:01	
RTL Files	Place & Route Reports	Project File:	C:/projects/Lattice/Certus-NX-	RT/applications/led_brightness/led_b	rightness/led_brightness.rdf	
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pwm_pll3.cfg						
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Synphity Pro		PFU Register:	0	EBR:	0	
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Figure 10: Looking at the Recently Added PLL IP

4.0 Compile Design using Radiant Software

4.1 Set Top Level File

12. From the **Project** menu, select **Active Implementation** > **Set Top-Level Unit...** and set **pwm_led_brightness_top.v** as the top level file, see **Figure 11**.

R Project Properties						×
 Project Properties Ied_brightness LFD2NX-40-9BG256C impl_1 source/impl_1/debounce.v source/impl_1/pwm.v source/impl_1/pwm_led_brightness pwm_pll3/pwm_pll3.ipx source/impl_1/impl_1.pdc source/impl_1/impl_1.sdc Area Timing Strategy1 	Name: Location: Na Verilog S Include	pwm_led_ attice/Cert me Standard for	_brightness_top.v us-NX-RT/application <inherit from="" im<br="">Synthesis and Si</inherit>	Category: ns/led_brightness/ Value nplementation> mulation	Resource /led_brightness/s	ource/impl_1
4					Ōĸ	Cancel

Figure 11: Setting a Top Level File

4.2 Synthesize Design

13. Synthesize the design by clicking on the **Synthesize Design** arrow, see **Figure 12**.

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 Importment Synthesis Reports Source/impl_1/debounce.vt Source/impl_1/prom_leld_brightness_top.v Source/impl_1/prom_leld_brightness_top.v Map Reports Map Reports Map Reports Map Reports Project File: Constraint Files Testbench Files Testbench Files Testbench Files Source/impl_1/impl_1.adc Misc Reports Source/impl_1/impl_1.adc Source/impl_1.adc Source/impl_1.	 impl_1 (Lattice LSE) impl_sequences 	-	Part Number:	LFD2NX-40-9BG256C	Synthesis:	Lattice LSE	
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<pre> Source/impl 1/pwm_plBjpwm_plBjpwm_plBjpwm_plBjpwm_plBjpmm_plB / pwm_plBjpvm_plB / pwm_plBjpvm_plB / pwm_plB / pwm/plB / pwm_plB / pwm/plB / pwm_plB / pwm_plB / pwm/plB / pwm_plB / pwm/plB / pwm_plB / pwm_pl</pre>	source/impl_1/pwm.v	Map Reports	Device:	LFD2NX-40	Project Created:	2022/03/18 09:15:00	
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<pre>debounce/debounce.inst3 - debounce.v" "C:/projects/Lattice/Certus-NX-RT/applications/led_brightness/sc/debounce.v" "C:/projects/Lattice/Certus-NX-RT/applications/led_brightness/sc/debounce.v" "C:/projects/Lattice/Certus-NX-RT/applications/led_brightness/sc/debounce.v" "C:/projects/Lattice/Certus-NX-RT/applications/led_brightness/sc/debounce.v" "C:/projects/Lattice/Certus-NX-RT/applications/led_brightness/sc/debounce.v" "C:/projects/Lattice/Certus-NX-RT/applications/led_brightness/sc/debounce.v" "C:/projects/Lattice/Certus-NX-RT/applications/led_brightness/sc/debounce.v" "C:/projects/Lattice/Certus-NX-RT/applications/led_brightness/led_brightness/sc/certus-NX-RT/applications/led_brightness/led_brightness/sc/certus-NX-RT/applications/led_brightness/led_brightness/sc/certus-NX-RT/applications/led_brightness/led_brightness/sc/certus-NX-RT/applications/led_brightness/led_brightness/sc/certus-NX-RT/applications/led_brightness/led_brightness/sc/certus-NX-RT/applications/led_brightness/led_brightness/sc/certus-NX-RT/applications/led_brightness/led_brightness/sc/certus-NX-RT/applications/led_brightness/led_brightness/sc/certus-NX-RT/applications/led_brightness/led_brightness/sc/certus-NX-RT/applications/led_brightness/led_brightness/sc/certus-NX-RT/applications/led_brightness/led_brightness/sc/certus-NX-RT/applications/led_brightness/sc/certus-NX-RT/applications/led_brightness/sc/certus-NX-RT/applications/led_brightness/sc/certus-NX-RT/applications/led_brightness/sc/certus-NX-RT/applications/led_brightness/sc/certus-NX-RT/applications/led_brightness/sc/certus-NX-RT/applications/led_brightness/sc/certus-NX-RT/applications/led_brightness/sc/certus-NX-RT/applications/led_brightness/sc/certus-NX-RT/applications/led_brightness/sc/certus-NX-RT/applications/led_brightness/sc/certus-NX-RT/applications/led_brightness/sc/certus-NX-RT/applications/led_brightness/sc/certus-NX-RT/applications/led_brightness/sc/certus-NX-RT/applications/led_brightness/sc/certus-NX-RT/applications/led_brightness/sc/certus-NX-RT/applications/led_b</pre>	pwm_gen(pwm_gen_inst1) - pwm.v						
<pre>debounce(debounce,inst2) - debounce.v > prj_add_source "C:/projects/Lattice/Certus-NX-RT/applications/led_brightness/source/imm_pll3/pwm_pll3.ipx" debounce(debounce,inst) - debounce.v * "C:/projects/Lattice/Certus-NX-RT/applications/led_brightness/led_brightness/pwm_pll3.ipx" prj_adv prj_adv prj_adv prj_surs ynthesis - impl impl_1 </pre>	debounce(debounce_inst3) - debounce.v	<pre>1 > file conv =force == "C:/projecte</pre>	/Lattice/Certue_NY_PT/annl	ications/lad brightness/er	c/debounce w" "C:/project	e/Lattice/Certue_NV_PT/aneli	
debounce(debounce_inst) - debouncev > prj_adwe prj_add_source "C:/projects/Lattice/Certus=NX=RT/applications/led_brightness/led_brightness/pwm_pll3.ipx" > prj_run Synthesis - impl impl_1 >	debounce(debounce_inst2) - debounce.v	<pre>> prj_add_source "C:/projects/Latt</pre>	ice/Certus-NX-RT/applicati	lons/led_brightness/led_bri	ghtness/source/impl_1/deb	ounce.v" "C:/projects/Lattic	
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>	debounce(debounce_inst) - debounce.v	> prj_run Synthesis -impl impl_1			gnonooo, pmm_p110/pmm_p110		
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	Carlos Da la David	4				*	

Figure 12: Synthesizing the Design

4.3 Pin Assignment (Device Constraint Editor)

14. Once the design has been synthesized, use the **Device Constraints Editor** option of the **Tools** drop down menu to assign the pin numbers to their respective signals, see **Figure 13**.

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	Name	Group By	Pin	BANK	IO_TYPE	DRIVE	PULLMODE	CLAMP	DIFFDRIVE	DIFFRESISTOR	GLITCHFILTER	HYSTERESIS	OPENDRAIN
	🔻 😓 All Port	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
	🝷 📄 Input	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
	🝷 🔝 Clock	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
	CLK_CUSTO	N/A	H11	2	LVCMOS33	NA	DOWN	ON	NA	OFF	ON	ON	OFF
	DIP_SW[1]	N/A	L10	3	LVCMOS15H	NA	UP	ON	NA	OFF	OFF	ON	OFF
	DIP_SW[2]	N/A	E16	0	LVCMOS18	NA	DOWN	ON	NA	OFF	ON	ON	OFF
	DIP_SW[3]	N/A	L11	3	LVCMOS15H	NA	UP	ON	NA	OFF	OFF	ON	OFF
	DIP_SW[4]	N/A	R3	4	LVCMOS15H	NA	UP	ON	NA	OFF	OFF	ON	OFF
	🔻 🦪 Output	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
	LED[0]	N/A	B3	2	LVCMOS33	8	NONE	OFF	NA	OFF	OFF	NA	OFF
	LED[1]	N/A	A2	2	LVCMOS33	8	NONE	OFF	NA	OFF	OFF	NA	OFF
	LED[2]	N/A	H16	2	LVCMOS33	8	NONE	OFF	NA	OFF	OFF	NA	OFF
	LED[3]	N/A	B2	2	LVCMOS33	8	NONE	OFF	NA	OFF	OFF	NA	OFF
	LED[4]	N/A	H15	2	LVCMOS33	8	NONE	OFF	NA	OFF	OFF	NA	OFF
	LED[5]	N/A	H14	2	LVCMOS33	8	NONE	OFF	NA	OFF	OFF	NA	OFF
	LED[6]	N/A	H12	2	LVCMOS33	8	NONE	OFF	NA	OFF	OFF	NA	OFF
	LED[7]	N/A	J15	2	LVCMOS33	8	NONE	OFF	NA	OFF	OFF	NA	OFF
	S_SEG[0]	N/A	G16	1	LVCMOS33	8	NONE	OFF	NA	OFF	OFF	NA	OFF
	S_SEG[1]	N/A	G14	1	LVCMOS33	8	NONE	OFF	NA	OFF	OFF	NA	OFF
	S_SEG[2]	N/A	G12	1	LVCMOS33	8	NONE	OFF	NA	OFF	OFF	NA	OFF
	S_SEG[3]	N/A	G11	1	LVCMOS33	8	NONE	OFF	NA	OFF	OFF	NA	OFF
	S_SEG[4]	N/A	E12	1	LVCMOS33	8	NONE	OFF	NA	OFF	OFF	NA	OFF
	S_SEG[5]	N/A	E10	1	LVCMOS33	8	NONE	OFF	NA	OFF	OFF	NA	OFF
	S_SEG[6]	N/A	E9	1	LVCMOS33	8	NONE	OFF	NA	OFF	OFF	NA	OFF
	S_SEG[7]	N/A	F9	1	LVCMOS33	8	NONE	OFF	NA	OFF	OFF	NA	OFF
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Figure 13: Performing Pin Assignment

4.4 Compile Design

15. Compile the design by clicking on the **Run All** arrow, see **Figure 14**.



Figure 14: Compiling the Design

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4.4 Simulate Design

16. From the Tools menu, select Simulation Wizard and click Next, see Figure 15.



Figure 15: Simulating the Design

17. Name the project **led_brightness_sim** and click **Next**, see **Figure 16**. If asked whether you want to create it, click **Yes**. Click Next to **Add and Reorder Source** and **Parse HDL files for simulation**. Click **Finish** to start the simulation.



Figure 16: Naming the Simulation





Figure 17: The ModelSim Simulation Wave View

5.0 Program the Device with Radiant Programmer

- 19. Make sure that in the Lattice Certus-NX Versa Evaluation board LFD2NX-VERSA-EVN:
- 20. there is a USB cable connecting the computer to J2
- 21. there is a 12V power supply connected to J35

22. From the Tools menu, select Programmer and a new window opens, see Figure 18.

Radiant Programmer - impl_1.xcf *					– Ö ×
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Output					5 ×
INFO - TTAG Chain Verification, No Errors					^
INEO - Check configuration seture: Successful					
INFO - Device 1 LFD2NX-40: Fast Configuration					
INFO - Operation Done. No errors.					
INFO - Elapsed time: 00 min : 10 sec					
INFO - Operation: successful.					
					~

Figure 18: Programming the FPGA

- 23. Once the cable is detected and settings are set, program the device by clicking the Program Device icon **Figure 18**.
- 24. Verify that:
 - \circ $\;$ the LED's [7:0] show the heartbeat of the system
 - the sever-segment LED displays a hexadecimal counter with the decimal point LED also being turned on whenever the count value equals F hex.

REVISION HISTORY

Date	Rev. #	Author	Change Description
3/18/2022	1.0.0	JA	Initial Release.
4/17/2023	1.0.1	JB	Completed porting App Note to Certus-NX-RT using Lattice Certus-NX Versa Evaluation board LFD2NX-VERSA-EVN

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