

# Creating Certus-NX-RT Project in Radiant Software

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PRODUCT NAME	MANUFACTURER PART NUMBER	DEVICE TYPE
Lattice Certus-NX-RT FPGA	UT24C407	RL01

**Table 1: Cross Reference of Applicable Products**

## 1.0 Overview

This document details the process of creating a **Certus-NX-RT** FPGA project using the **Lattice Radiant** software tools and the Lattice Certus-NX Versa Evaluation board LFD2NX-VERSA-EVN.

For the purposes of this document, create a project named **led\_brightness** and configure the **Radiant** tools to include all the source modules required for a successful build.

Using this template, projects are created using:


- (a) the preferred application source directory structures and
- (b) the directory structure for the **Radiant**-supplied files.



# Creating Certus-NX-RT Project in Radiant Software

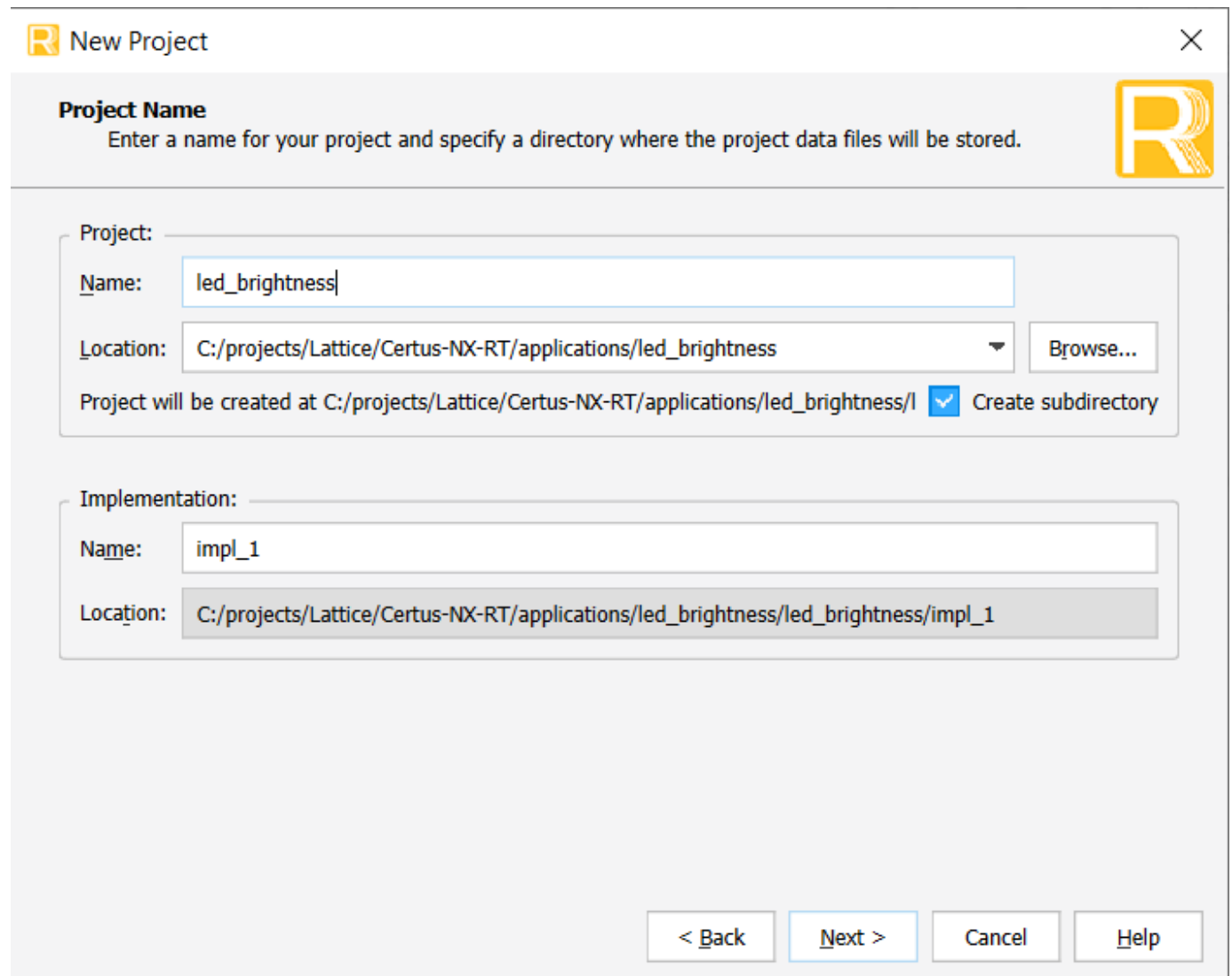
## 3.0 Creating a Design Project with Radiant Software

1. Download CreatingRadiantProject.zip from caes.com.

2. Launch Radiant Software 

3. From the **File** menu, select **New > Project...**

4. Specify the project name as **led\_brightness**, navigate to the **location** of your choice and click **Next**, see **Figure 2**.



**New Project**

**Project Name**  
Enter a name for your project and specify a directory where the project data files will be stored.

Project:  
Name: led\_brightness  
Location: C:/projects/Lattice/Certus-NX-RT/applications/led\_brightness Browse...  
Project will be created at C:/projects/Lattice/Certus-NX-RT/applications/led\_brightness/  Create subdirectory

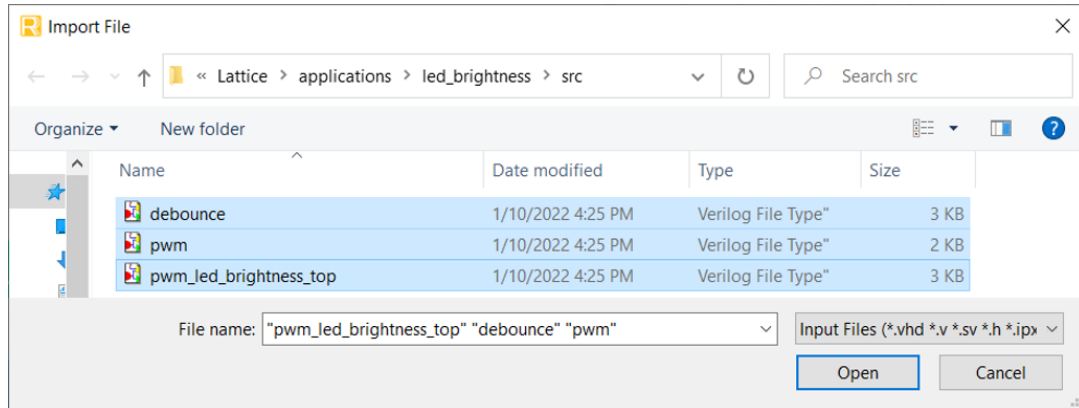
Implementation:  
Name: impl\_1  
Location: C:/projects/Lattice/Certus-NX-RT/applications/led\_brightness/led\_brightness/impl\_1

< Back Next > Cancel Help

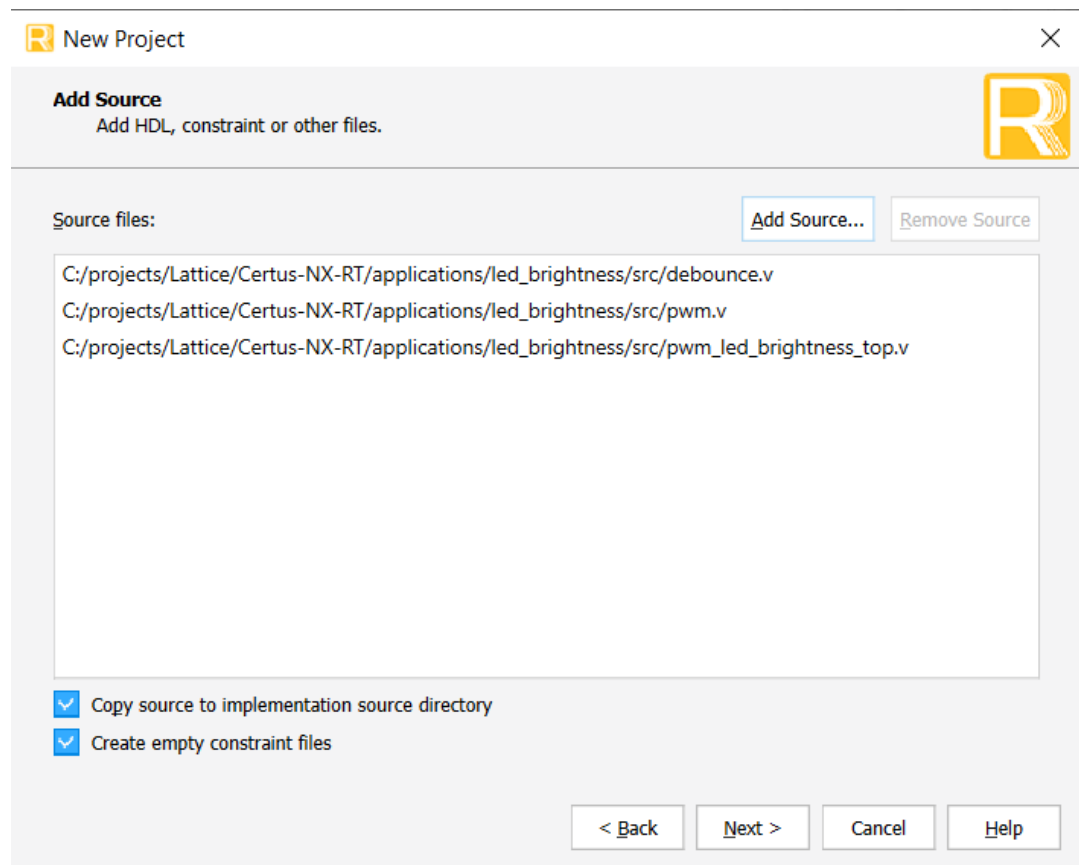
**Figure 2: Creating a Radiant Design Project**

# Creating Certus-NX-RT Project in Radiant Software

5. Select **Add Source...** and click **Open**, see **Figure 3** and **Figure 4**, click **Next**.



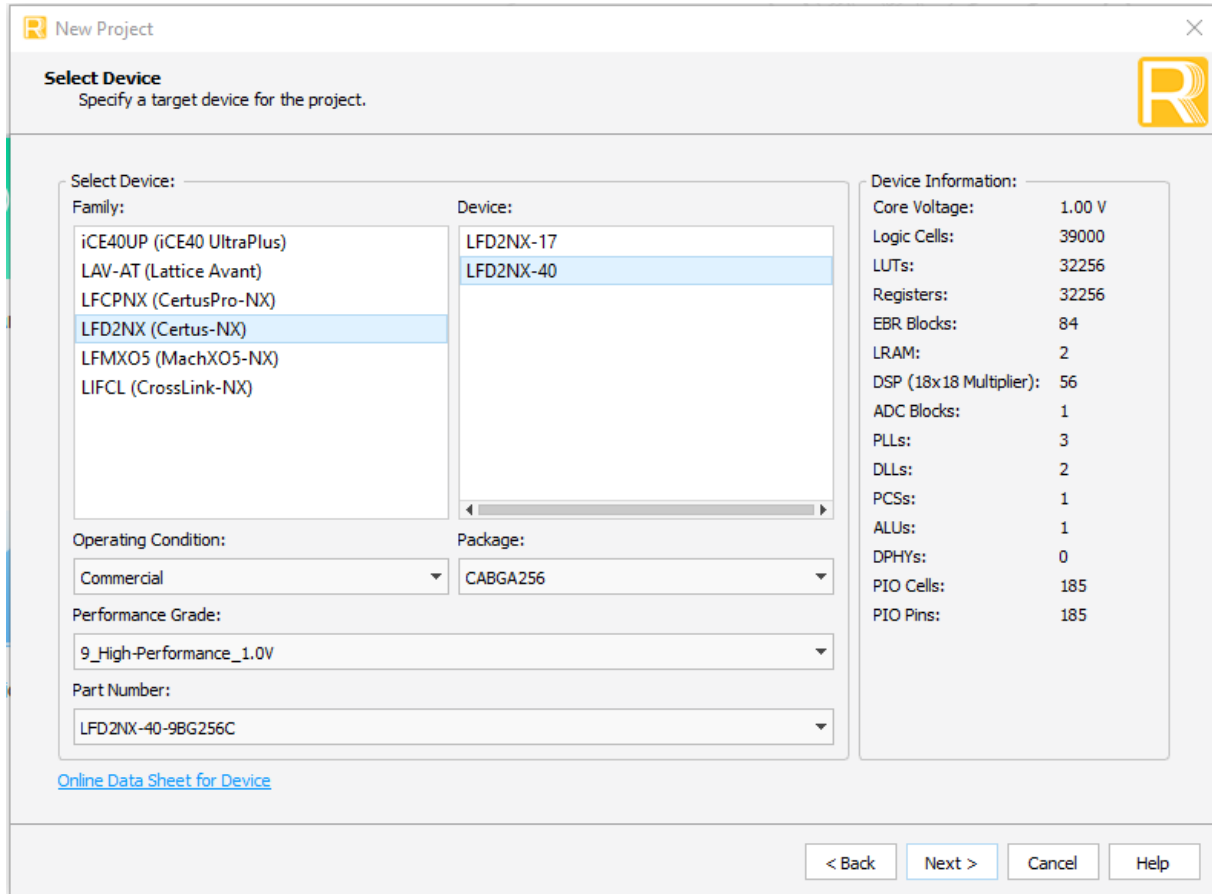
**Figure 3: Selecting Sources**



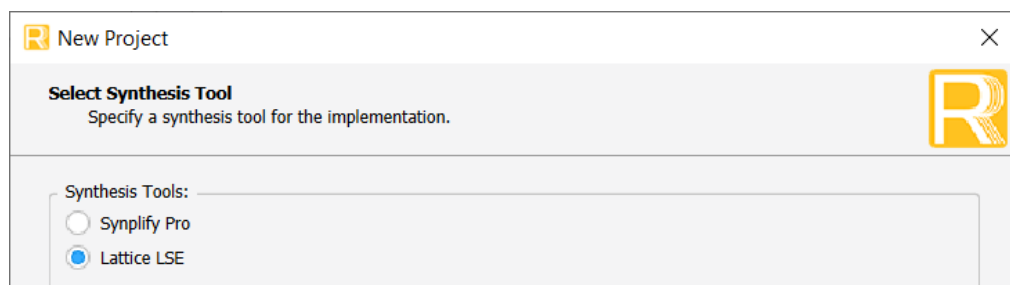
**Figure 4: Adding Sources**

# Creating Certus-NX-RT Project in Radiant Software

6. Select the appropriate device, click **Next** and choose **Lattice LSE**; click **Next** and **Finish**, see **Figure 5**.



**Figure 5: Selecting the FPGA Device**



**Figure 6: Selecting the Synthesis Tool**

7. The initial project with the provided files should look like **Figure 7**.

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The screenshot displays the Lattice Radiant Software Reports window for a project named 'led\_brightness'. The interface includes a menu bar (File, Edit, View, Project, Tools, Window, Help), a toolbar with various icons, and a progress bar showing the current step: 'Export Files'. The left sidebar shows a project tree with folders for 'Strategies', 'Input Files', 'Pre-Synthesis Constraint Files', 'Post-Synthesis Constraint Files', and 'Debug Files'. The main area is divided into two panes: 'Reports' and 'Led\_brightness Project Summary'.

**Reports**

- Project Summary
- Synthesis Reports
- Map Reports
- Place & Route Reports
- Export Reports
- Misc Reports

**Led\_brightness Project Summary**

Implementation Name:	impl_1	Performance Grade:	9_High-Performance_1.0V
Strategy Name:	Strategy1	Operating Condition:	COM
Part Number:	LFD2NX-40-9BG256C	Synthesis:	Lattice LSE
Family:	LFD2NX	Timing Errors:	
Device:	LFD2NX-40	Project Created:	2022/03/18 09:15:00
Package:	CABGA256	Project Updated:	2022/03/18 09:15:01
Project File:	C:/projects/Lattice/Certus-NX-RT/applications/led_brightness/led_brightness/led_brightness.rdf		
Implementation Location:	C:/projects/Lattice/Certus-NX-RT/applications/led_brightness/led_brightness/impl_1		

**Resource Usage**

LUT4:	0	IO Buffers:	0
PFU Register:	0	EBR:	0

The bottom pane shows a terminal window with the following commands:

```

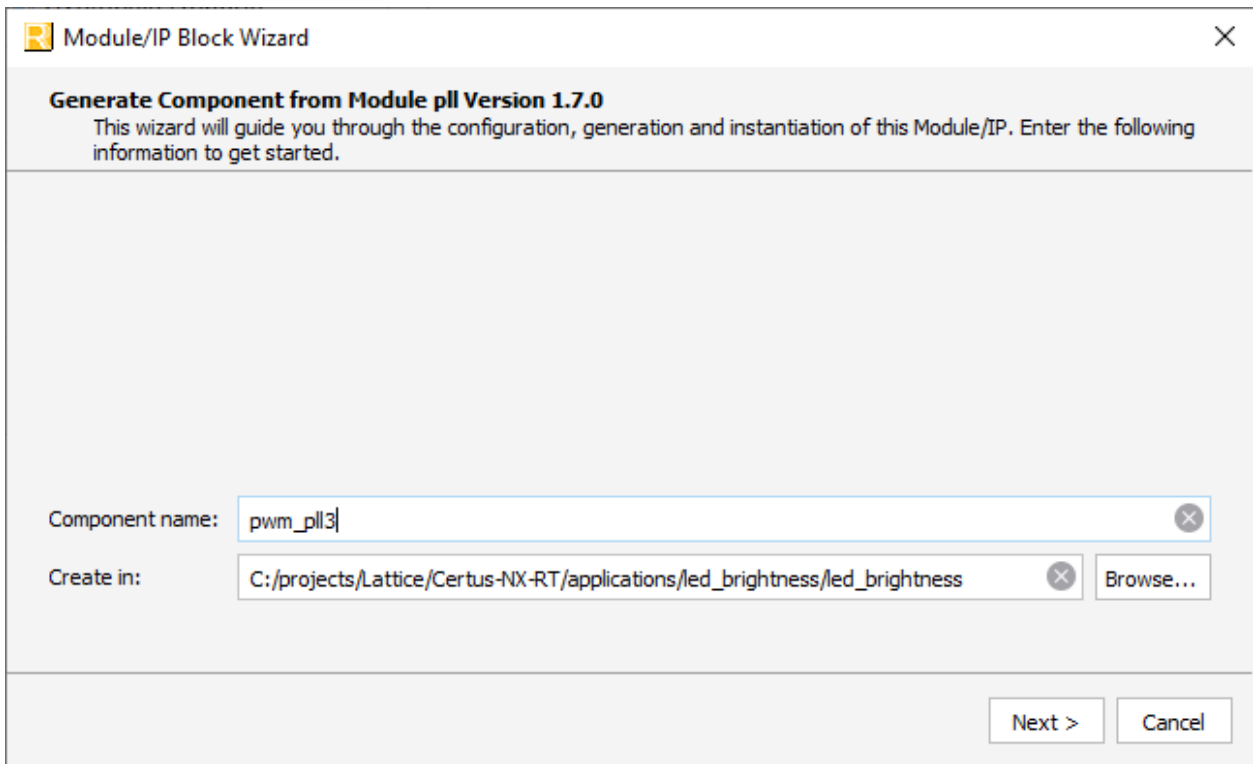
> prj_create -name "led_brightness" -impl "impl_1" -dev LFD2NX-40-9BG256C -performance "9_High-Performance_1.0V" -synthesis "lse"
> prj_add_source "C:/projects/Lattice/Certus-NX-RT/applications/led_brightness/led_brightness/source/impl_1/impl_1.sdc" "C:/projects/Lattice/Certus-NX-RT/applications/led_brightness/led_brightness/src/debounce.v" "C:/projects/Lattice/Certus-NX-RT/applications/led_brightness/led_brightness/src/debounce.v"
> prj_save

```

Figure 7: An Example of an Initial Project

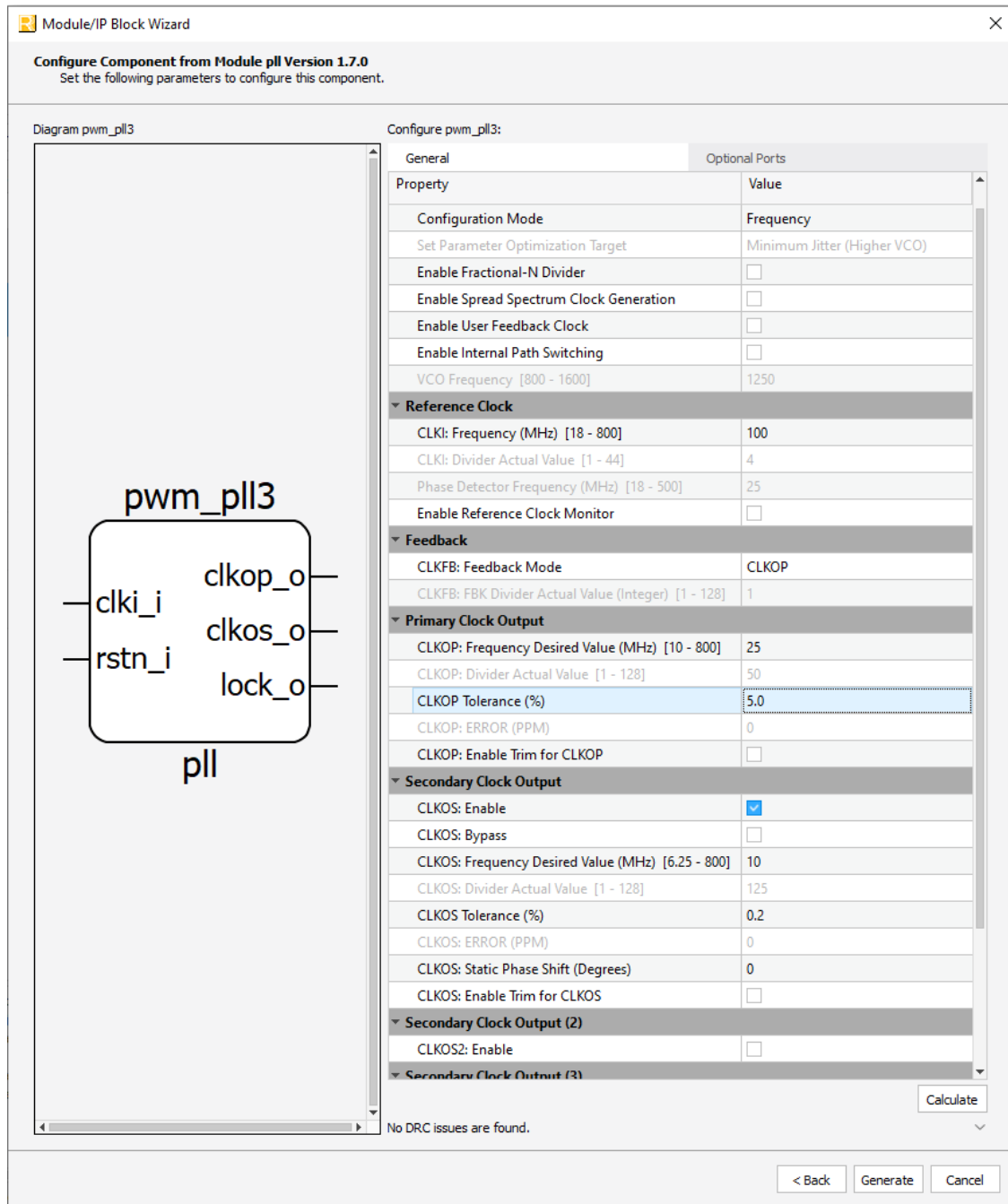
# Creating Certus-NX-RT Project in Radiant Software

- From the **IP Catalog Architecture Modules**, add a **PLL** module with the options shown below and name it **pwm\_pll3**, see **Figure 8** and **Figure 9**.



**Figure 8: Opening the IP Catalog**

# Creating Certus-NX-RT Project in Radiant Software



**Figure 9: Adding a PLL from the IP Catalog**

- Once the **PLL** options are entered, click the Generate button to start the creation of the module.
- ON the next screen, click the **Finish** button to complete the creation of the module.



# Creating Certus-NX-RT Project in Radiant Software

11. Once the **PLL** is created, it is added to the project files, see **Figure 10**.

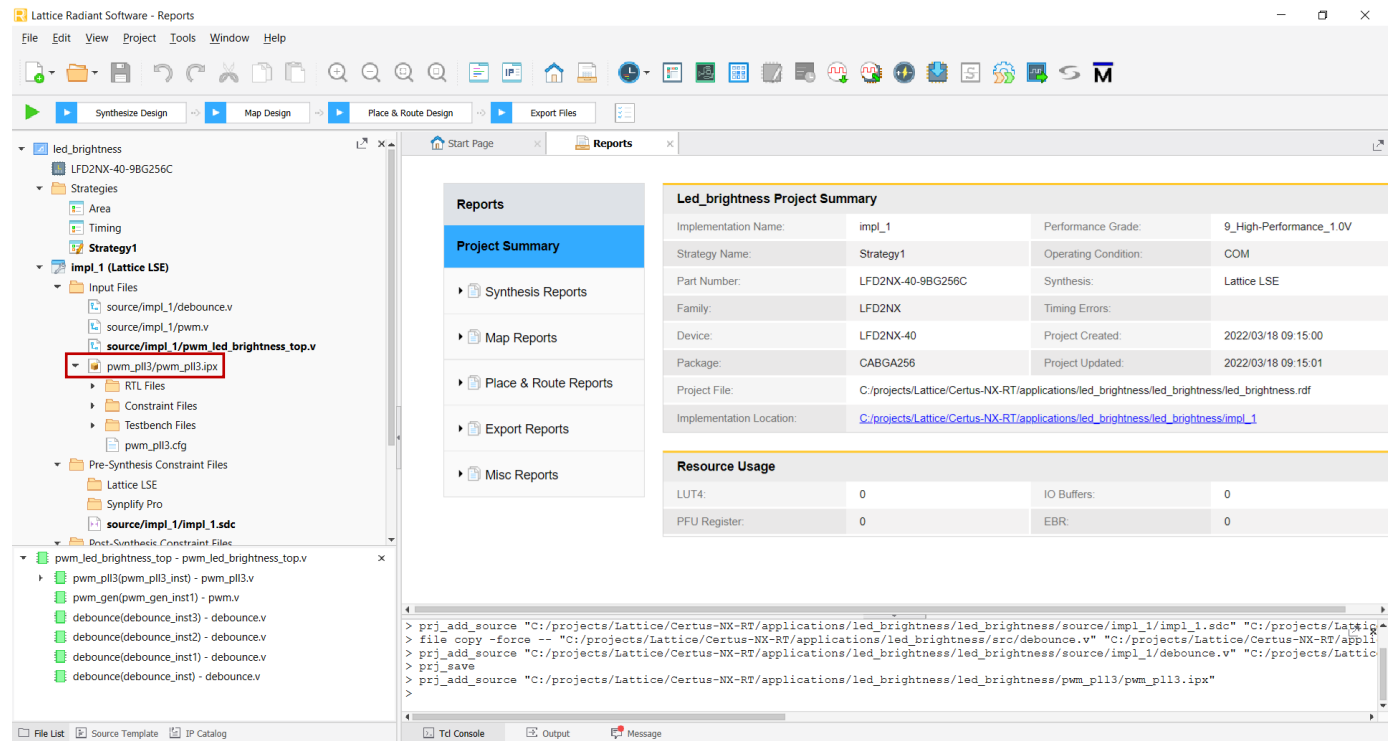


Figure 10: Looking at the Recently Added PLL IP

# Creating Certus-NX-RT Project in Radiant Software

## 4.0 Compile Design using Radiant Software

### 4.1 Set Top Level File

- From the **Project** menu, select **Active Implementation** > **Set Top-Level Unit...** and set **pwm\_led\_brightness\_top.v** as the top level file, see **Figure 11**.

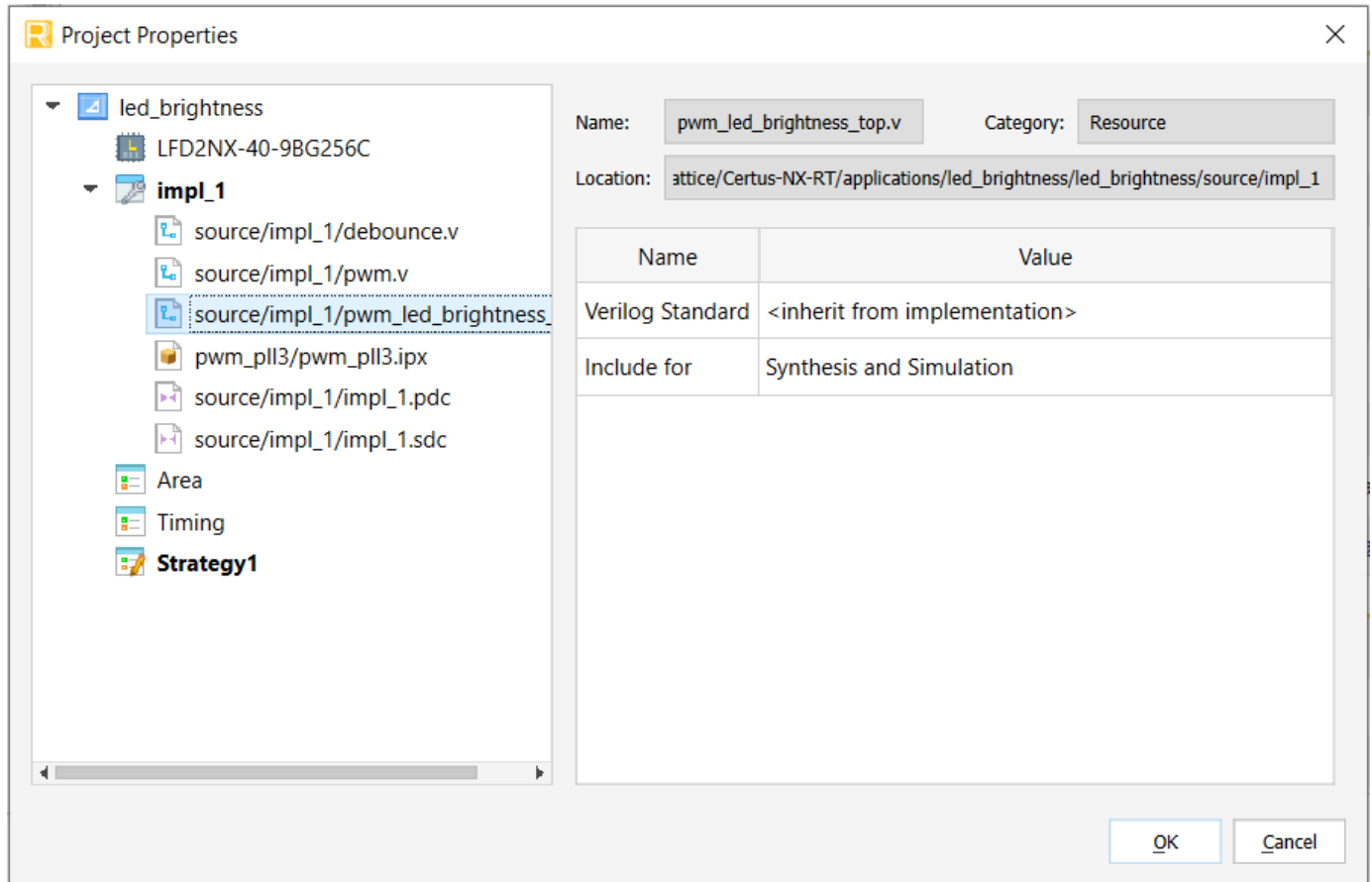


Figure 11: Setting a Top Level File

# Creating Certus-NX-RT Project in Radiant Software

## 4.2 Synthesize Design

13. Synthesize the design by clicking on the **Synthesize Design** arrow, see **Figure 12**.

The screenshot shows the Lattice Radiant Software interface during the synthesis process. The 'Synthesize Design' button in the top toolbar is highlighted with a red box. The main window displays the 'Reports' section, which includes a 'Project Summary' table and a 'Resource Usage' table. The console at the bottom shows the execution of synthesis commands.

Led_brightness Project Summary			
Implementation Name:	impl_1	Performance Grade:	9_High-Performance_1_0V
Strategy Name:	Strategy1	Operating Condition:	COM
Part Number:	LFD2NX-40-9BG256C	Synthesis:	Lattice LSE
Family:	LFD2NX	Timing Errors:	
Device:	LFD2NX-40	Project Created:	2022/03/18 09:15:00
Package:	CABGA256	Project Updated:	2022/03/18 09:15:01
Project File:	C:/projects/Lattice/Certus-NX-RT/applications/led_brightness/led_brightness/led_brightness.rdf		
Implementation Location:	C:/projects/Lattice/Certus-NX-RT/applications/led_brightness/led_brightness/impl_1		

Resource Usage			
LUT4:	63	IO Buffers:	13
PFU Register:	137	EBR:	0

```

> file copy -force -- "C:/projects/Lattice/Certus-NX-RT/applications/led_brightness/src/debounce.v" "C:/projects/Lattice/Certus-NX-RT/applications/led_brightness/impl_1/debounce.v"
> prj_add_source "C:/projects/Lattice/Certus-NX-RT/applications/led_brightness/led_brightness/source/impl_1/debounce.v" "C:/projects/Lattice/Certus-NX-RT/applications/led_brightness/impl_1/pwm.v"
> prj_save
> prj_add_source "C:/projects/Lattice/Certus-NX-RT/applications/led_brightness/led_brightness/pwm_pll3/pwm_pll3.ipx"
> prj_run_Synthesis -impl impl_1
  
```

**Figure 12: Synthesizing the Design**

# Creating Certus-NX-RT Project in Radiant Software

## 4.3 Pin Assignment (Device Constraint Editor)

14. Once the design has been synthesized, use the **Device Constraints Editor** option of the **Tools** drop down menu to assign the pin numbers to their respective signals, see **Figure 13**.

The screenshot shows the Device Constraint Editor interface. At the top, there is a menu bar (File, Edit, View, Design, Window, Help) and a toolbar with icons for save, undo, redo, and search. On the left, there is a tree view showing 'Ports', 'Instances(86)', and 'Nets'. The main area displays a grid of pins (A-D, 1-16) with colored circles indicating assignments. Below the grid is a table with the following columns: Name, Group By, Pin, BANK, IO\_TYPE, DRIVE, PULLMODE, CLAMP, DIFFDRIVE, DIFFRESISTOR, GLITCHFILTER, HYSTERESIS, and OPENDRAIN.

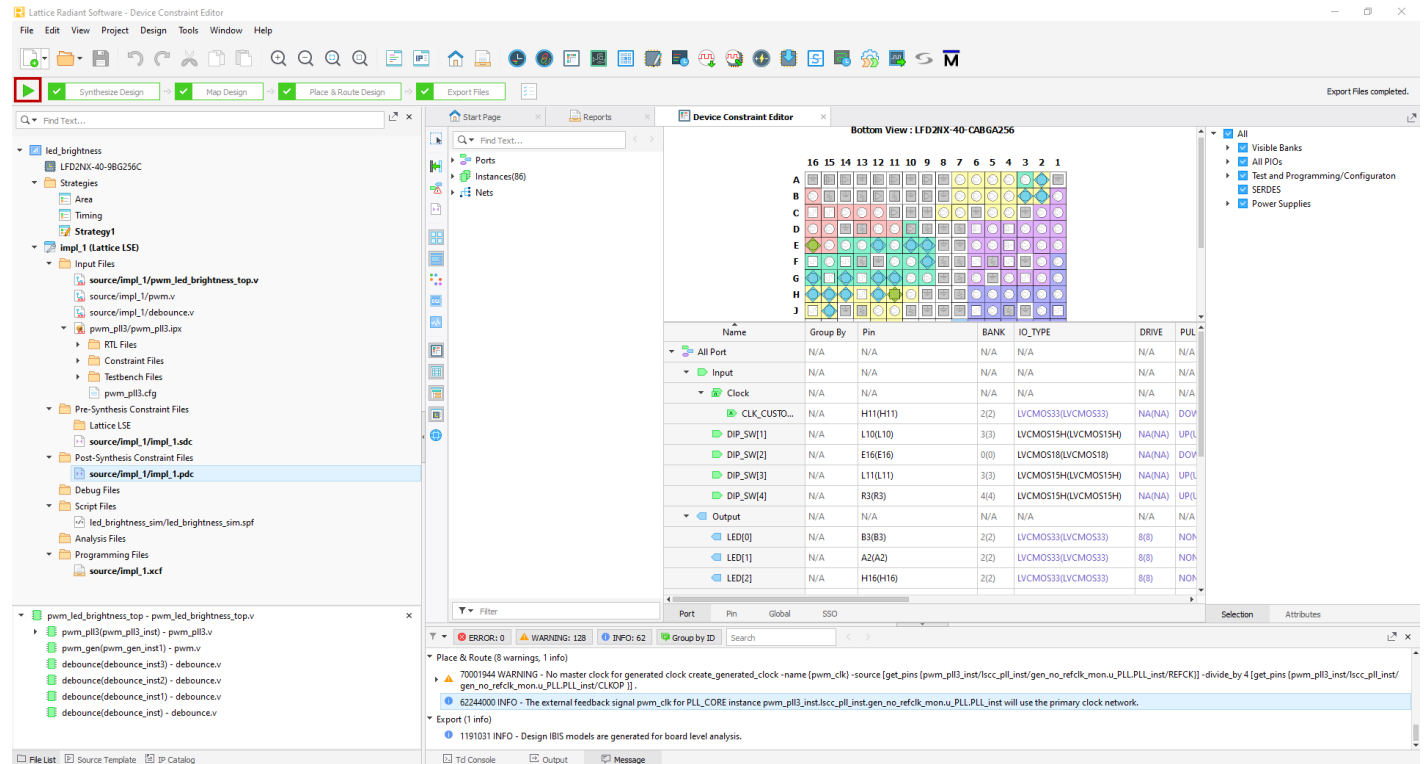
Name	Group By	Pin	BANK	IO_TYPE	DRIVE	PULLMODE	CLAMP	DIFFDRIVE	DIFFRESISTOR	GLITCHFILTER	HYSTERESIS	OPENDRAIN
▼ All Port	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
▼ Input	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
▼ Clock	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
▶ CLK_CUSTO...	N/A	H11	2	LVCMOS33	NA	DOWN	ON	NA	OFF	ON	ON	OFF
▶ DIP_SW[1]	N/A	L10	3	LVCMOS15H	NA	UP	ON	NA	OFF	OFF	ON	OFF
▶ DIP_SW[2]	N/A	E16	0	LVCMOS18	NA	DOWN	ON	NA	OFF	ON	ON	OFF
▶ DIP_SW[3]	N/A	L11	3	LVCMOS15H	NA	UP	ON	NA	OFF	OFF	ON	OFF
▶ DIP_SW[4]	N/A	R3	4	LVCMOS15H	NA	UP	ON	NA	OFF	OFF	ON	OFF
▼ Output	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
▶ LED[0]	N/A	B3	2	LVCMOS33	8	NONE	OFF	NA	OFF	OFF	NA	OFF
▶ LED[1]	N/A	A2	2	LVCMOS33	8	NONE	OFF	NA	OFF	OFF	NA	OFF
▶ LED[2]	N/A	H16	2	LVCMOS33	8	NONE	OFF	NA	OFF	OFF	NA	OFF
▶ LED[3]	N/A	B2	2	LVCMOS33	8	NONE	OFF	NA	OFF	OFF	NA	OFF
▶ LED[4]	N/A	H15	2	LVCMOS33	8	NONE	OFF	NA	OFF	OFF	NA	OFF
▶ LED[5]	N/A	H14	2	LVCMOS33	8	NONE	OFF	NA	OFF	OFF	NA	OFF
▶ LED[6]	N/A	H12	2	LVCMOS33	8	NONE	OFF	NA	OFF	OFF	NA	OFF
▶ LED[7]	N/A	J15	2	LVCMOS33	8	NONE	OFF	NA	OFF	OFF	NA	OFF
▶ S_SEG[0]	N/A	G16	1	LVCMOS33	8	NONE	OFF	NA	OFF	OFF	NA	OFF
▶ S_SEG[1]	N/A	G14	1	LVCMOS33	8	NONE	OFF	NA	OFF	OFF	NA	OFF
▶ S_SEG[2]	N/A	G12	1	LVCMOS33	8	NONE	OFF	NA	OFF	OFF	NA	OFF
▶ S_SEG[3]	N/A	G11	1	LVCMOS33	8	NONE	OFF	NA	OFF	OFF	NA	OFF
▶ S_SEG[4]	N/A	E12	1	LVCMOS33	8	NONE	OFF	NA	OFF	OFF	NA	OFF
▶ S_SEG[5]	N/A	E10	1	LVCMOS33	8	NONE	OFF	NA	OFF	OFF	NA	OFF
▶ S_SEG[6]	N/A	E9	1	LVCMOS33	8	NONE	OFF	NA	OFF	OFF	NA	OFF
▶ S_SEG[7]	N/A	F9	1	LVCMOS33	8	NONE	OFF	NA	OFF	OFF	NA	OFF

**Figure 13: Performing Pin Assignment**

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## 4.4 Compile Design

15. Compile the design by clicking on the **Run All** arrow, see **Figure 14**.



**Figure 14: Compiling the Design**

# Creating Certus-NX-RT Project in Radiant Software

## 4.4 Simulate Design

16. From the **Tools** menu, select **Simulation Wizard** and click **Next**, see **Figure 15**.

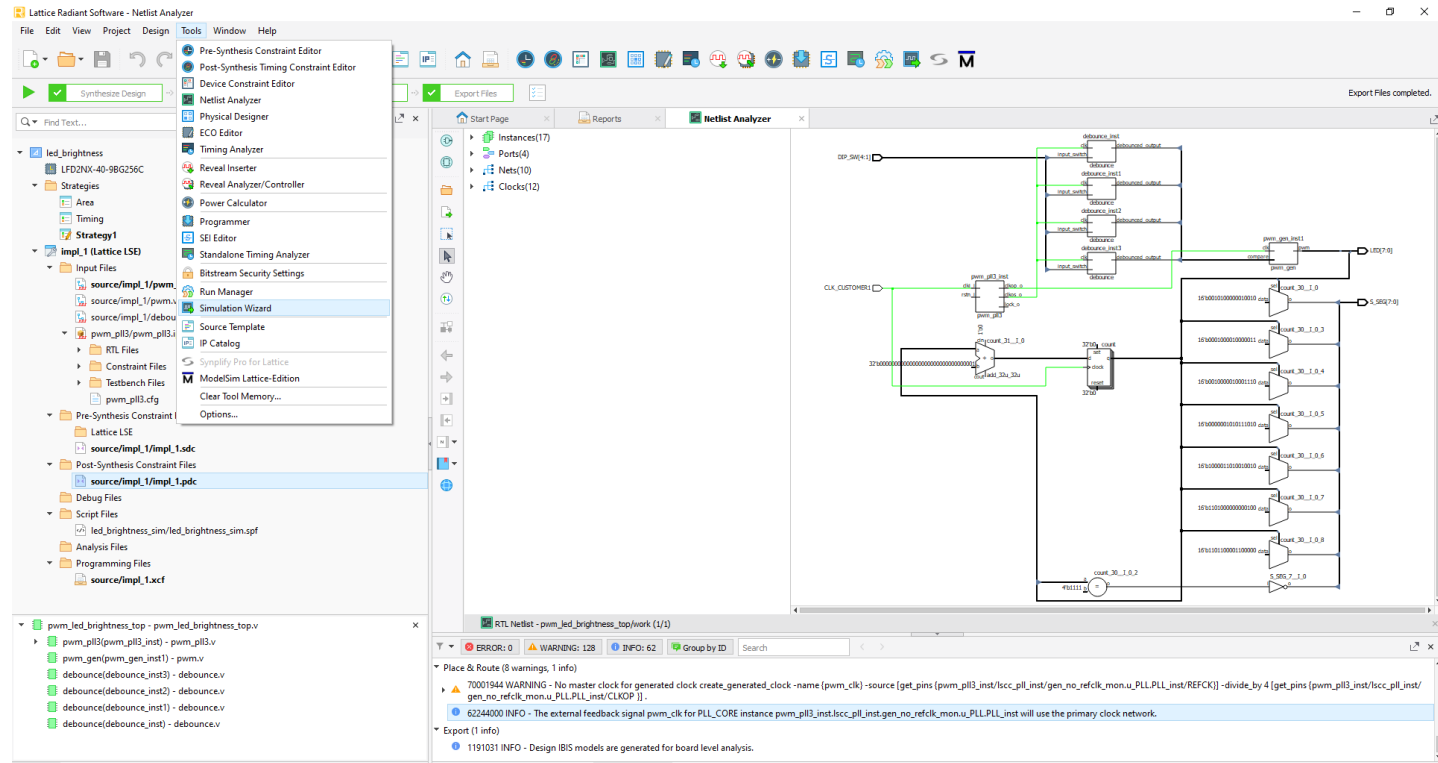


Figure 15: Simulating the Design

# Creating Certus-NX-RT Project in Radiant Software

17. Name the project **led\_brightness\_sim** and click **Next**, see **Figure 16**. If asked whether you want to create it, click **Yes**. Click Next to **Add and Reorder Source** and **Parse HDL files for simulation**. Click **Finish** to start the simulation.

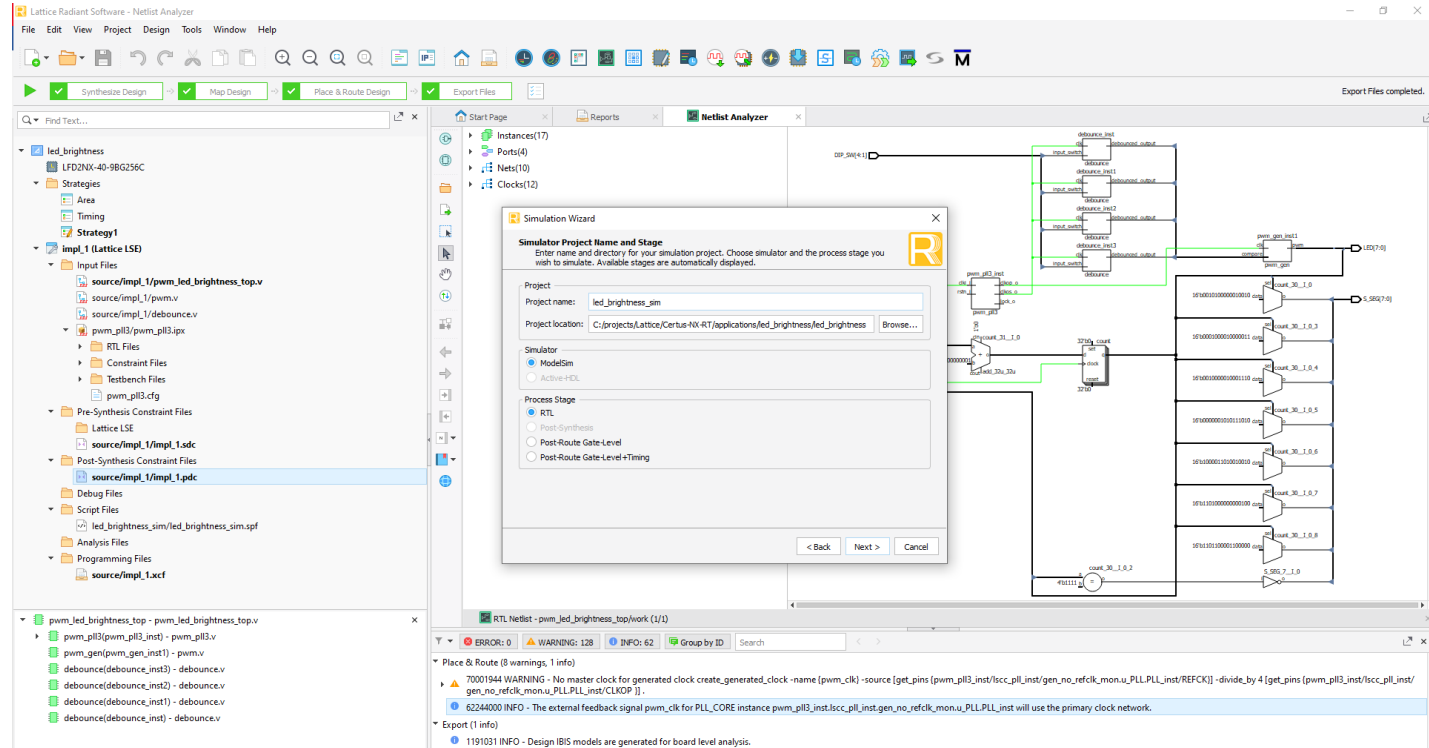


Figure 16: Naming the Simulation

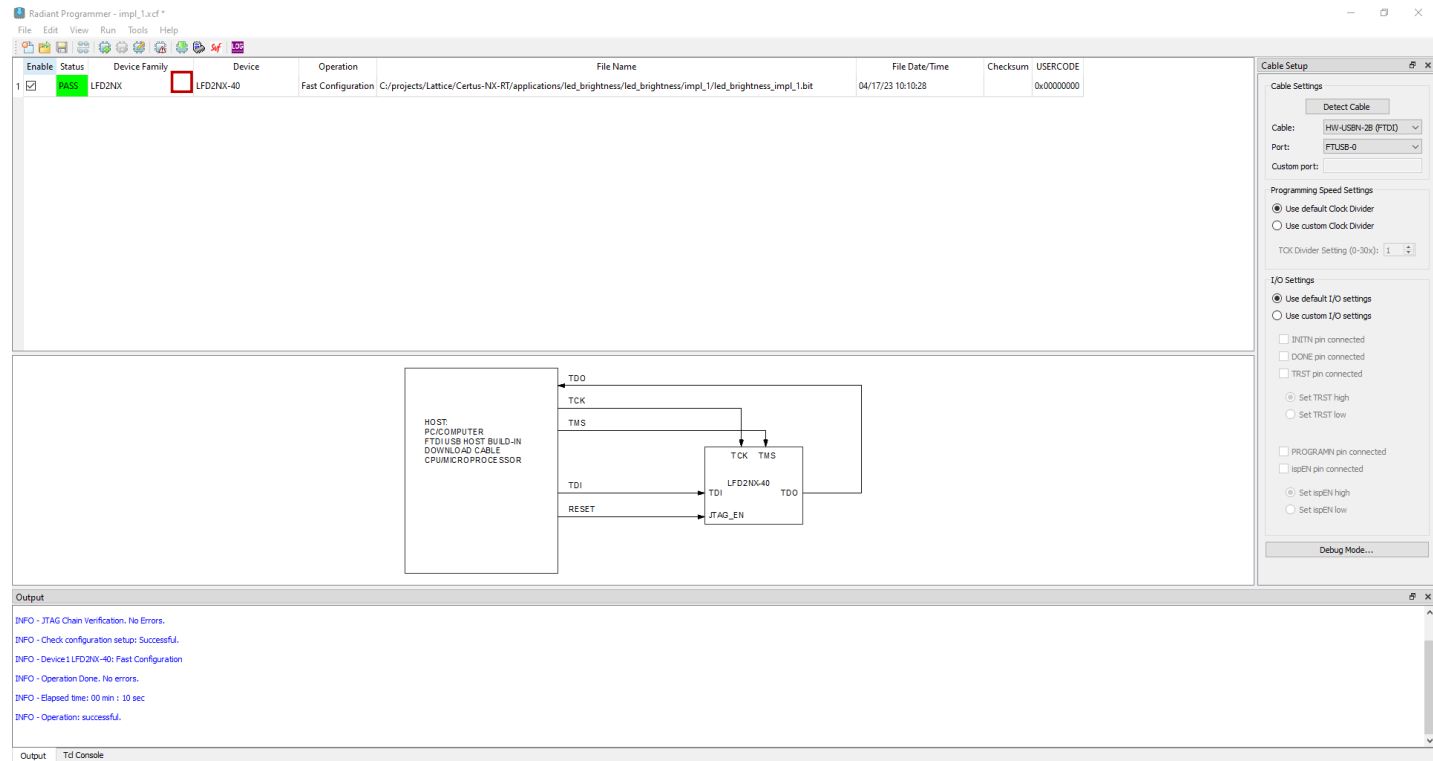





# Creating Certus-NX-RT Project in Radiant Software

## 5.0 Program the Device with Radiant Programmer

19. Make sure that in the Lattice Certus-NX Versa Evaluation board LFD2NX-VERSA-EVN:
20. there is a USB cable connecting the computer to J2
21. there is a 12V power supply connected to J35
22. From the **Tools** menu, select **Programmer** and a new window opens, see **Figure 18**.



**Figure 18: Programming the FPGA**

23. Once the cable is detected and settings are set, program the device by clicking the Program Device icon , **Figure 18**.
24. Verify that:
  - the LED's [7:0] show the heartbeat of the system
  - the seven-segment LED displays a hexadecimal counter with the decimal point LED also being turned on whenever the count value equals F hex.

# Creating Certus-NX-RT Project in Radiant Software

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## REVISION HISTORY

Date	Rev. #	Author	Change Description
3/18/2022	1.0.0	JA	Initial Release.
4/17/2023	1.0.1	JB	Completed porting App Note to Certus-NX-RT using Lattice Certus-NX Versa Evaluation board LFD2NX-VERSA-EVN

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