FRONTGRADE

SINGLE BOARD COMPUTERS

4350301-30x Sphinx SBC

SmallSat Command and Data Handling Module

REV.0001

9/11/2024

FEATURES

- ❑ Dual-core LEON3FT GR712RC microprocessor with up to 180 DMIPS processing speed at up to 90MHz system clock rate
  - ✓ Branch prediction and on-the-fly error correction resulting in 30% performance increase compared to single-core LEON3FT
  - ✓ 4x4 Kbytes instruction and data cache
  - ✓ On-chip Debug Unit with instruction and AHB (advance high-performance bus) trace buffers
  - ✓ Microprocessor JTAG debug link
- ❑ Flight Reconfigurable ProASIC3L Flash family FPGA with customizable firmware to meet mission-specific customer requirements
- ❑ Part List selection options for Class-D/C and high-reliability Class-B missions (QML Q/V , EEE-INST Level 1)
- ❑ VxWorks 6.7 compatible Board Support Package with native driver support for I^2C and NAND Flash controllers and OS agnostic bootloader
- ❑ EDAC-protected Memories:
  - ✓ 384MB SDRAM and controller (or 3Gbit) with Reed-Solomon EDAC protection (16-bit word level 256MB User Data Space +128MB EDAC)
  - ✓ 32MB NOR Flash and controller with BCH EDAC protection (16-bit word level)
  - ✓ 8GB or 16GB density options for user data NAND Flash with Hamming EDAC protection (64-bit word level)
  - ✓ 192 KB microprocessor OCM and controller with BCH EDAC protection (16-bit word level)
- ❑ System-level functions and features:
  - ✓ 6 X General Purpose Timers (2 with time latch capability)
  - ✓ FPGA Watchdog and Timekeeping timers
  - ✓ Fault Detection and Mitigation Unit (FPGA)
  - ✓ Supports up to four FSW boot images with image selection
  - ✓ Interfaces with IRIS and ACS systems (Star Tracker, IMU, Sunsors, Cold Gas)
- ❑ Interfaces:
  - ✓ 2x SpaceWire links with RMAP (GR712RC)
  - ✓ Up to 8x Asynchronous RS422 serial links with added Mezzanine Card
  - ✓ 4x SPI Master Ports (up to 16 slave-select bits)
  - ✓ Single I^2C multi-master core, with 7-bit or 10-bit mode slave-select addressing (GR712RC)
  - ✓ 32 GPIO (18 on GR712RC and 14 on FPGA)
  - ✓ Up to 26 analog channels with added Mezzanine Crad
  - ✓ Up to 24 high-precision current sources with added Mezzanine Card
  - ✓ 2x JTAG Interface (GR712 and FPGA)
  - ✓ Ethernet Interface (GR712RC)

OPERATIONAL ENVIRONMENT

- ❑ Temperature Range: -25°C to +65°C
- ❑ Total Dose: ≥ 25 kRad (Si)
- ❑ SEL Immune: ≥ 51.2 MeV-cm^2/mg
- ❑ Power Supply: Single 5V +/-5% power rail, on-board down-converted and regulated to 1.5V, 1.8V and 3.3V.

APPLICATIONS

- ❑ Command and Data Handling (C&DH) systems
- ❑ Avionics for Deep space Small Sats and Cube Sats

INTRODUCTION

The 4350301-30x Sphinx Single Board Computer (SBC) is a 1U/PC104 form factor processing platform based on the Frontgrade Gaisler GR712RC dual-core LEON3FT microprocessor, ideally suited for the Size, Weight, Power and Cost (SWaPc) sensitive applications. With a board size of only 100mm x 94mm, launch weight of 160gr and power dissipation of less than 3W typical, the Sphinx SBC is ideally suited for deep space Small Sat and Cube Sat missions as well as LEO missions of large population constellations, with predicted reliability and survival rates compatible with NASA Class-D/C mission requirements. The FLASH based flight re-programmable ProASIC3L FPGA, makes this SBC a highly versatile platform, customizable for a wide range of customer-specific applications, with minimal hardware, firmware, and BSP modifications and upgrades.

1. SPHINX SBC FUNCTIONAL DESCRIPTION

1.1. Overview

Figure 1.1 illustrates the functional block diagram and physical appearance of the Sphinx SBC.

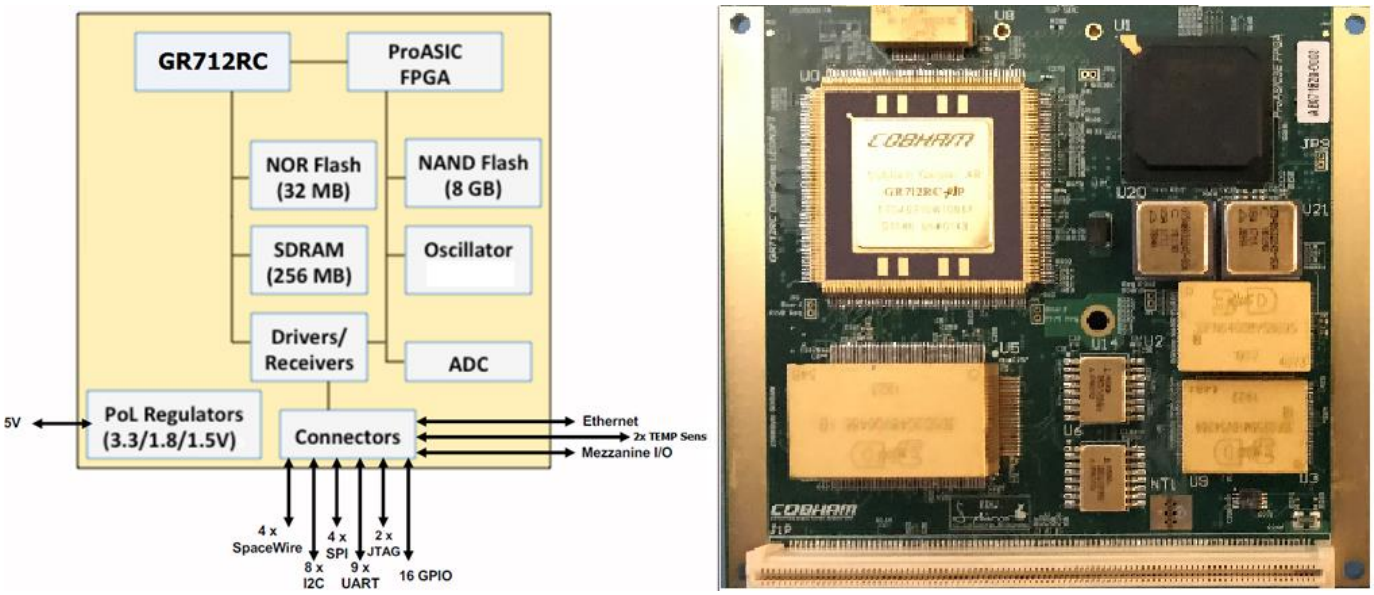

Figure 1.1: Sphinx SBC Functional Block Diagram and Form Factor

The GR712RC dual-core LEON3FT System-on-Chip (SoC) is the main microprocessor that runs the application software and controls the various memory and other peripherals such as the NOR flash and SDRAM. The Microchip ProASIC3L FPGA provides additional functions such as NAND Flash control, clock management, power management, and other interface functions. The NOR flash memory stores the boot-up code, the FSW code image, and some system parameters. There are two types of connectors on board. The 200-pin stacking connectors are used to provide connections among slices on the same system stack. The single Nano-D connector provides interfaces to Ground System Equipment (GSE) and other IOs off the stack. The board receives an external regulated 5V power supply and down-converts it to the required 1.5V, 1.8V, and 3.3V on-board voltage rails. The Sphinx SBC operates with an on-board clock source oscillator running at 90MHz. The FPGA uses this clock source to drive the SpaceWire and the main system clock on GR712RC microprocessor.. The ProASIC3L FPGA communicates with the GR712RC CPU through a memory mapped IO interface. Through this interface, the GR712RC is able to read and write to the address space of the FPGA. The FPGA is regarded as a slave device to the CPU and cannot initiate any instructions or data transactions towards the CPU.

2. PROASIC3L FPGA FIRMWARE FUNCTIONAL DESCRIPTION

2.1. FPGA Watchdog and Timekeeping Timers

The Watchdog block of FPGA firmware ensures both the FPGA logic and CPU are brought up only after all three on-board regulated power supplies stabilize. If any power supply regulator de-asserts its digital “OK” signal for more than 25 nanoseconds, both the FPGA and CPU will be reset. This logic is also capable of resetting just the CPU if such a reset is requested via the watchdog flag. This flag is generated by a timer hardware unit within the CPU (with interrupts enabled) and monitored by FPGA firmware. The FPGA firmware also incorporates Spacecraft Timekeeping and Spacecraft Uptime timers which track the number of seconds (in microsecond resolution) the time since power-on. Both of these timer modules are provided via a software interface to the standard memory map of the FPGA. The FPGA firmware also implements an EPS Heartbeat signal with a period of 2.5 microseconds and pulse duration of 250 nanoseconds as well as a dedicated spacecraft time synchronization payload pulse-per-second (PPS) SC_TIME_SYNC signal.

2.2. FPGA FDMU (Fault Detection and Mitigation Unit)

Fault Detection and Mitigation Unit keeps a close watch on the GR712RC microprocessor. In the event that the microprocessor is trapped into a state that disables the watchdog and spacecraft timers, the FDMU will be able to detect this state and perform a CPU reset. Figure 2 shows the top-level functional block diagram of the FDMU module.

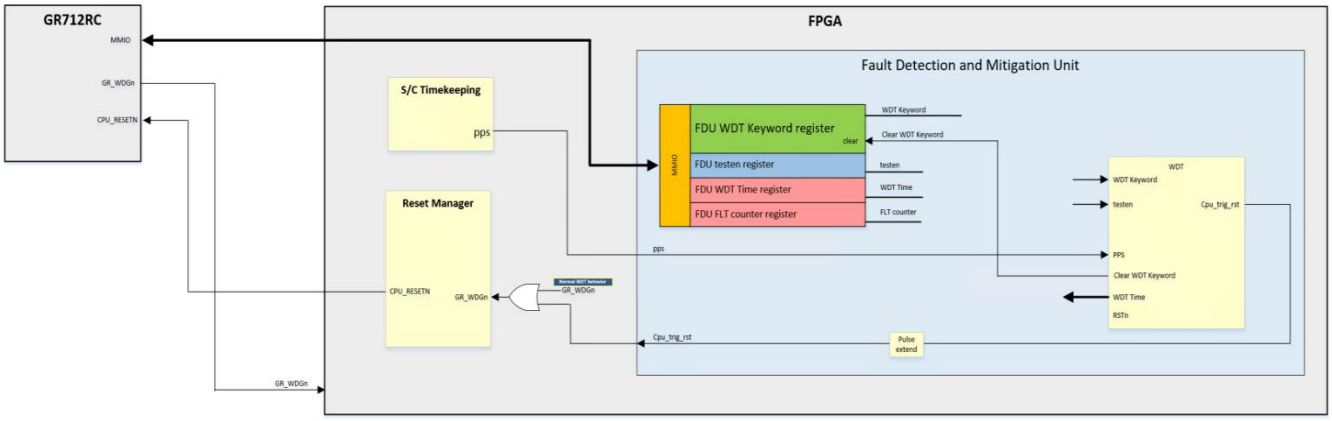

Figure 2.1 ProASIC3L FPGA FDMU Functional Block Diagram

3. SPHIX SBC OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
VDD	Main Power Supply	4.75	5.0	5.25	V
PD	Power Dissipation	1.5	3.0	7.0	W
TID	Total Ionizing Dose			2.5E4	rad (Si)
SEL	Single Event Latchup Immunity			51.2	MeV*cm2/mg
LW	Launch Weight		0.16		kg

4. SPHINX SBC PHYSICAL DESCRIPTION AND CONNECTOR PIN ALLOCATION

4.1. 200-Pin Stacking Connectors Pin Description

Two 200-pin stacking connectors placed on the opposite sides of the PWB, are used for inter-board connections within the spacecraft stack. Table 1 shows the pinout assignments and configuration.

Table 1: 200-Pin Stacking Connectors Pinout

Sphinx Pin-Name	Pin No.	Pin No.	Sphinx Pin-Name
ADC_CSn	1	2	**ADC_DIN**
ADC_SCLK	**3**	**4**	**ADC_DOUT**
GND	**5**	**6**	**GND**
XCVR_EN	**7**	**8**	**EPS_HB**
ANALOG_0	**9**	**10**	**ANALOG_1**
GND	**11**	**12**	**GND**
SPI0_CLK	**13**	**14**	**SPI0_MISO**
SPI0_MOSI	**15**	**16**	**SPI1_CLK**
SPI1_MISO	**17**	**18**	**SPI1_MOSI**
SPI2_CLK	**19**	**20**	**SPI2_MISO**
SPI2_MOSI	**21**	**22**	**SPI0_SS2**
GND	**23**	**24**	**GND**
I2C0_SCL	**25**	**26**	**I2C0_SDA**
SPI0_SS3	**27**	**28**	**SPI1_SS0**
UART0_TX	**29**	**30**	**UART0_RX**
SPI1_SS1	**31**	**32**	**SPI2_SS0**
SPI3_MISO	**33**	**34**	**SPI3_MOSI**
GND	**35**	**36**	**GND**
GPIO_GINT0	**37**	**38**	**GPIO_GINT1**
GPIO_GINTOUT0	**39**	**40**	**UART2_RX**
GPIO_GINOUT0	**41**	**42**	**UART3_RX**
SPI2_SS2	**43**	**44**	**SPI3_SS0**
SPI3_SS1	**45**	**46**	**SPI3_SS2**
UART7_TX_P	**47**	**48**	**UART7_TX_N**

UART7_RX_N	49	50	UART7_RX_P
GND	51	52	GND
SPW0_RXD_P	53	54	SPW0_RXD_N
SPW0_RXS_P	55	56	SPW0_RXS_N
SPW0_TXD_N	57	58	SPW0_TXD_P
SPW0_TXS_N	59	60	SPW0_TXS_P
GND	61	62	GND
SPW1_RXD_P	63	64	SPW1_RXD_N
SPW1_RXS_P	65	66	SPW1_RXS_N
SPW1_TXD_N	67	68	SPW1_TXD_P
SPW1_TXS_N	69	70	SPW1_TXS_P
GND	71	72	GND
UART4_TX_P	73	74	UART4_TX_N
UART4_RX_N	75	76	UART4_RX_P
UART5_TX_P	77	78	UART5_TX_N
UART5_RX_N	79	80	UART5_RX_P
UART6_TX_P	81	82	UART6_TX_N
UART6_RX_N	83	84	UART6_RX_P
UART8_TX	85	86	UART8_RX
GND	87	88	GND
GPIO_FOUT0_PWM	89	90	GPIO_FOUT1
GPIO_GINTOUT1	91	92	GPIO_GINTOUT2
GPIO_GINT2	93	94	GPIO_GIN0
GPIO_GINOUT1	95	96	GPIO_GINOUT2
GPIO_GIN1	97	98	GPIO_GIN2
GPIO_GIN3	99	100	GPIO_GIN4
GPIO_FOUT2_PWM	101	102	GPIO_FOUT3
GPIO_GIN5	103	104	GPIO_GIN6
GPIO_GINT3	105	106	GPIO_GINT4
GND	107	108	GND
GPIO_GINT5	109	110	SC_TIME_SYNC
GPIO_FIN0	111	112	GPIO_FIN1
GPIO_FIN2	113	114	GPIO_FIN3
GPIO_FIN4	115	116	GPIO_FIN5
GPIO_FIN6	117	118	GPIO_FIN7
SPI2_SS1	119	120	SPI3_CLK
SPI0_SS1	121	122	SPI0_SS0
UART2_TX_GR	123	124	UART3_TX
GND	125	126	GND
SSI0_CLKO	127	128	SSI1_CLKO
SSI0_FRAMEO	129	130	SSI1_FRAMEO
SSI0_DATAO	131	132	SSI1_DATAO
SSI2_FRAMEI	133	134	SSI3_FRAMEI

SSI2_DATAI	135	136	SSI3_DATAI
SSI2_CLKI	137	138	SSI3_CLKI
GND	139	140	GND
AGND	141	142	AGND
P3V3A	143	144	P3V3A
GND	145	146	GND
P3V3	147	148	P3V3
P3V3	149	150	P3V3
GND	151	152	GND
VBATT_RTN	153	154	VBATT_RTN
VBATT_RTN	155	156	VBATT_RTN
VBATT_RTN	157	158	VBATT_RTN
VBATT_RTN	159	160	VBATT_RTN
VBATT_RTN	161	162	VBATT_RTN
VBATT_RTN	163	164	VBATT_RTN
VBATT_RTN	165	166	VBATT_RTN
VBATT_RTN	167	168	VBATT_RTN
VBATT_PWR	169	170	VBATT_PWR
VBATT_PWR	171	172	VBATT_PWR
VBATT_PWR	173	174	VBATT_PWR
VBATT_PWR	175	176	VBATT_PWR
VBATT_PWR	177	178	VBATT_PWR
VBATT_PWR	179	180	VBATT_PWR
VBATT_PWR	181	182	VBATT_PWR
VBATT_PWR	183	184	VBATT_PWR
DGND	185	186	DGND
DGND	187	188	DGND
DGND	189	190	DGND
DGND	191	192	DGND
P5VBUS	193	194	P5VBUS
P5VBUS	195	196	P5VBUS
P5VBUS	197	198	P5VBUS
P5VBUS	199	200	P5VBUS

4.2. Nano-D Service Connector Pin Description

The 31-pin Nano-D connector is used to provide the GSE interface. Its pinout is defined in Table 2.

Table 2: Nano-D Connector Pinout

Pin No.	Designator	Description
1	DGND	Digital Ground
2	UART1_TX	UART1 RS22 Transmit
3	UART1_RX	UART1 RS22 Receive
4	P3V3	Digital 3.3V Power
5	GA_CPV	FPGA JTAG SPV
6	GA_TRST	FPGA JTAG TRST
7	GA_TDO	FPGA JTAG TDO
8	GA_TDI	FPGA JTAG TDI
9	GA_TMS	FPGA JTAG TMS
10	GA_TCK	FPGA TCK
11	P3V3	Digital 3.3V Power
12	GR_TDI	GR712 JTAG TDI
13	GR_TDO	GR712 JTAG TDO
14	GR_TMS	GR712 JTAG TMS
15	GR_TCK	GR712 JTAG TCK
16	TP11	GR_WDGn
17	DGND	Digital Ground
18	ETHR_TXEN	Ethernet PHY TXEN
19	ETHR_TXD0	Ethernet PHY TXD0
20	ETHR_TXD1	Ethernet PHY TXD1
21	ENET_RXD0	Ethernet PHY RXD0
22	ENET_RXD1	Ethernet PHY RXD1
23	ENET_CRSDV	Ethernet PHY CRSDV
24	ENET_PHYCLK	Ethernet PHY CLK
25	ENET_INTn	Ethernet PHY CINTn
26	ENET_MDIO	Ethernet PHY MDIO
27	ETHR_MDC	Ethernet PHY MDC
28	TP13	GR_RSTn
29	DGND	Digital Ground
30	TP12	SYS_RST
31	TP0	GR_ERRn

4.3. Sphinx SBC Physical Dimensions and Board Outline

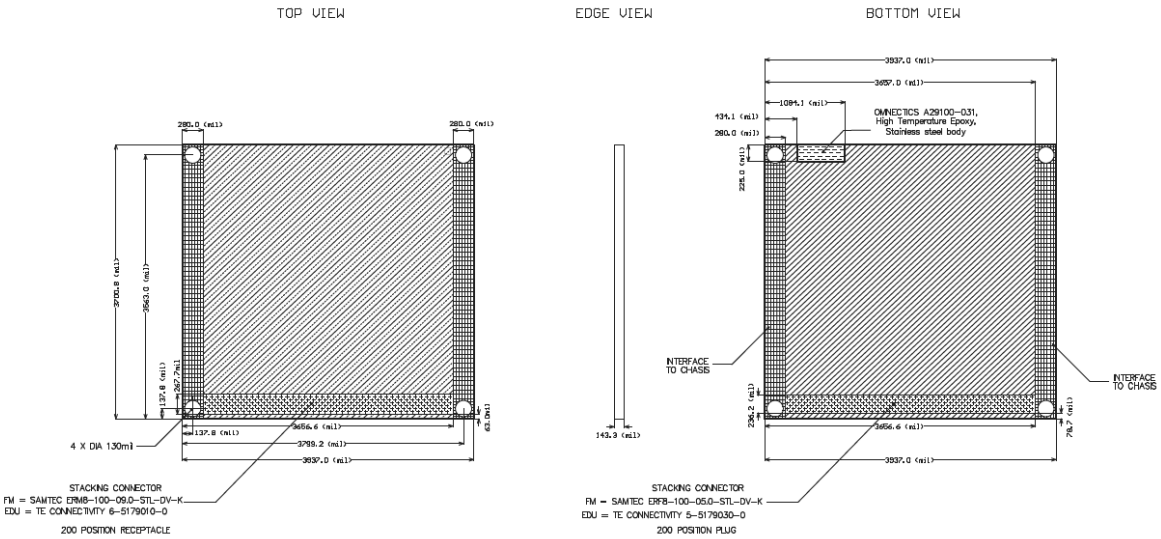

Figure 4.1: Sphinx SBC Board Outline

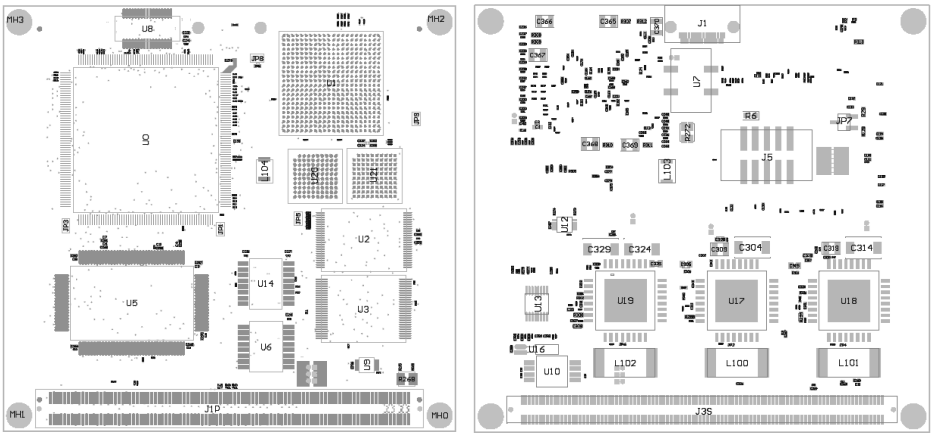

Figure 4.2: Sphinx Assembly Drawings

5. REVISION HISTORY

09/11/2024	0.0.1	Initial Released revision

Frontgrade Technologies – Datasheet Definitions

Datasheet Definitions

DEFINITION	
Advanced Datasheet	**Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the datasheet is subject to change. Specifications can be TBD and the part package and pinout are not final.**
Preliminary Datasheet	**Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.**
Datasheet	**Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.**