FRONTGRADE

DATASHEET

UT54BS32245

32-bit Bus Switch

8/9/2021
Version #: 2.0.5

Features

- 3.3V operating power supply with typical 11Ω switch connection between ports
- 5.0V operating power supply with typical 5Ω switch connection between ports
- Bidirectional operation
- Ultra-low power CMOS technology
- ESD Rating HBM: 2000V, Class 2
- Signal Isolation: -60dB
- Channel Bandwidth (3dB): 500MHz
- Standard Microcircuit Drawing (SMD):
  - 5962-15241
  - QML Q and V compliant part
- Package Options: 99-lead LGA, BGA, & CGA

Operational Environment

- Temperature Range: -55℃ to +125℃
- Total Dose: 300 krad(Si)
- SEL Immune: ≤100 MeV-cm^2/mg

Applications

- Memory Interface
- Bus Isolation
- Redundancy
- Supports Analog Applications

Introduction

The UT54BS32245 provides 32 bits of high-speed CMOS compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay. The device can be organized as four 8-bit bus switches, two 16-bit bus switches, or one 32-bit bus switch. When output enable (/ENn) is low, the switch is on and port A is connected to port B. When /ENn is high, the switch is open and a high-impedance state exists between the two ports.

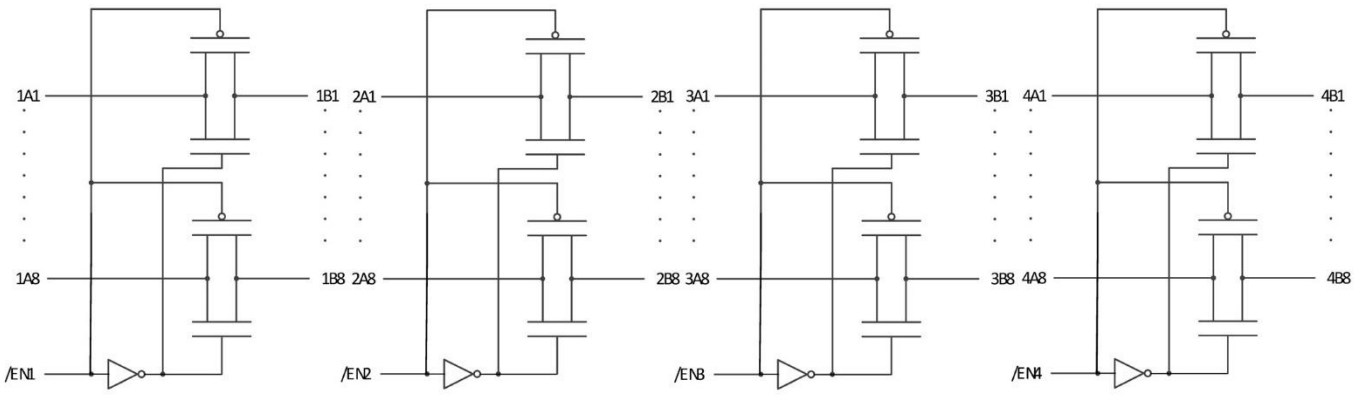


Figure 1: 32-bit Bus Switch Block Diagram

Pinlist

Table 1: Power and Ground Connections

Type	PINS
V_{SS}	A10, C5, C6, D4, D7, E3, E5, E6, E8, F3, F5, F6, F8, G4, H5, H6, K1, K10
V_{DD}	B2, B9, D5, D6, E4, E7, F4, F7, G5, G6, G7, J2, J9

Table 2: Channel Connections

Enable		A Channel Pins		B Channel Pins	
NAME	PIN	NAME	PIN	NAME	PIN
/EN1	H08	1A1	J10	1B1	J08
		1A2	H10	1B2	J07
		1A3	F10	1B3	H07
		1A4	G10	1B4	J06
		1A5	K07	1B5	H09
		1A6	K06	1B6	G09
		1A7	K09	1B7	G08
		1A8	K08	1B8	F09
/EN2	C08	2A1	E10	2B1	E09
		2A2	D10	2B2	D09
		2A3	B10	2B3	D08
		2A4	C10	2B4	C09
		2A5	A07	2B5	B07
		2A6	A08	2B6	C07
		2A7	A06	2B7	B06
		2A8	A09	2B8	B08
/EN3	C03	3A1	B01	3B1	B03
		3A2	C01	3B2	B04
		3A3	E01	3B3	C04
		3A4	D01	3B4	B05
		3A5	A04	3B5	C02
		3A6	A05	3B6	D02
		3A7	A02	3B7	D03
		3A8	A03	3B8	E02
/EN4	H03	4A1	F01	4B1	F02
		4A2	G01	4B2	G02
		4A3	J01	4B3	G03
		4A4	H01	4B4	H02
		4A5	K04	4B5	J04
		4A6	K05	4B6	H04
		4A7	K03	4B7	J05
		4A8	K02	4B8	J03

Package Pinout Diagram

Top View

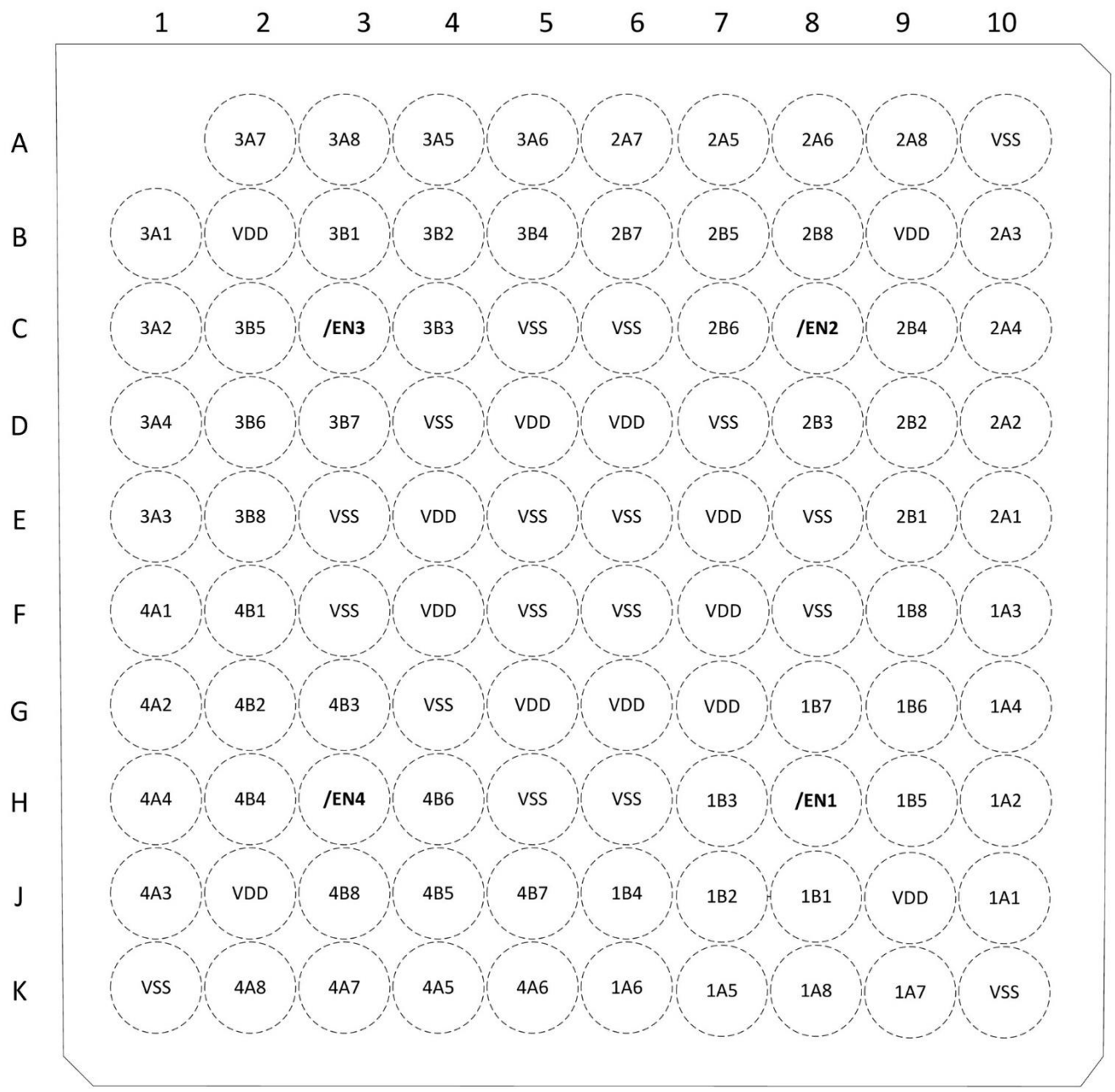


Figure 2: 99 - Lead CCGA, CLGA, CBGA – Top View

Absolute Maximum Ratings[1,2]

Table 3: Absolute Maximum Ratings

Symbol	Parameter	MIN	MAX	Units
V_{DD}	Positive Supply Voltage	-0.5	+7.2	V
V_I	Input Voltage	-0.5	V_{DD}+0.3	V
I_{CCC}	DC Channel Current		65	mA
P_D	Max Power Dissipation[3]		1.6	W
T_J	Junction Temperature		+150	°C
Θ_{JC}	Thermal resistance, junction-to-case		15	°C/W
T_{STG}	Storage Temperature	-65	+150	°C
ESD_{HBM}	ESD Protection[4]		2000	V

Notes:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification are not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability and performance.
2. All voltages referenced to V_{SS}
3. Per MIL-STD-883, method 1012, section 3.4.1, $P_D=(T_J(max)-T_C(max))/\Theta_{JC}$)
4. Per MIL-STD-883, method 3015, Table 3

Operational Environment[1]

Table 4: Operational Environment

Symbol	Parameter	Limit	Units
TID	Total Ionizing Dose[2]	300	krad(Si)
SEL	Single Event Latchup Immunity[3]	≤100	MeV-cm^2/mg

Notes:

1. For devices with procured with a total ionizing dose tolerance guarantee, post-irradiation performance is guaranteed at 25°C per MIL-STD-883 Method 1019, Condition A up to maximum TID level procured.
2. Per MIL-STD-883, method 1019, condition A
3. SEL is performed at V_{DD} = Max Voltage at 125°C

Recommended Operating Conditions[1]

Table 5: Recommended Operating Conditions

Symbol	Parameter	Conditions	MIN	MAX	Units
V_{DD}	Positive Supply Voltage		3.0 or 4.5	3.6 or 5.5	V
V_{IN}	Input Voltage on any pin		0.0	V_{DD}	V
T_C	Case Temperature Range		-55	+125	℃
t_R	Rise time, logic inputs	Transition from V_{IL} to V_{IH}		5	ns
t_F	Fall time, logic inputs	Transition from V_{IH} to V_{IL}		5	ns
I_{CCC}	DC Channel Current			60	mA

Note:

1. All voltages referenced to V_{SS}

Electrical Characteristics[1]

(V_{DD}= 5.0V ± 0.5V, 3.3V ± 0.3V, -55°C< T_C <+125°C); Unless otherwise noted, T_C is per the temperature range ordered

Table 6: DC Electrical Characteristics

Symbol	Parameter	Conditions	MIN	MAX	Units
V_{IH}	High digital input voltage	V_{DD} = 3.6, 5.5	0.7* V_{DD}		V
V_{IL}	Low digital input voltage	V_{DD} = 3.0, 4.5		0.3* V_{DD}	V
I_{ID}	Leakage current digital	V_{DD} (max); V_I=V_{DD} or V_{SS}	-1	1	µA
I_{IA}	Leakage current analog	V_{DD} (max); V_I=V_{DD} or V_{SS}	-1	1	µA
I_{DD}	Active supply current	V_{DD} = 3.6, 5.5		0.1	mA/MHz
I_{DDQ}	Quiescent Supply Current	V_{DD} (max); I_O=0mA; /EN=V_{DD}		15	µA
C_I	Input Capacitance (/EN)[2]	V_I=V_{DD} or V_{SS}		18	pF
$C_{IO(OFF)}$	Channel pin capacitance (channel disabled)[2]	V_{DD} (max); V_O=V_{DD} or V_{SS}; V_I=V_{DD}/2; /EN=V_{DD}		18	pF
R_{ONL}	Resistance through switch (channel input low)[3]	V_{DD}=4.5V, V_I=V_{SS}, /EN=0V, I_O=30mA		10	Ω
		V_{DD}=4.5V, V_I=V_{SS}, /EN=0V, I_O=15mA		10	Ω
		V_{DD}=3.0V, V_I=V_{SS}, /EN=0V, I_O=30mA		12	Ω

Symbol	Parameter	Conditions	MIN	MAX	Units
		V_{DD}=3.0V, V_I=V_{SS}, /EN=0V, I_O=15mA		12	Ω
R_{ONH}	Resistance through switch (channel input high)[3]	V_{DD}=4.5V, V_I=V_{DD}, /EN=0V,I_O=-30mA		10	Ω
		V_{DD}=4.5V, V_I=V_{DD}, /EN=0V,I_O=-15mA		10	Ω
		V_{DD}=3.0V, V_I=V_{DD}, /EN=0V,I_O=-30mA		12	Ω
		V_{DD}=3.0V, V_I=V_{DD}, /EN=0V,I_O=-15mA		12	Ω
$R_{ON(FLAT)}$	Switch on resistance[3]	V_{DD}=4.5V, /EN=0V, I_O=+/-15mA, 25°C V_{IN} = V_{SS}, V_{DD} /2, V_{DD}		2	Ω
		V_{DD}=3.0V, /EN=0V, I_O=+/-15mA, 25°C V_{IN} = V_{SS}, V_{DD} /2, V_{DD}		10	Ω

Notes:

1. All voltages referenced to V_{SS}
2. Per MIL-STD-883, method 3012
3. Guaranteed by Characterization

AC Electrical Characteristics[1]

(V_{DD}= 5.0V ± 0.5V, 3.3V ± 0.3V, -55°C< T_C <+125°C); Unless otherwise noted, T_C is per the temperature range ordered

Table 7: AC Electrical Characteristics

Symbol	Parameter	Conditions	MIN	MAX	Units
t_{PD15}	Channel Propagation Delay[1]	V_{DD}= 5.0V ± 0.5V, I1=+/-15mA, /EN=V_{SS}		250	ps
t_{EN}	Channel Enable Delay[2]	V_{DD}= 5.0V ± 0.5V	1	4	ns
t_{DIS}	Channel Disable Delay[2]	V_{DD}= 5.0V ± 0.5V	1	4	ns
t_{PD15}	Channel Propagation Delay[1]	V_{DD}= 3.3V ± 0.3V, I1=+/-15mA, /EN=VSS		250	ps
t_{EN}	Channel Enable Delay[2]	V_{DD}= 3.3V ± 0.3V	1	6	ns
t_{DIS}	Channel Disable Delay[2]	V_{DD}= 3.3V ± 0.3V	1	6	ns

Notes:

1. The propagation delay through the channel is based on the RC time constant of the channel capacitance and maximum channel resistance for defined V_{DD}
2. Measured at 300mV above or below steady state output voltage using output test load circuit

Table 8: Signal Characteristics

Symbol	Parameter	Conditions	MIN	TYP	MAX	Units
X_{TALK}	Channel Cross-Talk[1,2]	V_{DD} = 5.0V			-60	dB
X_{TALK}	Channel Cross-Talk[1,2]	V_{DD} = 3.3V			-60	dB
ISO_{OFF}	Off Isolation[1,2]				-60	dB

Notes:

1. Guaranteed by characterization
2. R_L = 50Ω, C_L = 50pF, fin = 1MHz, Vin = 1VRMS centered at $V_{DD}/2$

Timing Diagram

Figure 3: Channel Propagations Delay (/EN = V_{SS})

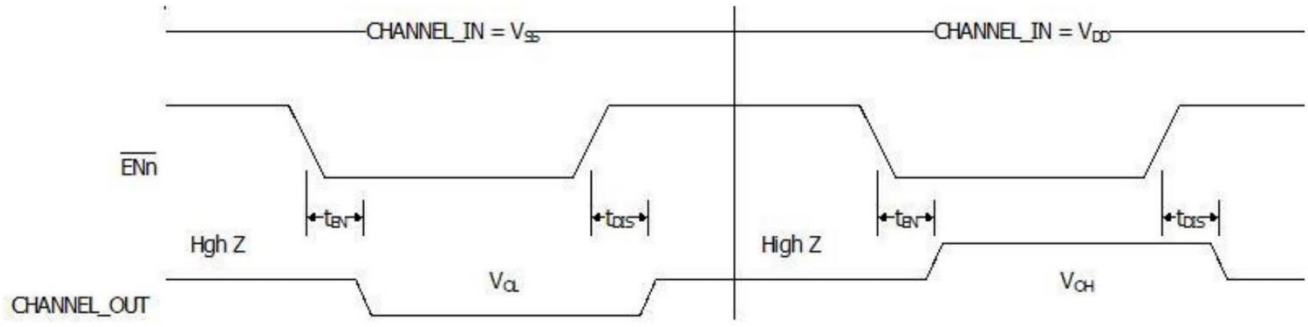


Figure 4: Enable Timing

Test Loads

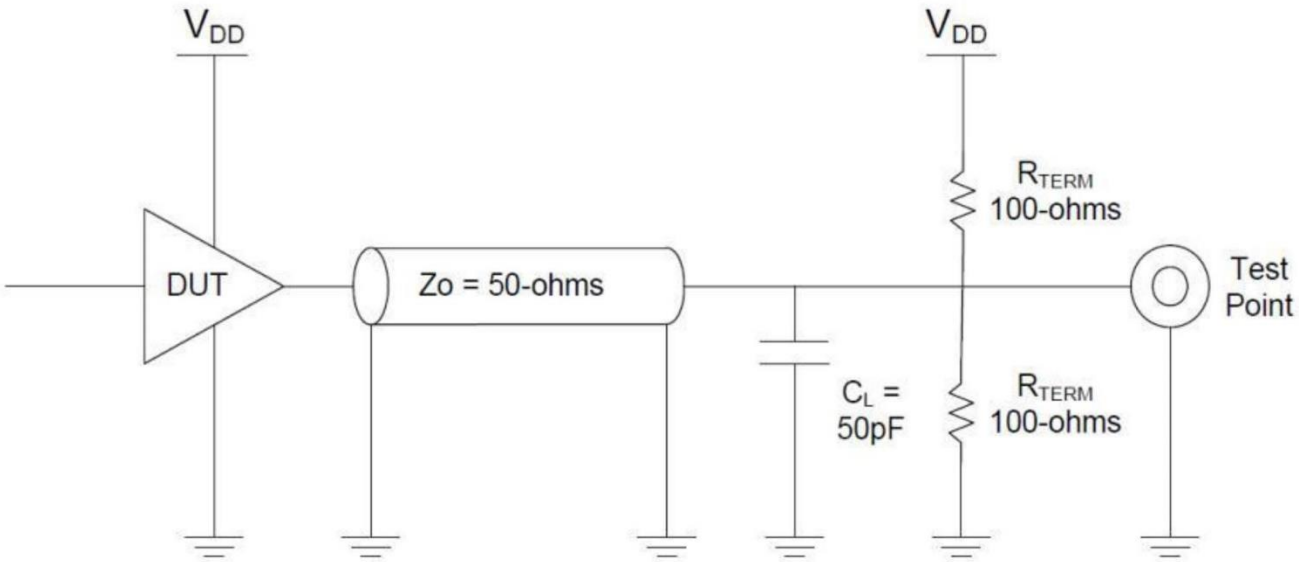


Figure 5: Standard Test Load

Package Drawings

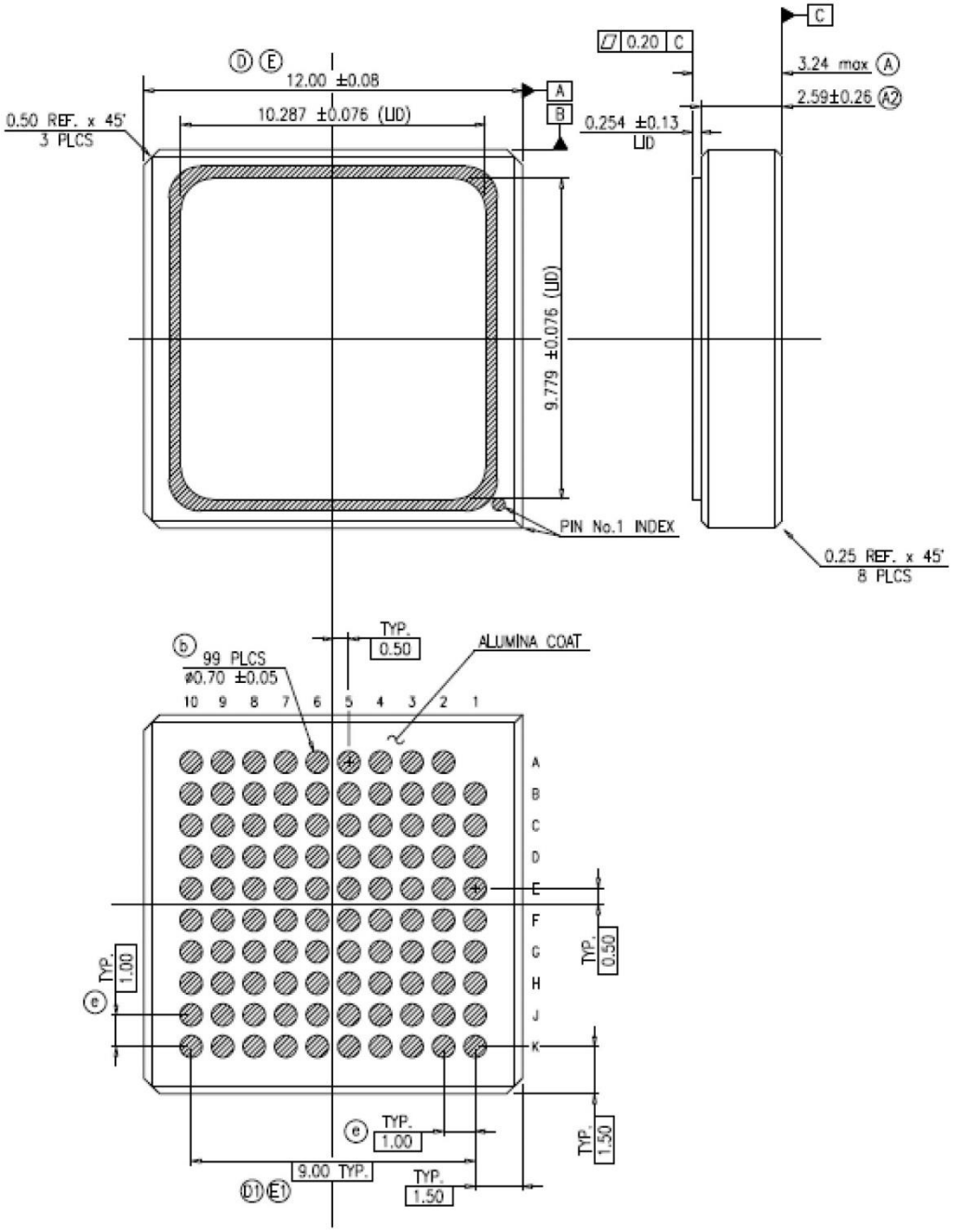


Figure 6: 99-Lead CLGA

Notes:

1. Material is 90% alumina (∈r = 9.8)
2. Lid is connected to V_{SS}
3. Units are millimeters

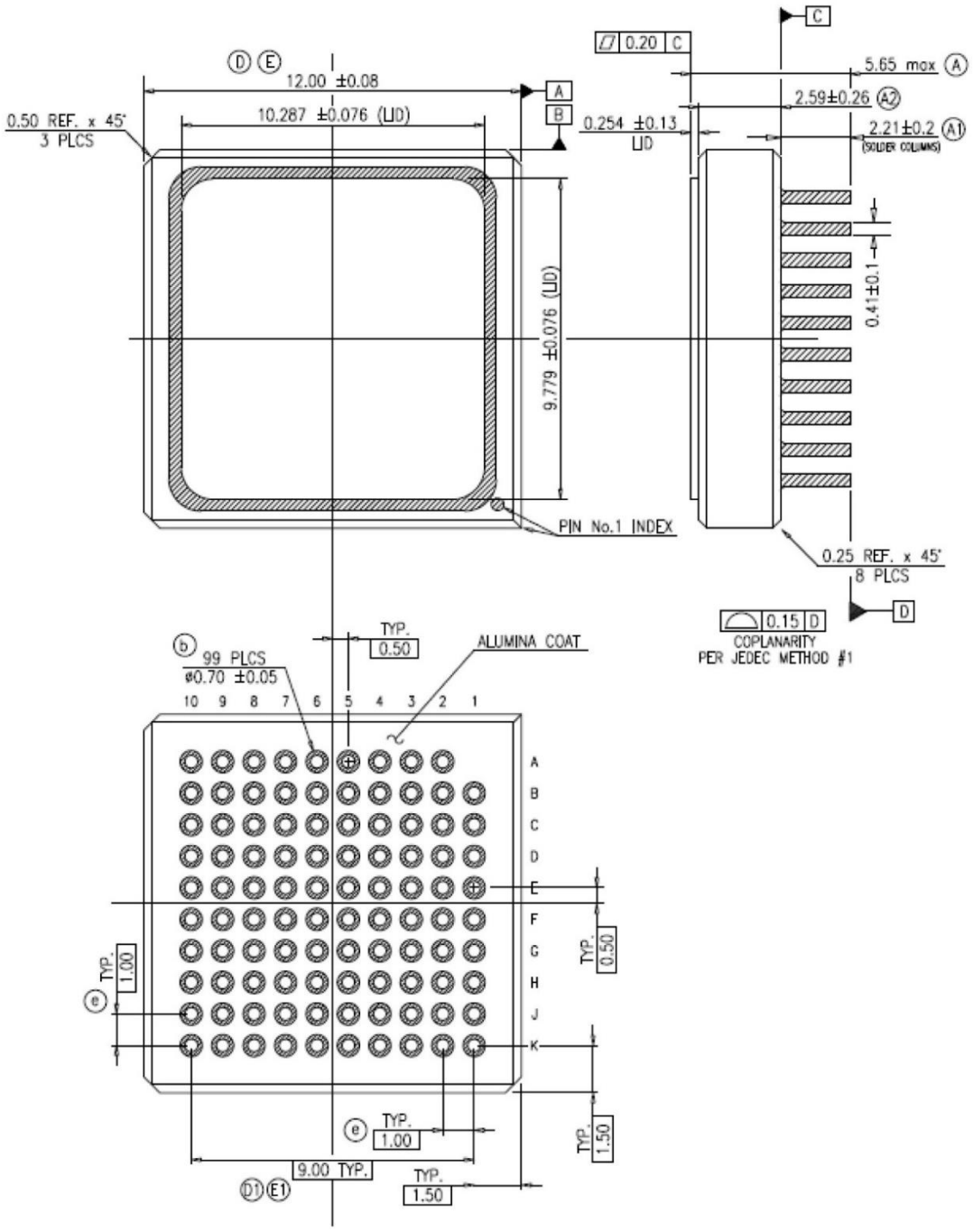


Figure 7: 99-Lead CCGA

Notes:

1. Material is 90% alumina (∈r = 9.8)
2. Lid is connected to V_{SS}
3. Units are millimeters

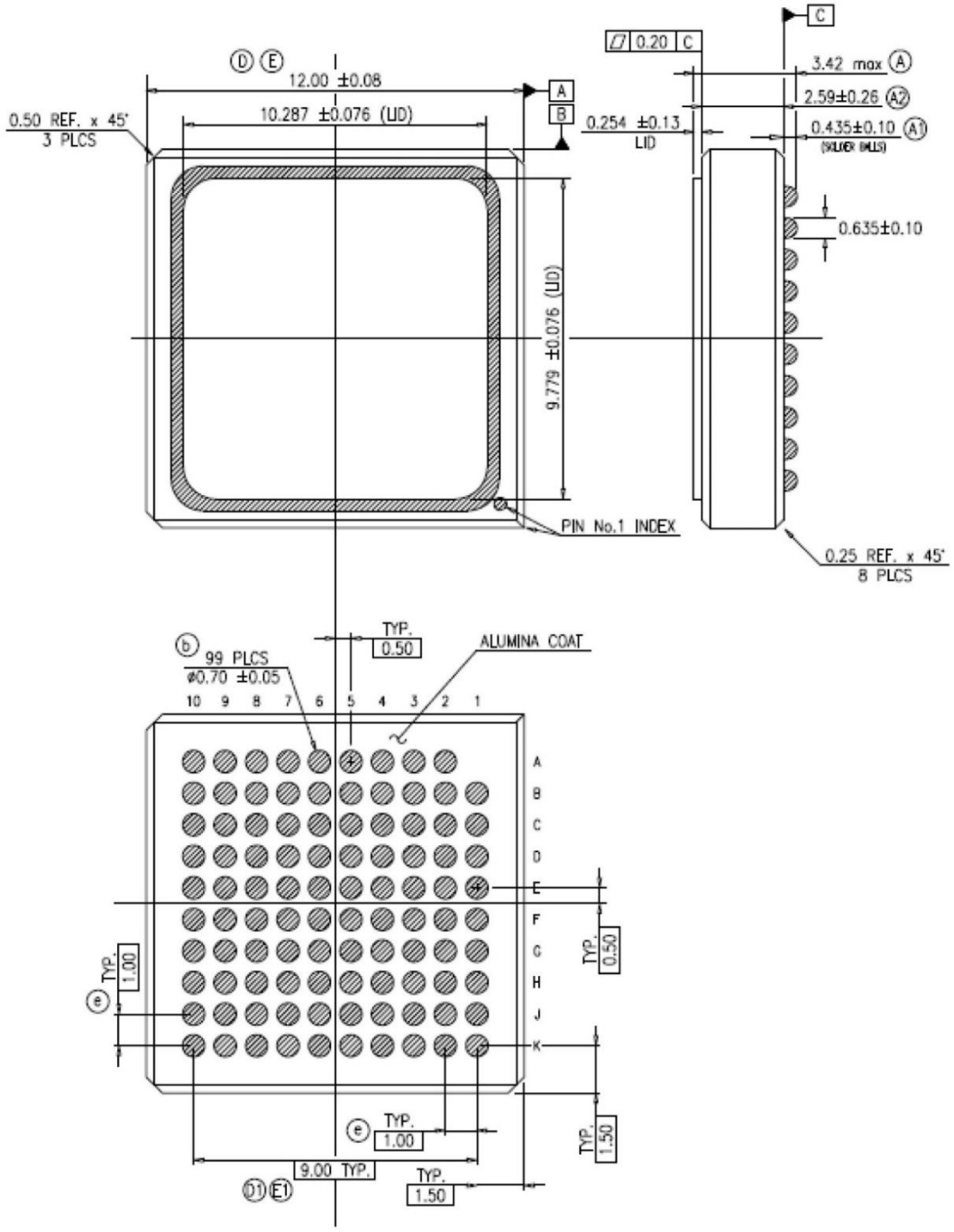


Figure 8: 99-Lead CBGA

Notes:

1. Material is 90% alumina (Er = 9.8)
2. Lid is connected to V_{SS}
3. Units are millimeters

Ordering Information

Frontgrade Part Numbering Ordering Information

UTxxxxxxxx * * * *

Lead Finish:
(A) = Hot Solder Dipped or Tinned
(C) = Gold

Screening Level: (Notes: 1,2,4)
(P) = Prototype Flow (Temperature Range: 25°C only)
(C) = HiRel Flow (Temperature Range: -55°C to +125°C)

Case Outline: (Notes: 3,4)
(Z) = 99-Ceramic Land Grid Array
(S) = 99-Ceramic Column Grid Array
(C) = 99-Ceramic Ball Grid Array

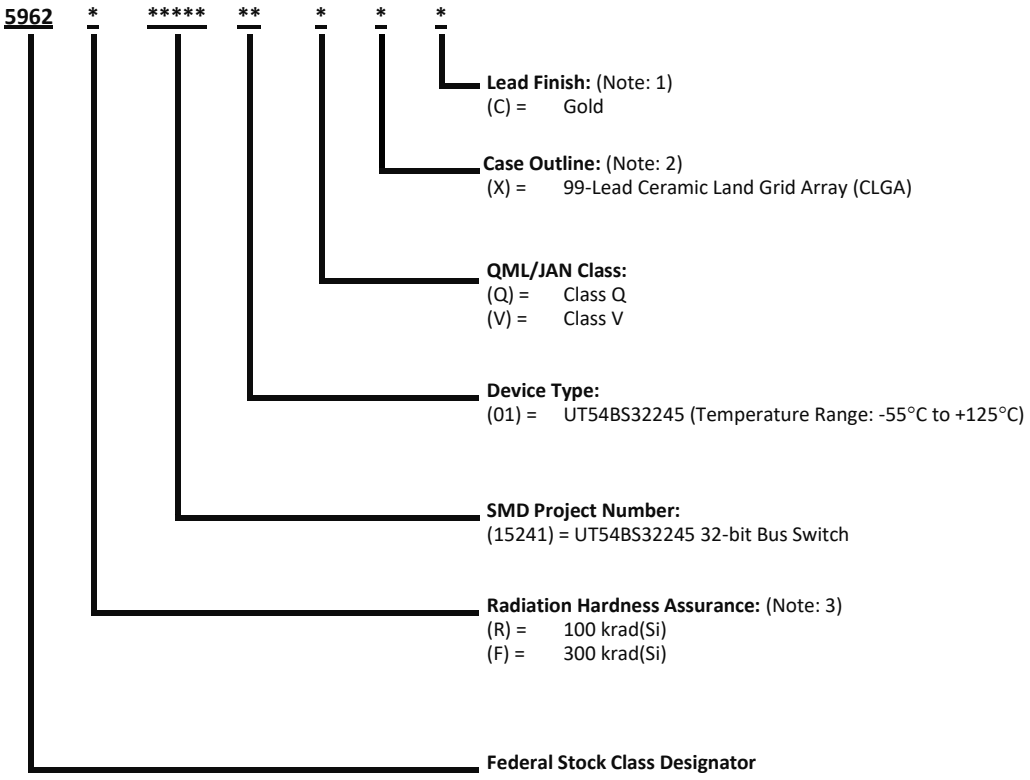
Access Time:
(-)

Generic part number:
(54BS32245)

Notes:

4. Prototype Flow per Frontgrade Manufacturing Flows Document. Lead finish is Factory Option "C" - only. Radiation is neither tested nor guaranteed.
5. HiRel Flow per Frontgrade Manufacturing Flows Document. Radiation TID tolerance may (or may not) be ordered.
6. For Ceramic Land Grid Array (CLGA) packages, the lead finish is “C” (Gold-only). For Ceramic Ball Grid Arrays (CBGA) and Ceramic Column Grid Array (CCGA) packages, the lead finish is “A” (Hot Solder Dipped).
7. Ceramic Ball Grid Array (CBGA) package option is for Prototype Flow only.

SMD Part Number Ordering Information



Notes:

1. For ceramic Land Grid Array (LGA) packages, the lead finish is “C” (Gold-only).
2. Frontgrade offers Column Attachment as an additional service for the Ceramic Column Grid Array (CCGA), Case Outline “S.” If needed, please ask for COLUMN ATTACHMENT when submitting your request for quotation.
3. A radiation hardness assurance level must be selected. The use of “-” indicates no radiation hardness assurance guarantee.

Revision History

Date	Revision #	Author	Change Description	Page #
05/01/2016	1.0.0	MM	Updated datasheet to reflect Frontgrade logo, colors, and modified format. Updated the following specifications: RON, IIA, IDD, IDDQ, TEN, and TDIS.	
06/23/2016	2.0.0	BM	Released Datasheet. Updated capacitance, propagation delay, and minor formatting.	
08/11/2016	2.0.1	BM	Updated Fig. 2 to show dashed landing pads for Top View	5
01/04/2017	2.0.2	BM	FEATURES: QML Q and V compliant part	
04/11/2017	2.0.3	BM	Added note: Order info., CBGA package for Protos only	11
05/31/2018	2.0.4	BM	Correction: Table 2: H03=/EN4, Package Pinout Diag.: /OEn →/ENn	2, 3
08/19/2021	2.0.5	BM	ROC Table, p.4: Input tR, tF parameter updates.	

Datasheet Definitions

	Definition
Advanced Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the **datasheet is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final.**
Preliminary Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.